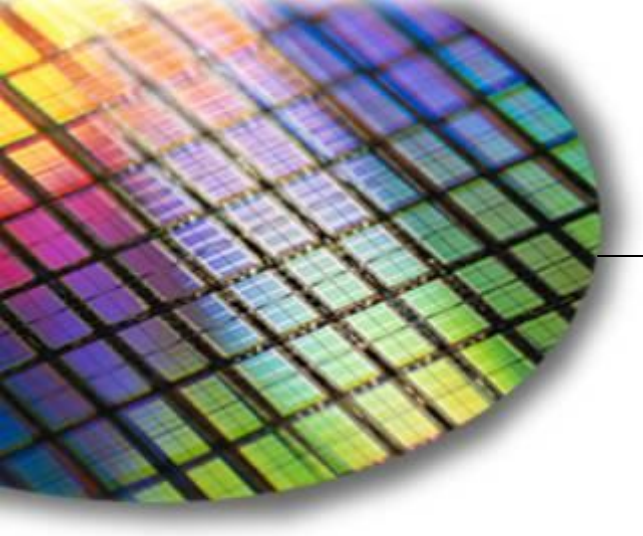

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High-performance GSPS Data Converter Technology Enables Simplified RADAR & EW Architectures

by

Rob Reeder

July 2014

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ANALOG DEVICES

Today we'll cover:

- Wideband Signal Processing: What is it, and why is it so Important?
- Radar Applications and Systems
- Radar Signal Chain Review – Classic vs. GSPS converter-enabled
- GSPS Converter Front-ends: Amplifiers vs. Baluns
- Tools and Collateral
- Q&A

What is Wideband Signal Processing?

- Data acquisition and signal synthesis signal chain solutions that address applications with a critical need for high dynamic range and noise performance at DC to up to 2 GHz bandwidths
- GSPS ADCs have been available for some time, but the performance achieved at 1 GHz+ bandwidths has not been good enough to enable advanced architectures in many leading-edge applications.
- ADI has introduced a couple of GSPS A/D converter cores that have set new standards in wideband performance:

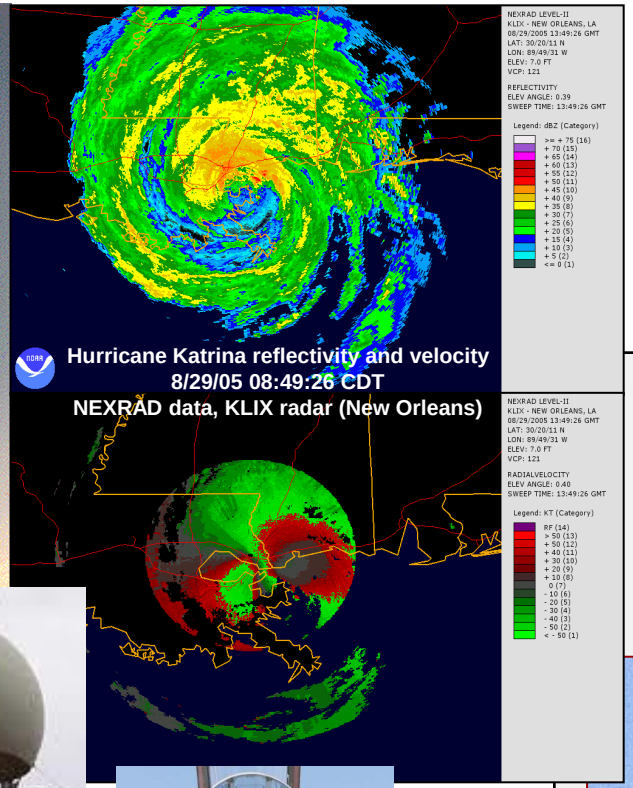
  AD9625 - 12-bit, 2.0/2.5 GSPS JESD204B ADC w/DDC that delivers 80 dBFS at 1 GHz Ain

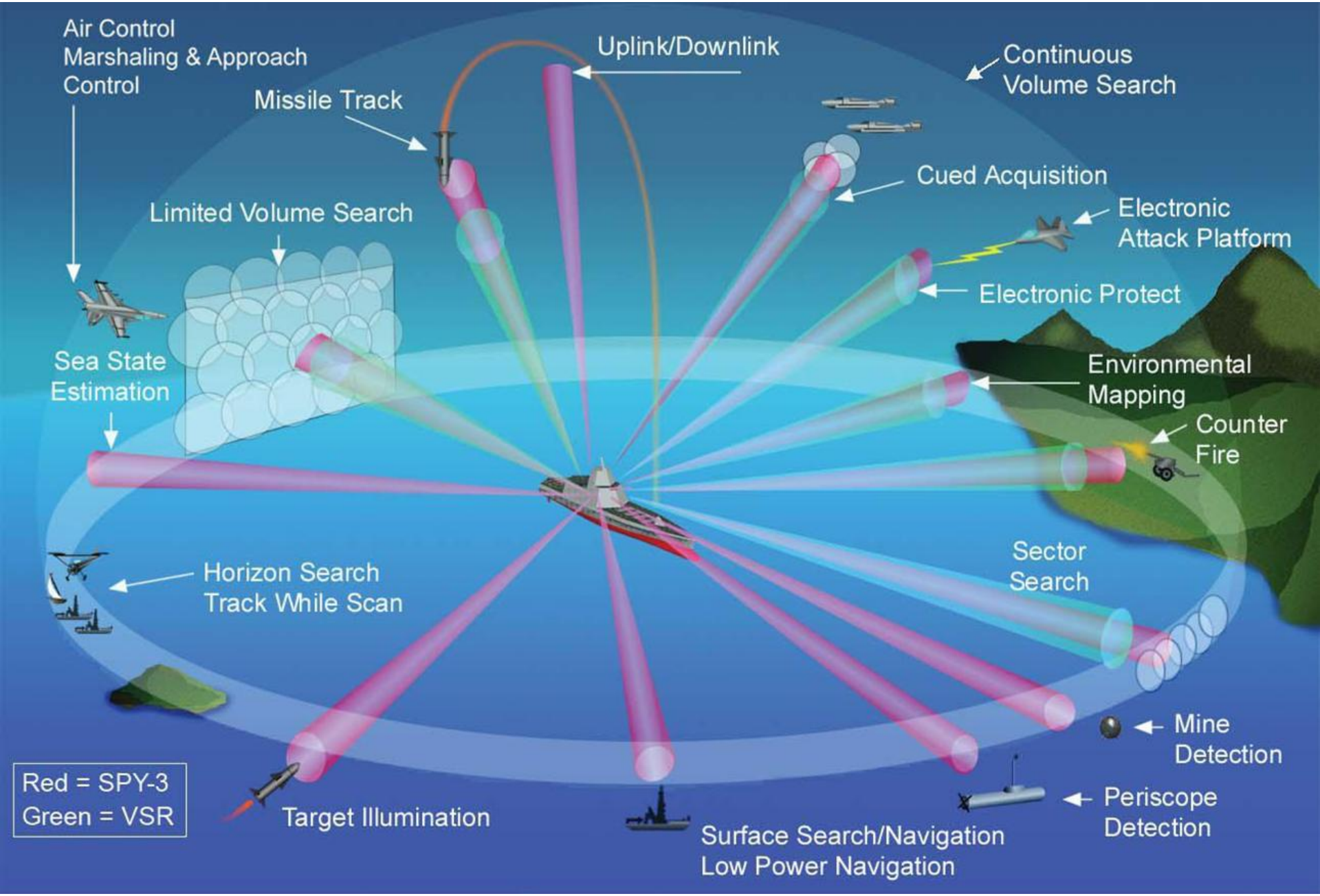
  AD9640 - Dual 14-bit, 1.0 GSPS JESD204B ADC w/DDC that delivers 85 dBc at 340 MHz Ain

- This new level of wideband performance and functionality is set to initiate the next generation system designs in high-end, cutting edge Aerospace and Defense's RADAR systems, RF test equipment and wireless and wired communication infrastructure applications.

Radar & Electronic Warfare Applications

Weather Radar

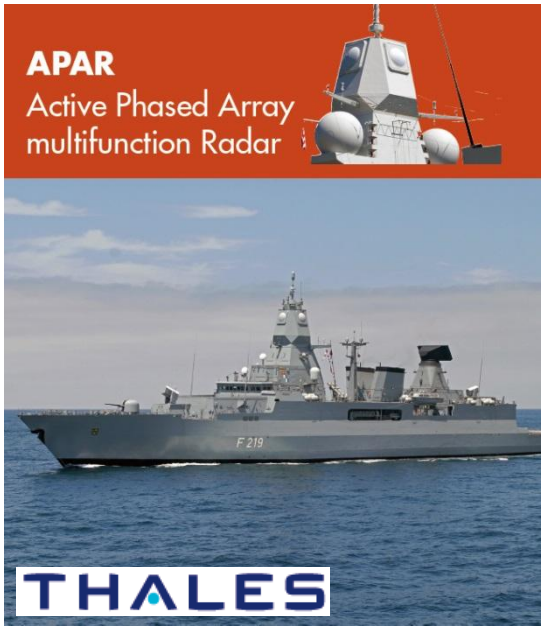



Air Control
Marshaling & Approach
Control
Missile Track
Uplink/Downlink
Continuous
Volume Search
Cued Acquisition
Limited Volume Search
Electronic
Attack Platform
Electronic Protect
Sea State
Estimation
Environmental
Mapping
Counter
Fire
Horizon Search
Track While Scan
Sector
Search
Mine
Detection
Red = SPY-3
Green = VSR
Target Illumination
Surface Search/Navigation
Low Power Navigation
Periscope
Detection

Radar-Applications

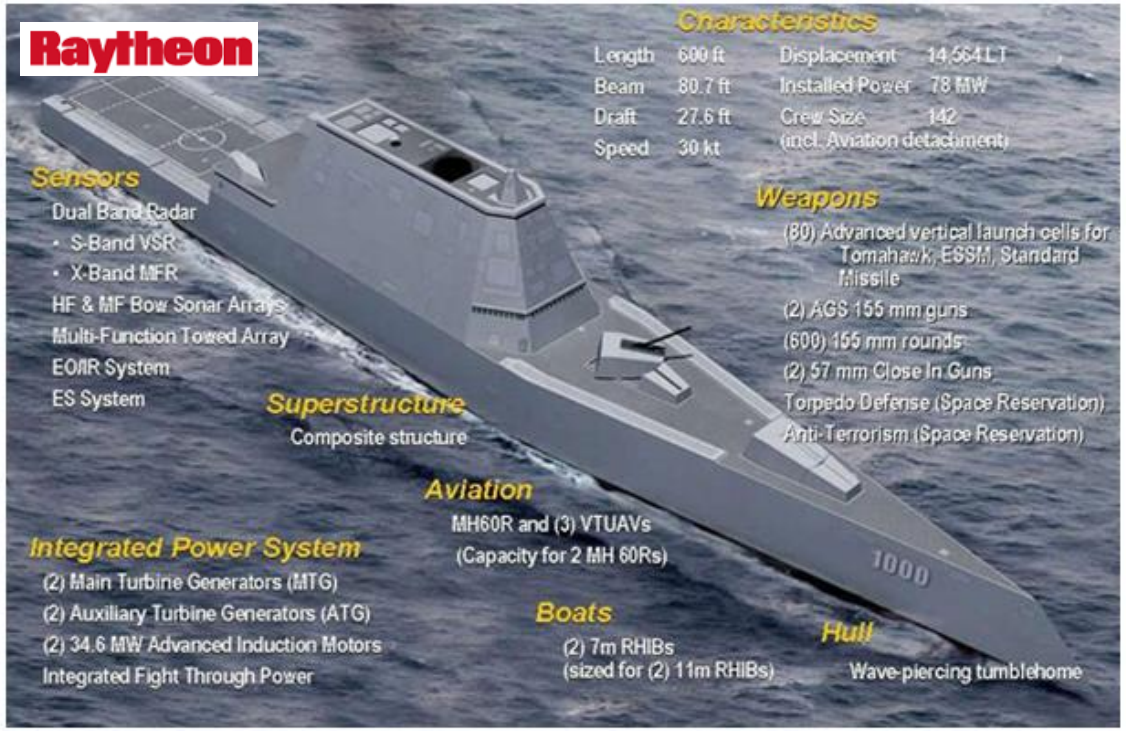
- *Search / Track and Fire Control*
  - Multi-Role Electronically Scanned Array (MESA)
    - simultaneous air and sea search
    - fighter control and area search
  - Active Electronically Scanned Array (AESA)
    - Phased Array RADAR
    - Aim their "beam" by emitting separate radio waves from each module that interfere constructively at certain angles in front of the antenna.
    - allow ships and aircraft to broadcast powerful radar signals while still remaining stealthy
  - Passive electronically scanned array (PESA)
    - Phased Array which has a **central** RF source
      - *Magnatron, Klystron, Traveling Wave Tube (TWT) or High Power GaN on SiC*
    - *Easier to build*

Multi-Function, dual-band, sea/air/land is the newest platform type. SWaP.



LOCKHEED MARTIN

Nowhere to Run, Nowhere to Hide



DDG 1000 design features and systems. The Zumwalt Class will be multimission vessels tailored for land attack and littoral dominance.

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Radar Frequency Allocations

IEEE US

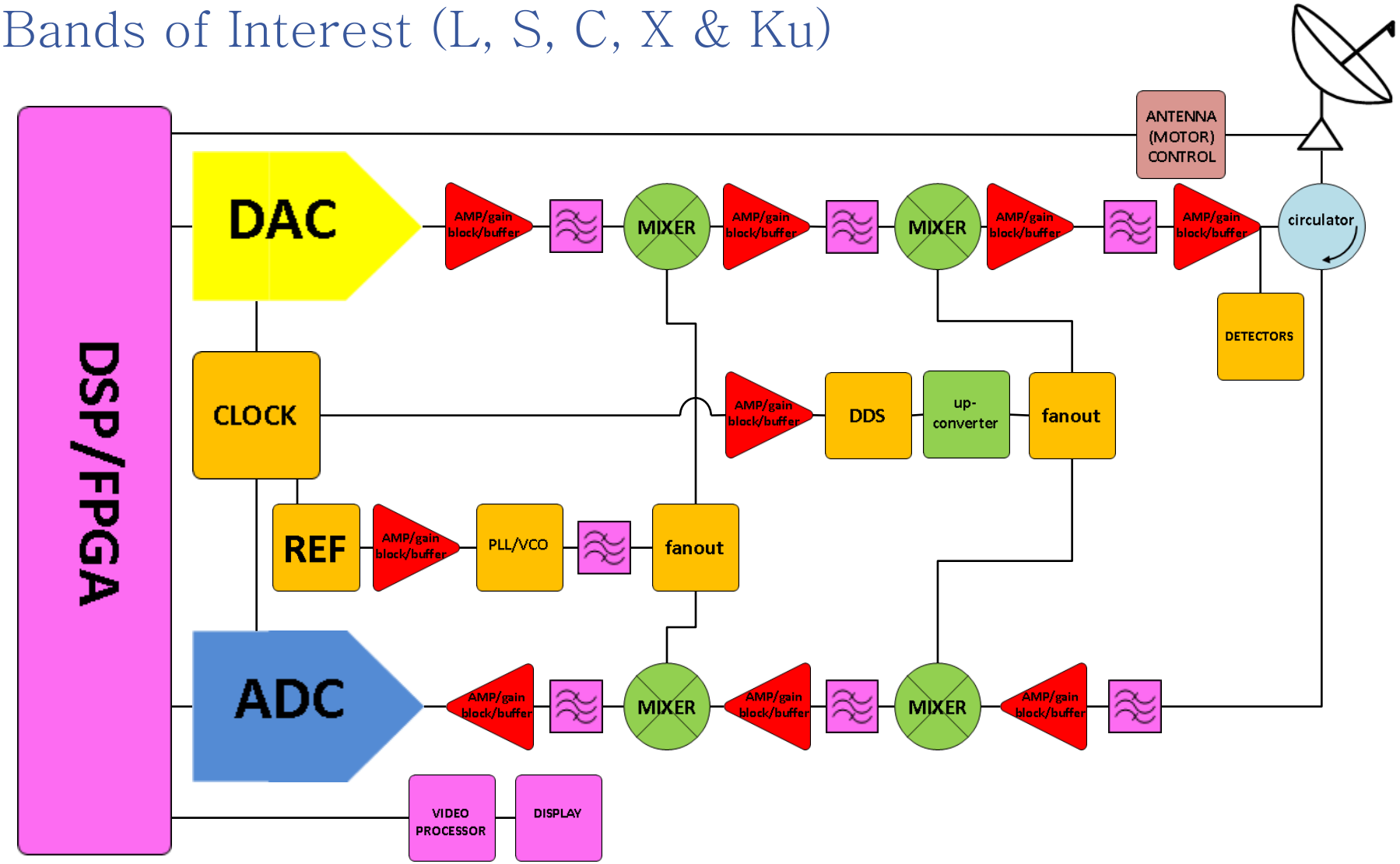
Table of IEEE bands

Band	Frequency range	Origin of name [*citation needed*]
HF band	3 to 30 MHz	**H**igh **F**requency
VHF band	30 to 300 MHz	**V**ery **H**igh **F**requency
UHF band	300 to 1000 MHz	**U**ltra **H**igh **F**requency
L band	1 to 2 GHz	**L**ong wave
S band	2 to 4 GHz	**S**hort wave
C band	4 to 8 GHz	**C**ompromise between S and X
X band	8 to 12 GHz	Used in WW II for fire control, X for cross (as in crosshair)
K_u band	12 to 18 GHz	**K**urz-**u**nder
K band	18 to 27 GHz	German **K**urz (short)
K_a band	27 to 40 GHz	**K**urz-**a**bove
V band	40 to 75 GHz	
W band	75 to 110 GHz	**W** follows V in the alphabet
mm band	110 to 300 GHz	

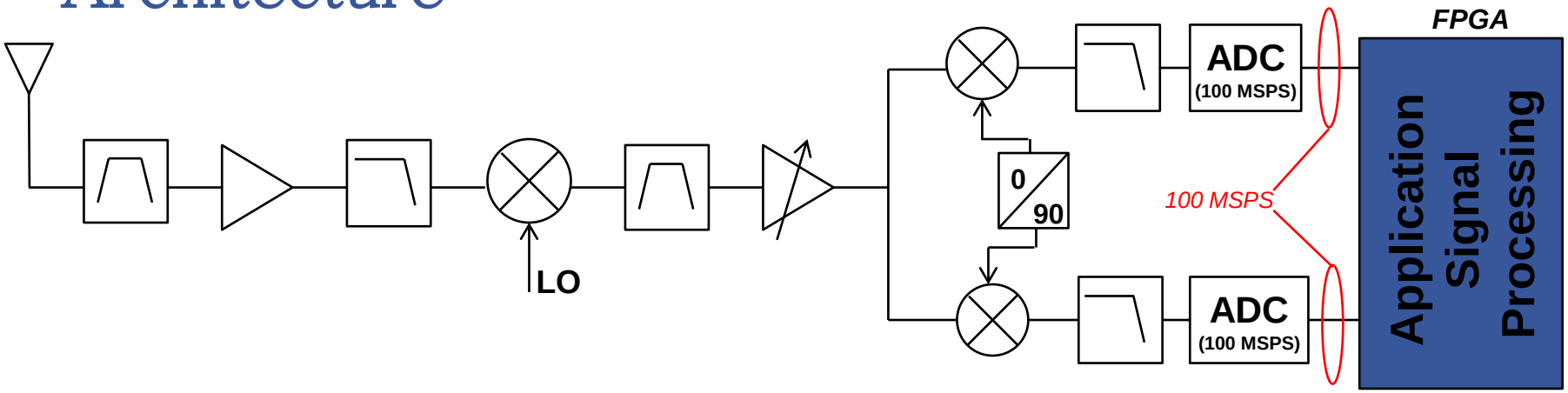
EU, NATO, US ECM frequency designations

Band	Frequency range
A band	0 to 0.25 GHz
B band	0.25 to 0.5 GHz
C band	0.5 to 1.0 GHz
D band	1 to 2 GHz
E band	2 to 3 GHz
F band	3 to 4 GHz
G band	4 to 6 GHz
H band	6 to 8 GHz
I band	8 to 10 GHz
J band	10 to 20 GHz
K band	20 to 40 GHz
L band	40 to 60 GHz
M band	60 to 100 GHz

Classic RADAR Signal Chain Covers all Frequency Bands of Interest (L, S, C, X & Ku)

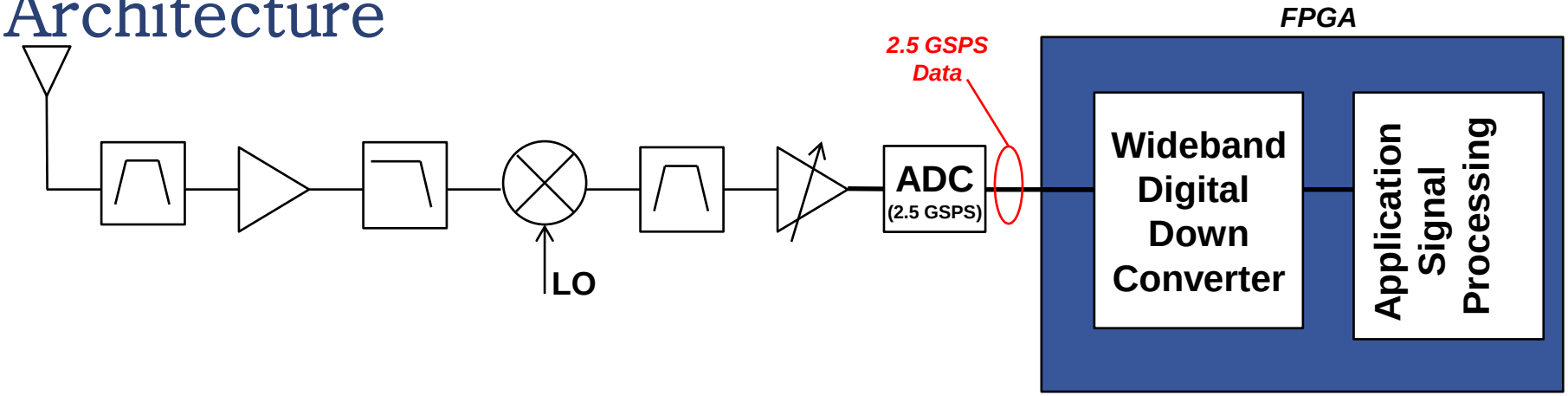


A Closer Look at The Traditional Radar Receiver Architecture



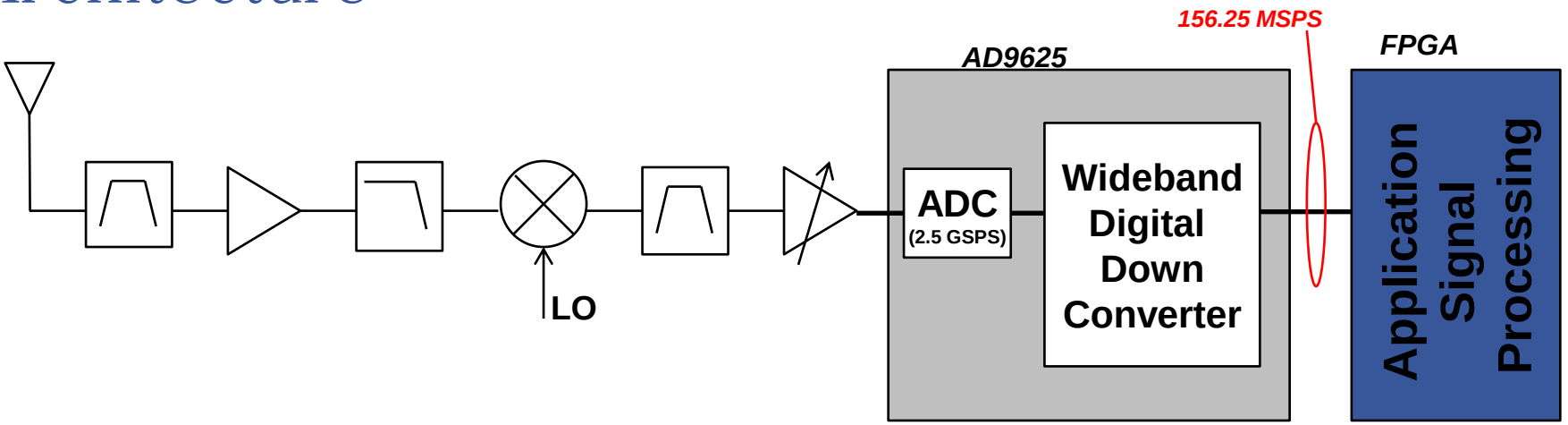
- Typical Super Heterodyne Receiver Architecture
  - Dual Mixing stages to reduce data first to an IF and then to baseband.
    - Second stage could be complex or real depending on requirements
  - Application specific functionality implemented inside the FPGA.
    - FPGA functionality may include a Digital Down Conversion (DDC). Assuming digitization rates are < 100 MHz DDC is relatively simple to implement as minimal parallelization needed.

Giga Sample Per Second ADC-enabled Architecture



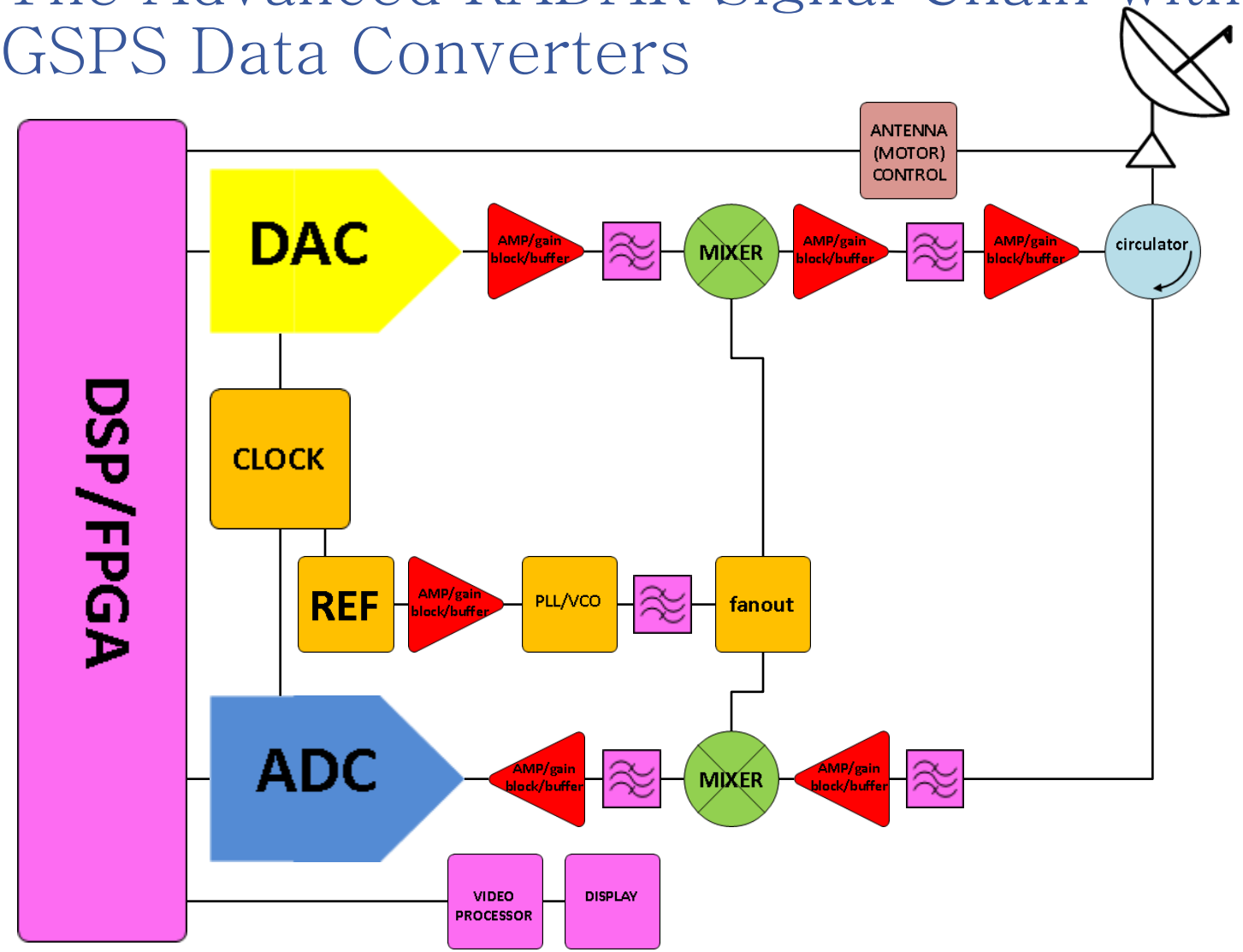
- **Higher Sampling Rate ADCs enable Direct IF / RF Sampling**
  - Giga-sample per second ADCs enable the RF or IF feeds to be digitized directly simplifying the system architecture and number of components
  - This increases the system flexibility as more functionality is processed in the digital domain
  - Often a stage of Digital Down Conversion is required and due to the high ADC data rates.
  - JESD204B serial interface technology is incorporated in the converter and FPGA which simplifies the interface, supports a high data rate, and provides synchronization and deterministic latency capabilities.

Giga Sample Per Second ADC-enabled Architecture



- **Integrated DDCs in AD9625 and AD9680 enable high sampling rates and reduce further down conversion requirements in downstream FPGA**
  - **Wideband DDC in AD9625 reduces data rate to 156.25 MSPS.**
    - Reduces FPGA processing required for narrowband data
    - Less parallelism needed in FPGA processing, simplifying logic, reducing power consumption and enabling more FPGA resources for user signal processing

The Advanced RADAR Signal Chain with GSPS Data Converters

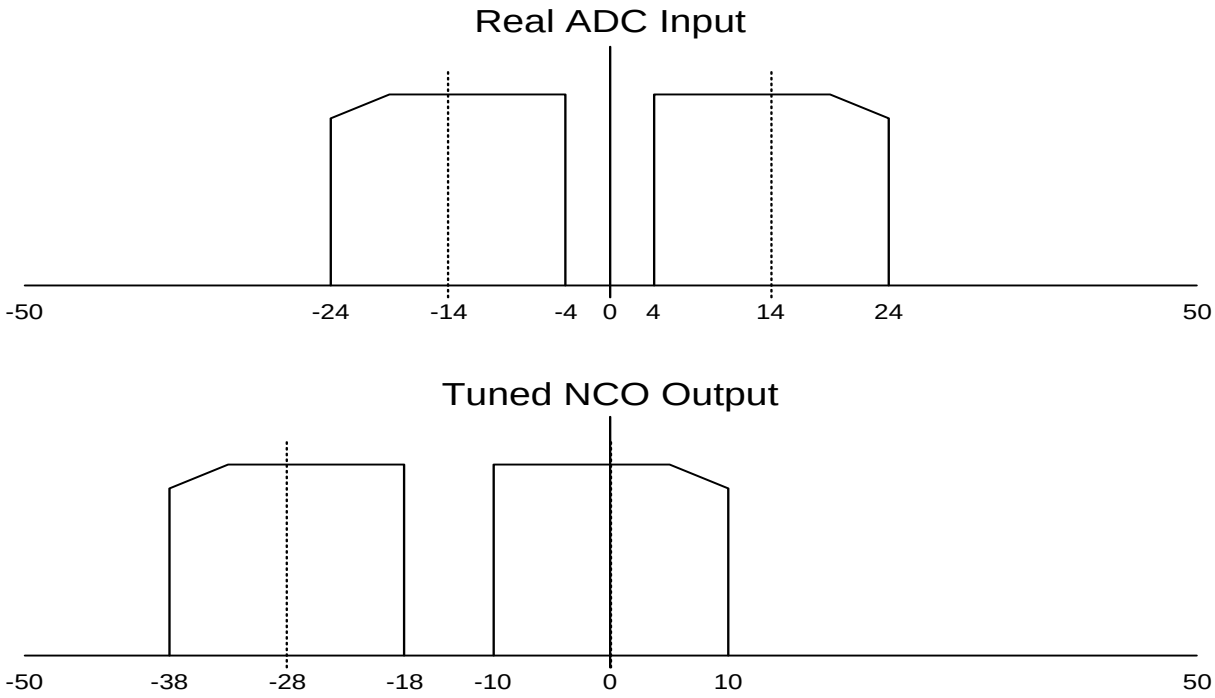


Moving Towards Digital in Radar Designs

- Giga-sample/second ADCs & DACs Increase System Options:
  - High frequency IFs or possibly direct RF conversion
  - Reduced RF components and circuitry reducing system size weight and power (SWAP)
  - Greater flexibility as more data is available in the digital domain
- Higher frequency ADCs Brings New Challenges:
  - New higher performance wider band ADC drivers are needed
  - Removing an IF mixing stage requires broad-band flexible mixers & wideband LNAs & passive devices

NCO Frequency Translation Example

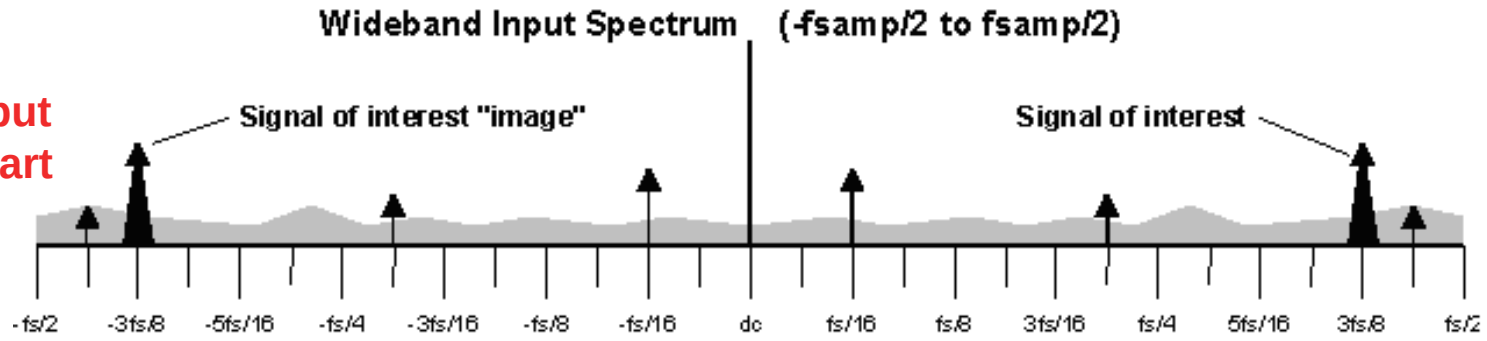
- Example:
  - 20 MHz Band centered at 14MHz tuned to Baseband. 100MHz ADC Sample Rate.
- Decimation Filters must reject negative image of the NCO.



DDC Operation

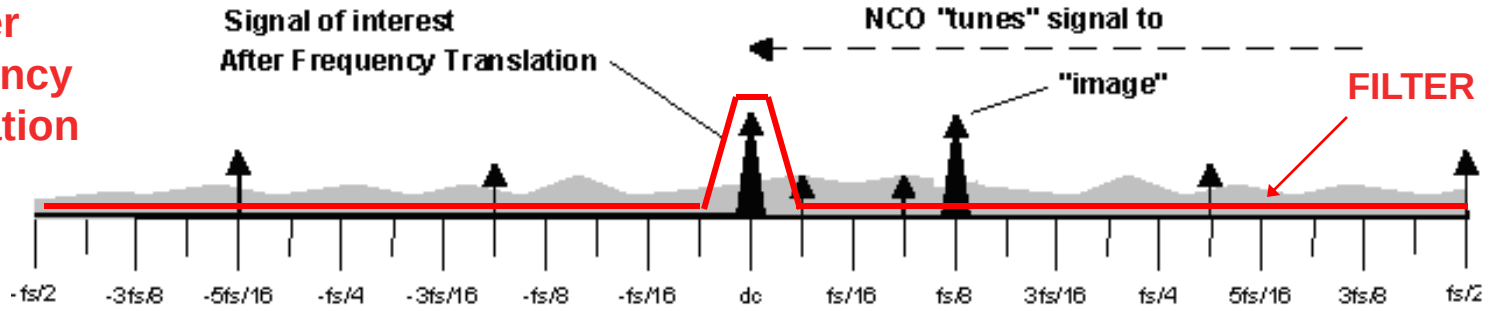
Frequency Translation + Low Pass Filter = Band pass filter

Real Input to the part



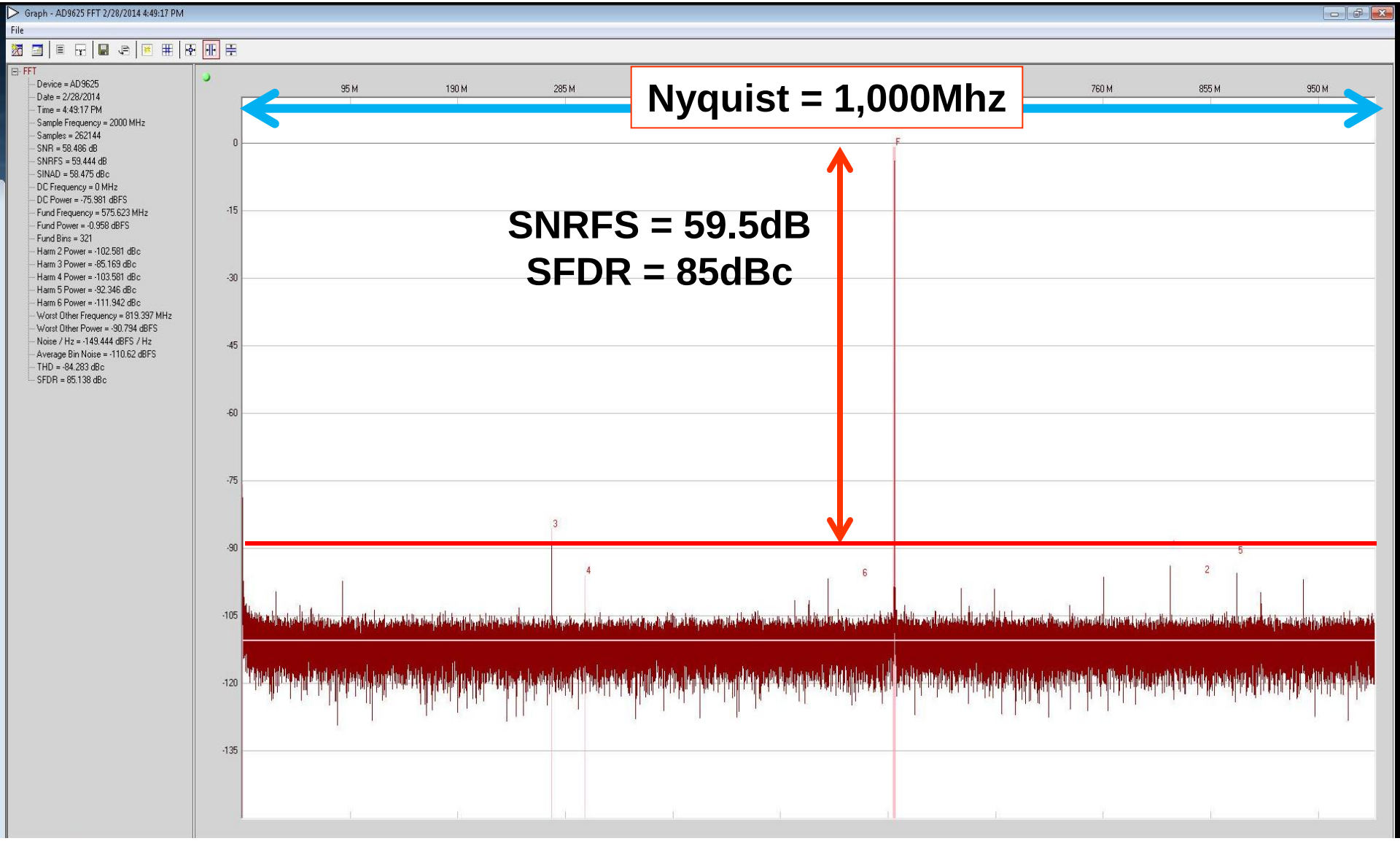
Wideband Input Spectrum (e.g. 30MHz from Highspeed ADC)

After frequency translation

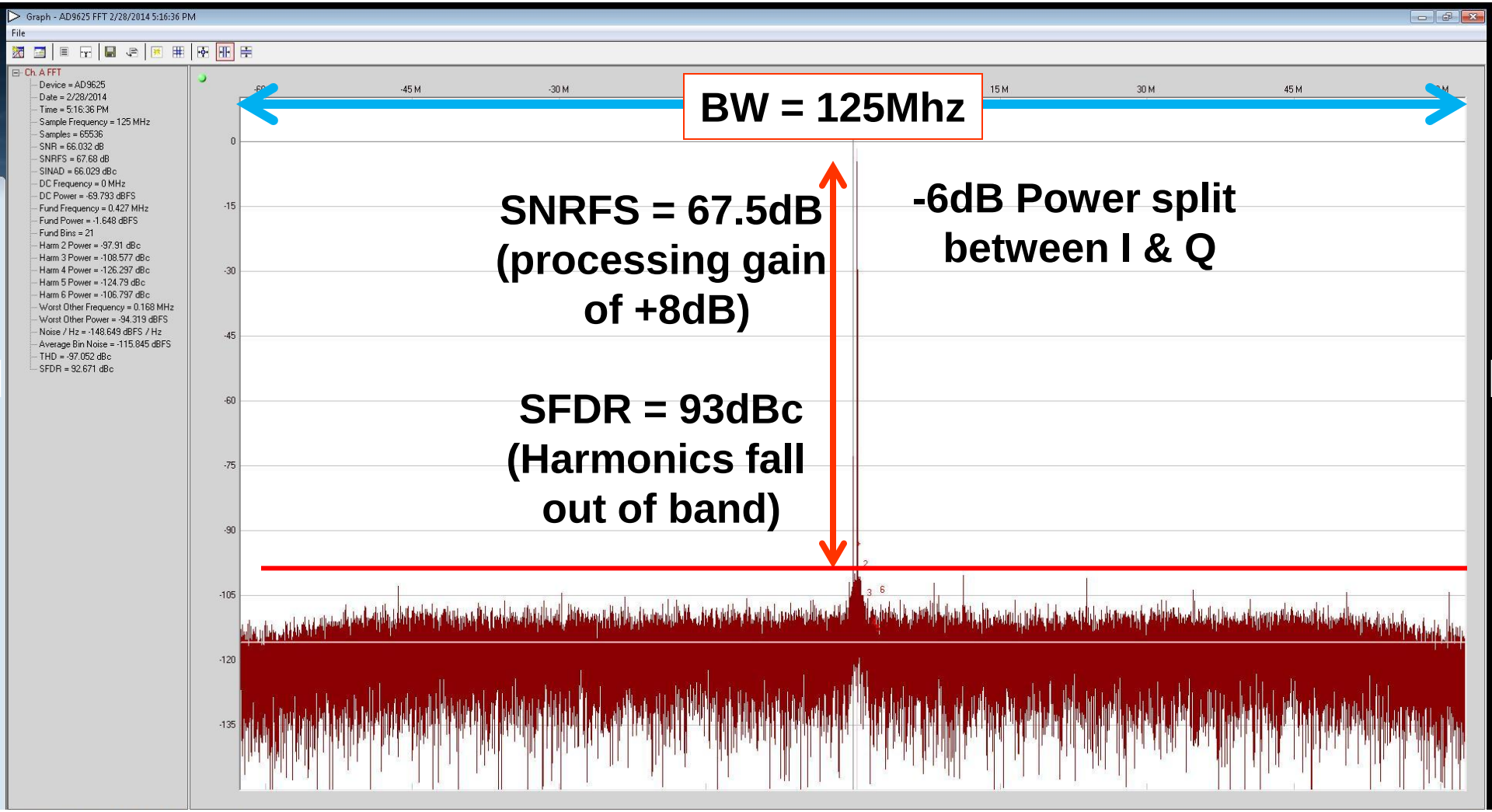


Frequency Translation (e.g. single 1MHz channel tuned to baseband)

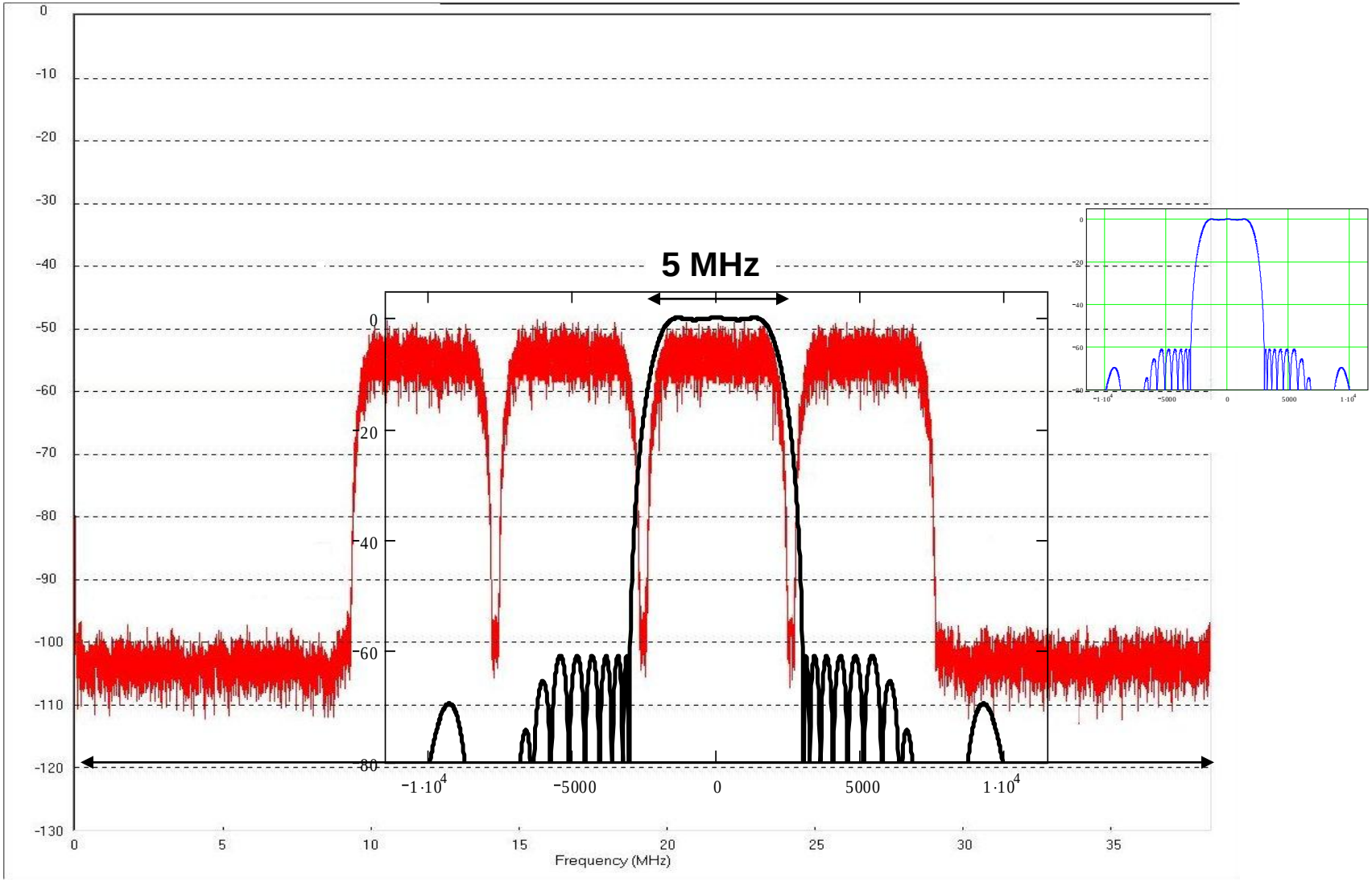
DDC Example – Wideband



DDC Example – Decimate x16, NCO tuned to Fund.



DDC Usage Example



DDC Advantages/Disadvantages

Advantages

- Less number of lanes, ie - fewer pins used
  - Can combine more ADCs into fewer FPGAs
- More fabric/resources available in the FPGA
- Lower cost FPGA possibly
- Multiple DDCs/Bands on ADC
- DDC on ADC may be lower power

Disadvantages

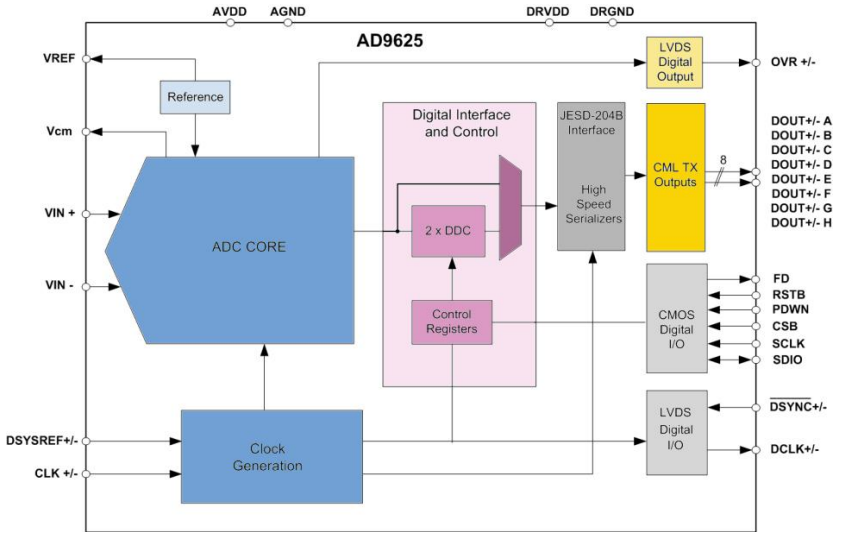
- Fixed tap filter co-efficients
- SPI register writes for NCO tuning

AD9625: 12-Bit, 2.5GSPS ADC

- 12-bit 2.5 Gsps ADC with no missing codes
- SFDR > 75dBc with Ain up to 1.8GHz
- SNR = 56 dBFS with Ain up to 1.8GHz
- Noise Floor = -150dBFS/Hz
- 2 Powerful Digital Down Converter (DDC) blocks. Each block contains:
  - A 10 bit NCO with 2.44MHz tuning resolution.
  - A digital mixer for message band placement.
  - Selectable bandwidth/decimation rate filter bands:
    - High BW: +/-120MHz (/8)
    - Low BW: +/- 60MHz (/16)
- 8-lane JESD204B output format w/ embedded clock (6.25Gbps)
- Serial Port Control (SPI):
  - Flexible digital output modes
  - Built-in selectable digital test pattern generation
  - Configuration of foreground, background calibrations
- Package: 196-ball CSPBGA, 12x12mm

Key Benefit

- IF receiver-level performance brought to giga-sample speeds.



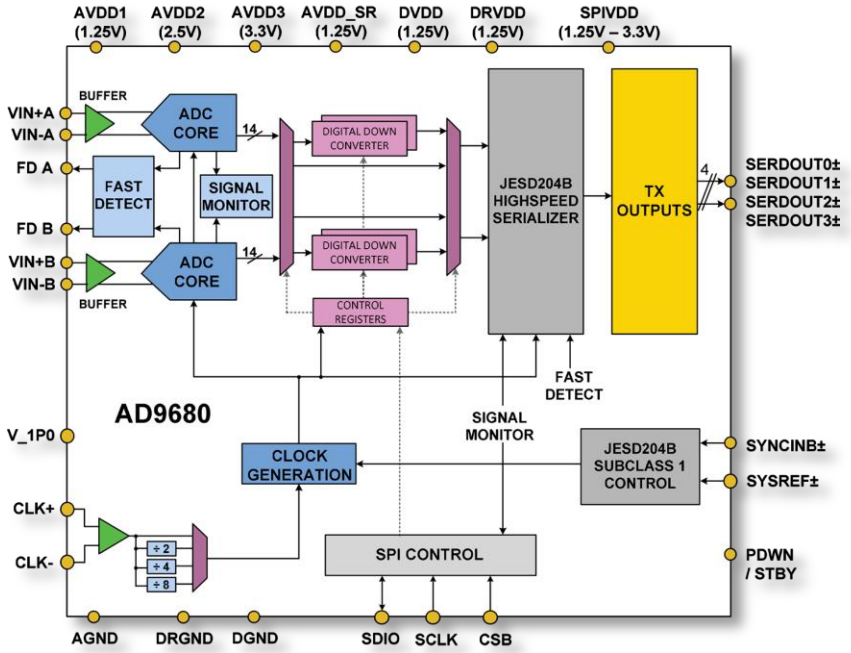
Temp	Package
-40° C - +85° C*	144mm² CS-BGA

Samples	Final Release
Now	July 2014

AD9680: Dual 14-Bit, 1 GSPS ADC

- JESD204B (subclass 1) coded serial digital outputs
- 1.65W total power per channel at 1.25GSPS
  - *Noise Density = -154dBFs/Hz*
  - *SFDR = 85 dBc at 340MHz Ain (1000Msps)*
  - *SFDR = 78 dBc at 1000MHz Ain (1000Msps)*
  - *ENOB = 10.9 bits*
- +/-0.5 LSB DNL, +/-1.0 LSB INL
- Voltage supplies : 1.2V and 2.5V/3.3V
- Flexible Input range: 1.2Vp-p to 2Vp-p (1.6Vp-p nominal)
- 2GHz analog input bandwidth
- 95dB channel isolation/crosstalk
- Amplitude detection for efficient AGC implementation
- Two Integrated wide band digital down converters (DDC) per channel
  - 12-bit complex NCO
  - 4 cascaded half band filters
- Differential Clock input and divider
- Serial Port Control
  - Dither for improved signal linearity
  - Energy-saving power-down modes
- 12-bit variant: AD9234 (500MSPS/1000MSPS)
- LVDS Variant: AD9684 (500MSPS)
- Exportable IF receiver : AD6674

Key Benefit
High performance over wide bandwidth



Temp	Package
-40° C - +85° C	64-LFCSP; Pb Free

Sampling	Final Release
Now	May 2014

Driving GSPS ADCs: Amplifier vs. Transformer

List of critical system parameters and which performs best….

Parameter	Usual preference
◆Bandwidth	Transformer
◆Gain	Amplifier
◆Passband flatness	Amplifier
◆Power requirement	Transformer
◆Noise	Transformer
◆DC vs. AC coupling	Amplifier (dc level preservation)
	Transformer (dc isolation)

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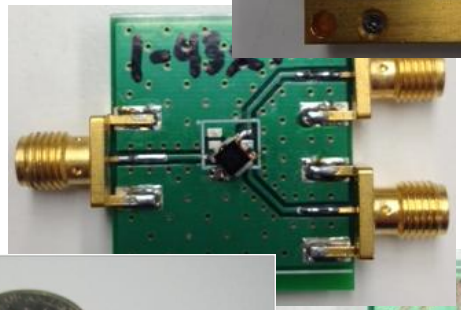
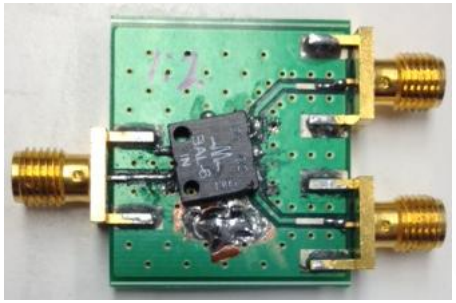
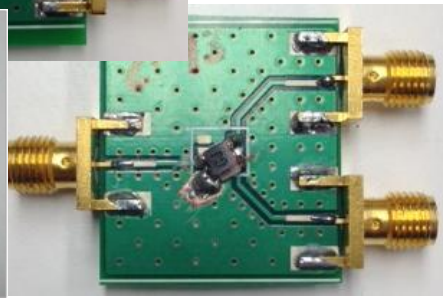
WB 1:1 Z Ratio XFMR/Balun Types

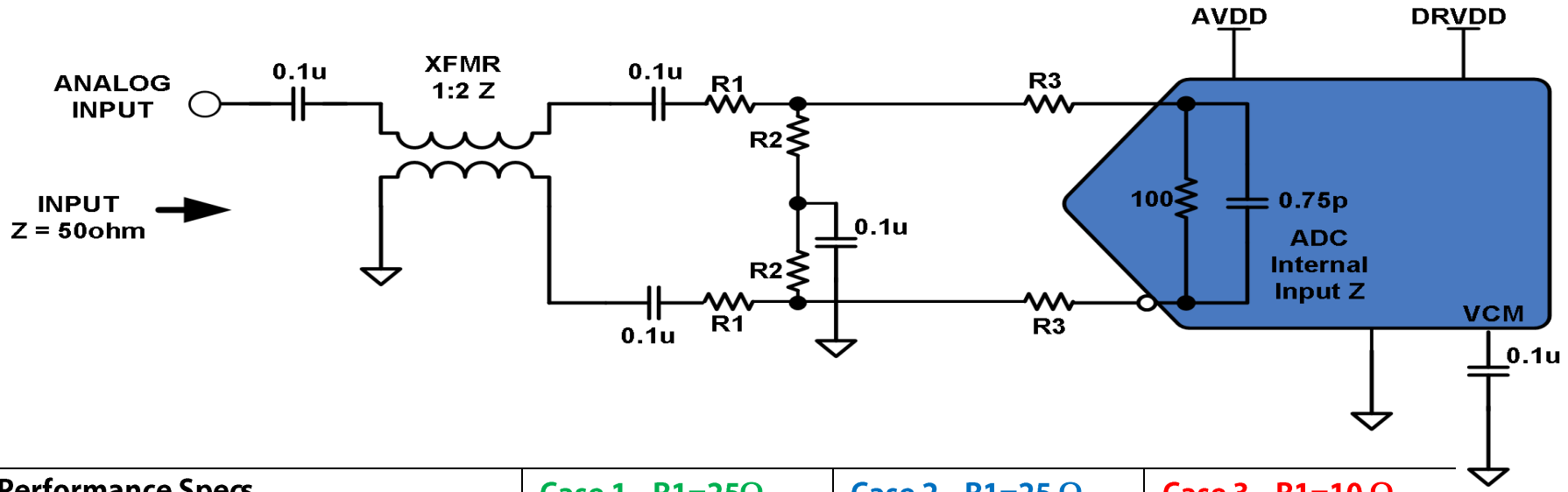
MFG / Model Number	BW	Cost (USD)
Hyperlabs / HL9402/3	20GHz	$2400/$1000
Picosecond / 5310A	6.5GHz	$1200
Marki uWave / BAL-0006SM	6GHz	$124
MiniCircuits / TCM1-83X+	8GHz	<$10
MiniCircuits / TCM1-63AX+	6GHz	<$10
MiniCircuits / TCM1-43X+	4GHz	<$10
Anaren / B0322J5050A00	2.2GHz	<$5





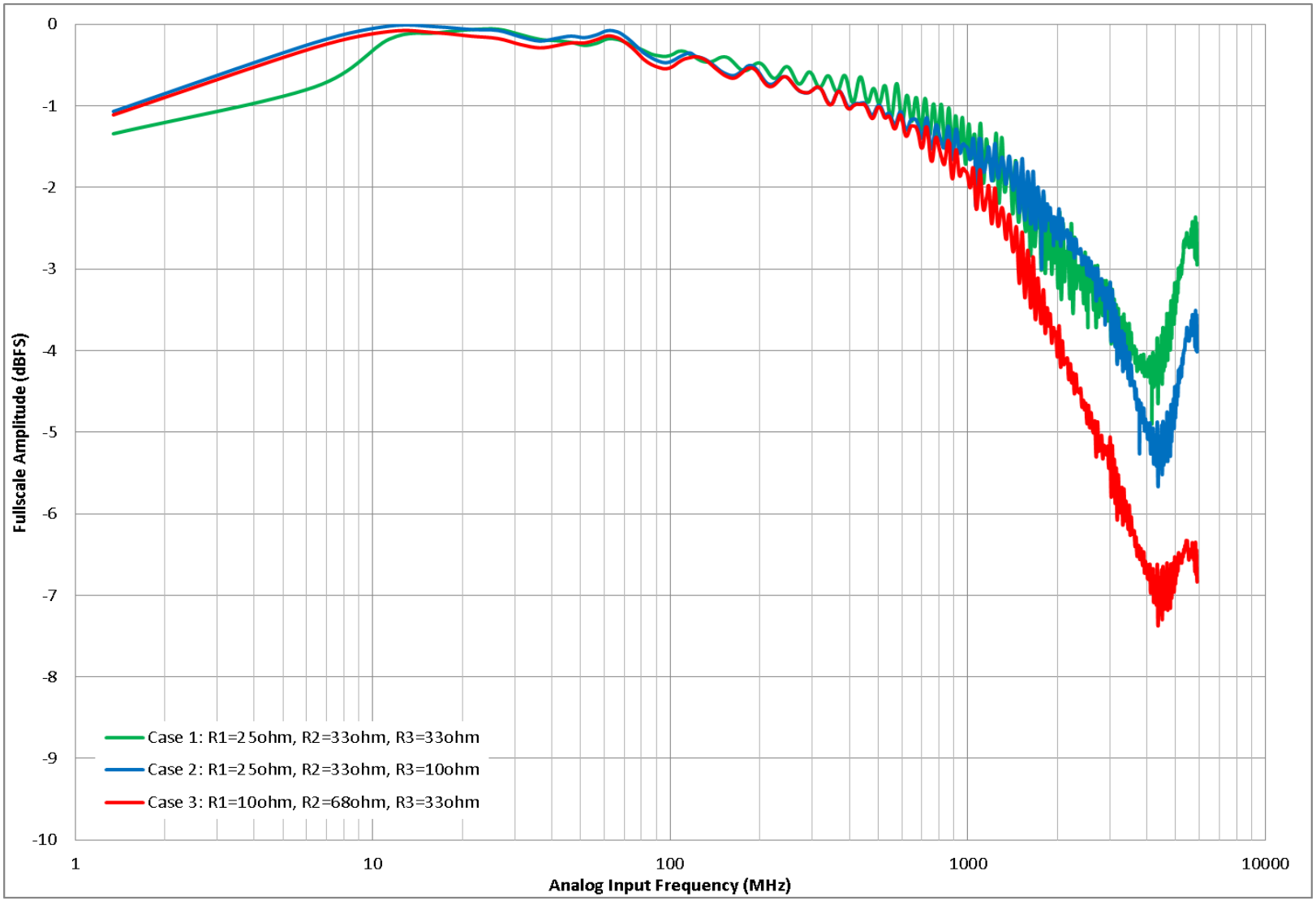


Generic Passive Frontend "Matching" Exercise



Performance Specs	Case 1 – R1=25Ω, R2=33Ω, R3=33Ω	Case 2 – R1=25 Ω, R2=33 Ω, R3=10 Ω	Case 3 – R1=10 Ω, R2=68 Ω, R3=33Ω
Bandwidth (-3dB)	3169 MHz	3169 MHz	1996 MHz
Pass-Band Flatness (2GHz Ripple)	2.34 dB	2.01 dB	3.07 dB
SNRFS @ 1000 MHz	58.3 dBFS	58.0 dBFS	58.2 dBFS
SFDR @ 1000 MHz	74.5 dBc	74.0 dBc	77.5 dBc
H2/H3 @ 1000 MHz	-74.5 dBc/-83.1 dBc	-77.0 dBc/-74.0 dBc	-77.5 dBc/-85.6 dBc
Input Impedance @ 500MHz	46 Ohms	45.5 Ohms	44.4 Ohms
Input Drive @ 500 MHz	+15.0 dBm	+12.6dBm	+10.7dBm

Bandwidth Matching



Let's Look at the ADA4961: Low Distortion 2.5GHz Diff DGA for Driving GSPS ADCs

FEATURES

High speed
- **–3 dB bandwidth 2.5 GHz**
- **–1 dB bandwidth 1.8 GHz**
- **Slew rate: TBD V/µs**
- **Settling time to 0.1%: TBD ns**
- **Overdrive recovery: TBD ns**

Digitally adjustable gain
- **–6 dB to +15 dB voltage gain**
- **–3 dB to +18 dB power gain**
- **Five-bit parallel or SPI bus gain control with Fast Attack**

IMD3/HD3 distortion
- **IMD3 @ 1GHz: –90 dBc**
- **500Mhz -82dBc HD3**
- **1 Ghz -80dBc HD3**
- **1.5 Ghz -75dBc HD3**

Low noise
- **Noise density RTO: 6.9 nV/√Hz**
- **Noise figure : 5.6dB @ G = +15 dB**

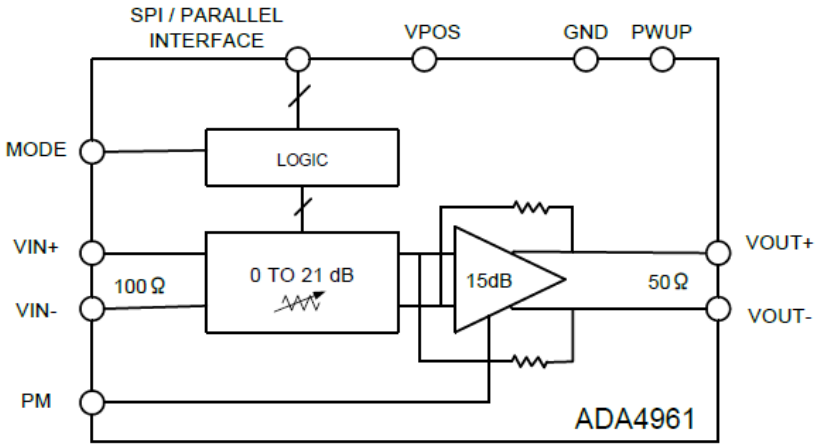
Differential impedances: 100 Ω input, 50 Ω output

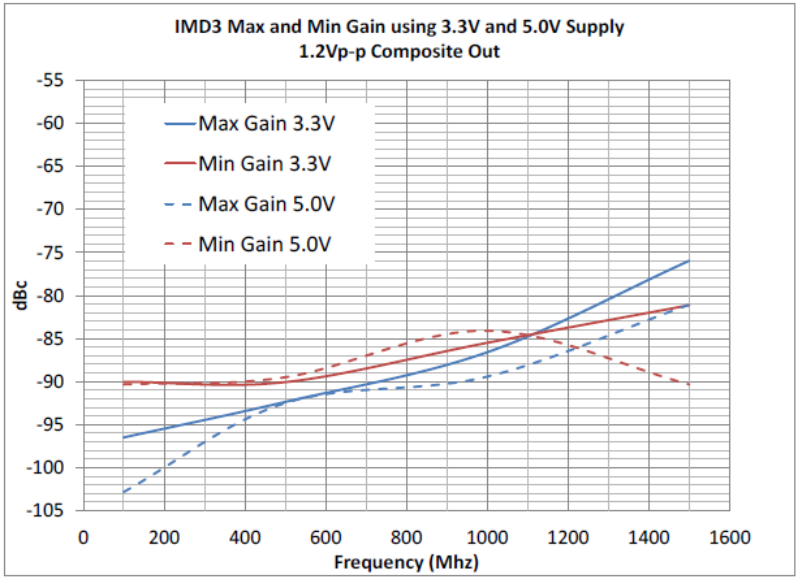
Low power mode operation

Power-down control

Single 3.3V or 5V supply operation

Available in 24-Lead 4 x 4 mm LFSCP package





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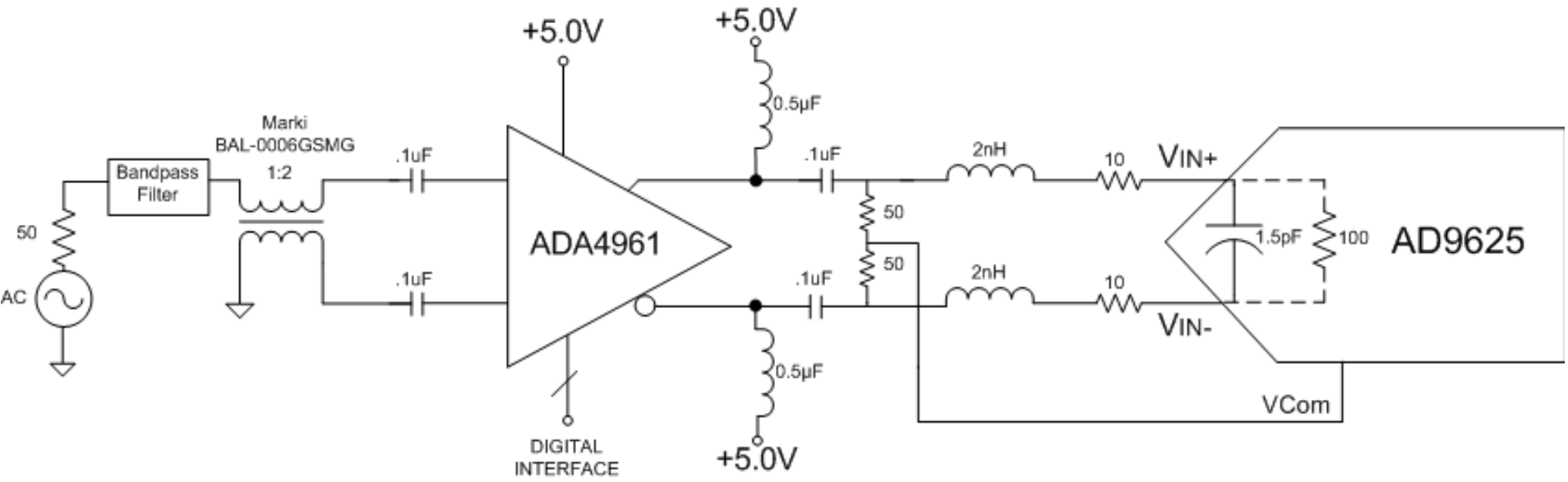
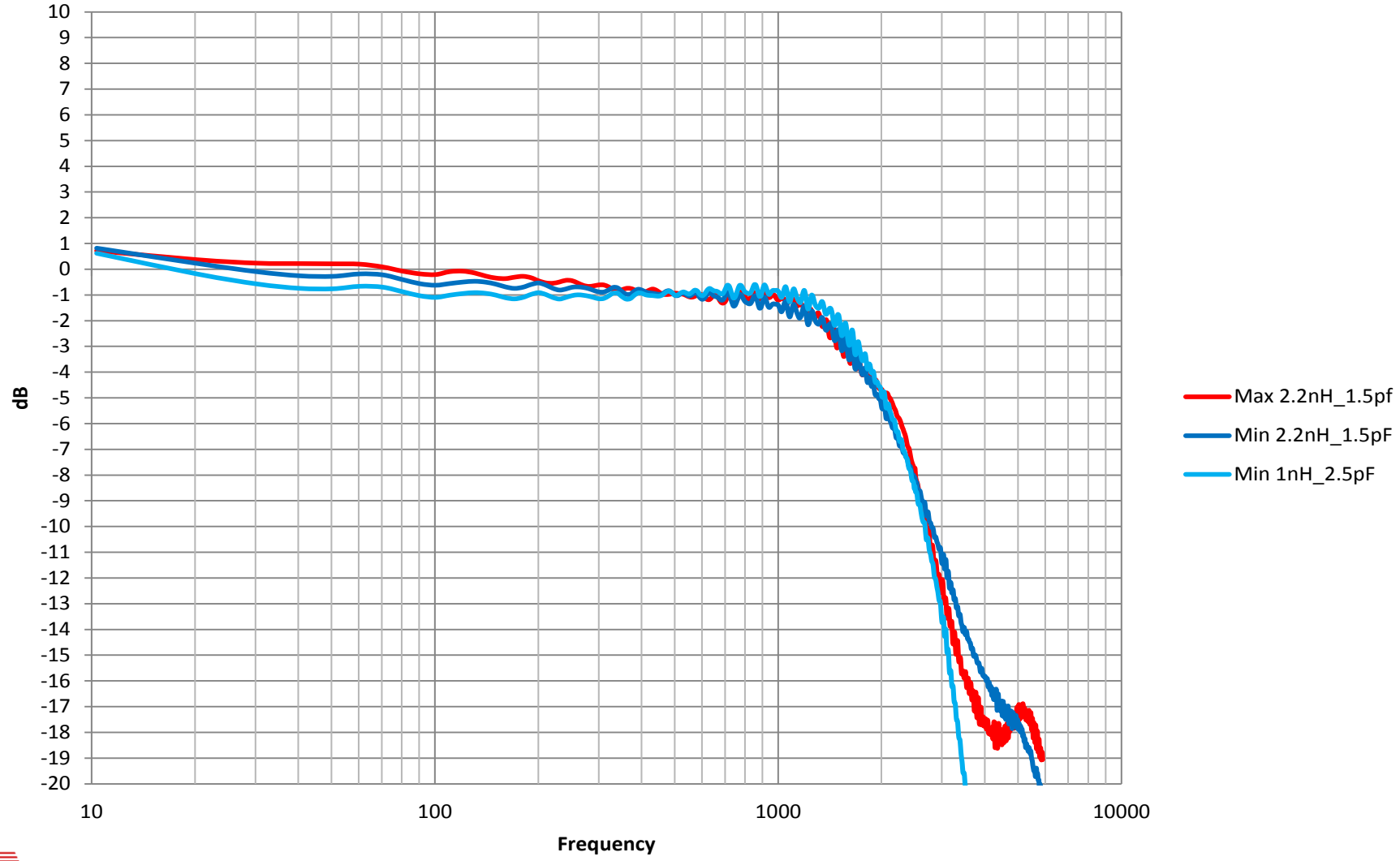
Amp & ADC FE Block Diagram

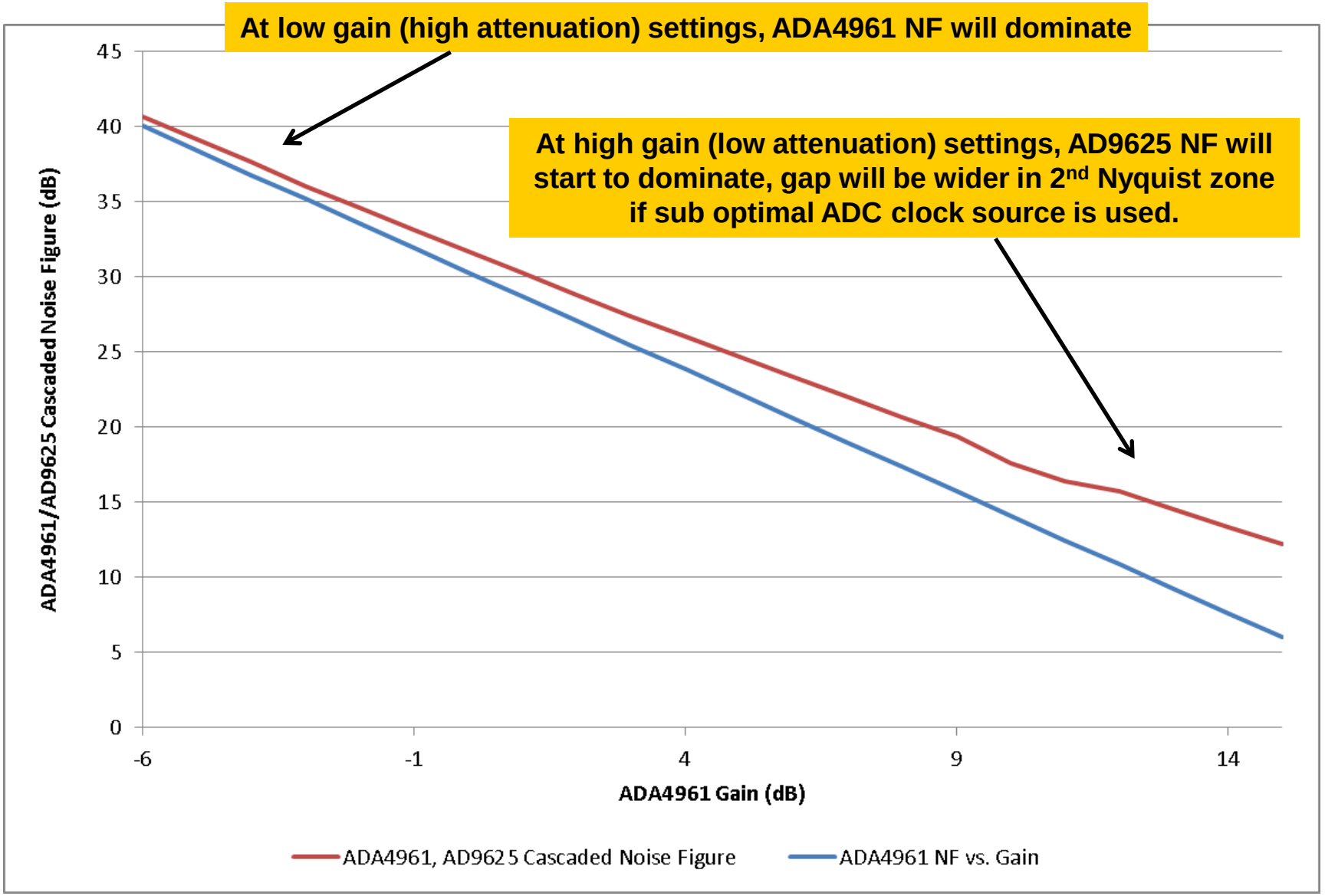


Cascaded ADA4961 + Filter + AD9625

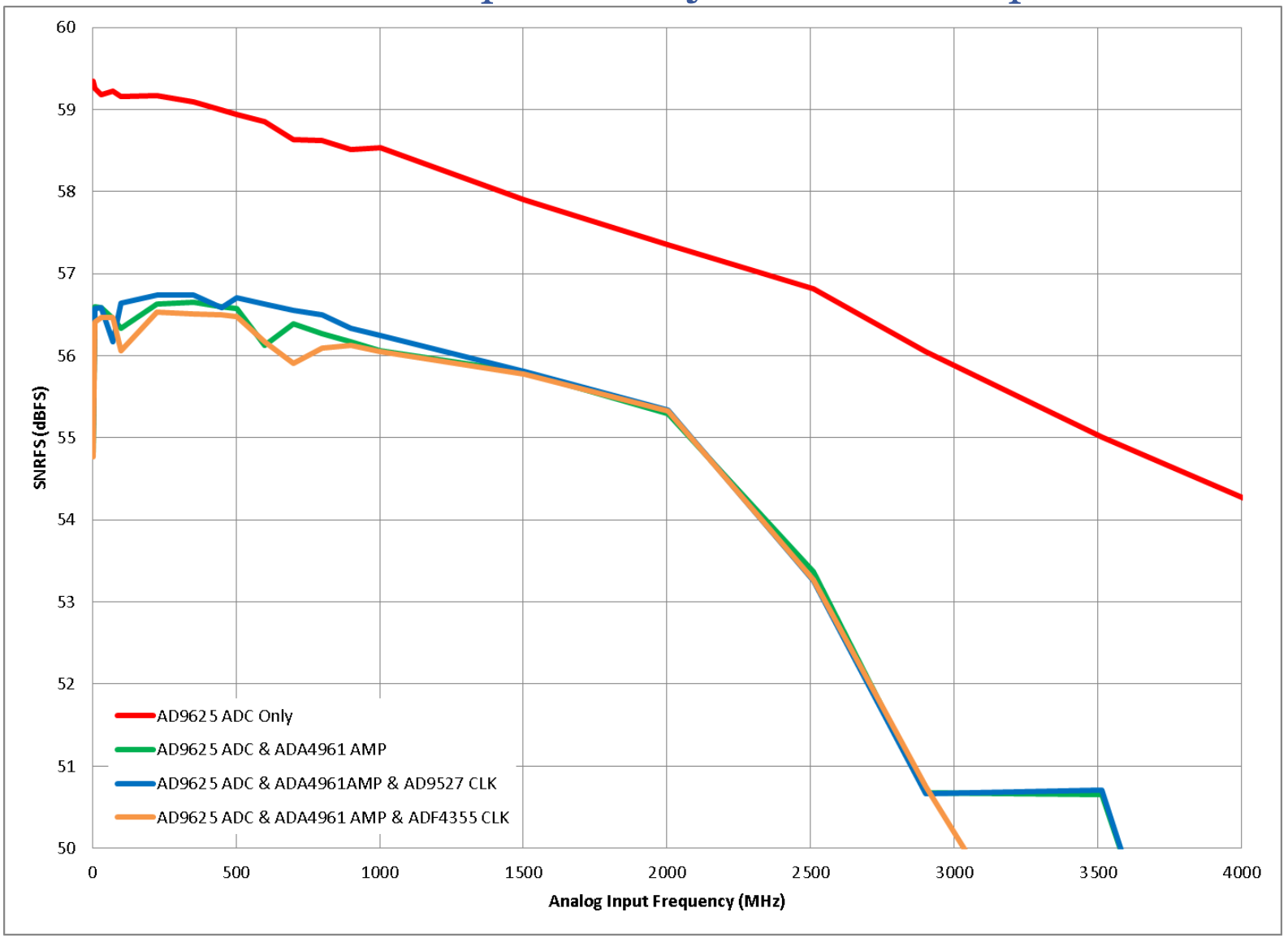
Bode: Max & Min Gains: Two Filters



AD9625 + ADA4961 Cascaded Noise Figure



SNRFS – Complete System Comparison

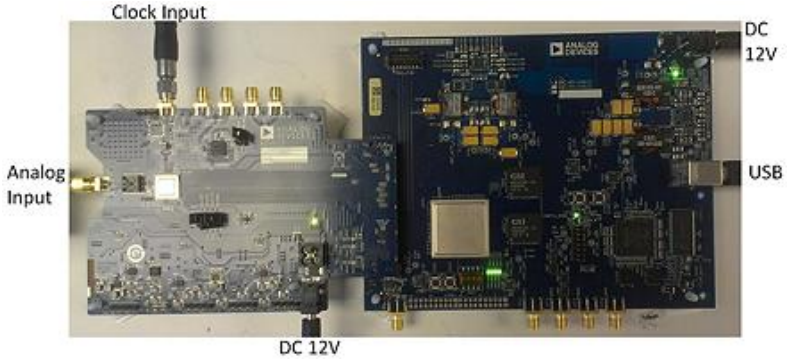


Summary

- GSPS converters offer ease of use in theory however, achieving bandwidth in the +1GHz range can pose new challenges to designing a frontend network.
- Phase imbalance is important when specifying a balun yielding optimal second order linearity.
- There are offerings in driver technologies as well. Using the ADA4961 as a good example which provides high BW and low NF when cascaded with the AD9625.
- Finally, keep choose your clocking device for the converter wisely. Only a low phase noise clocking device, either an active clock generator, VCXO or oscillator will yield the best datasheet performance in your system.

Complete Set of Hardware Support Tools for Designing with GSPS ADCs

- Hardware and Schematics
  - Eval boards – Traditional product performance eval. boards with connection to ADI data capture platform.



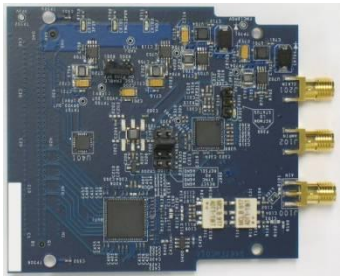
  - New! FMC modules – for rapid prototyping, and development with connection to FPGA development platform.

Signal chain components
On board power
On board clock

Xilinx Eval Cards + ADI FMC Developments

ML605

FMCs



- **Xilinx ML605 / ZC706 + ADI FMCs**
  - ML605 / ZC706
    - Supports 2 FMC interfaces
    - Range of other peripherals inc
      - SFP
      - USB
      - DDR3 SDRAM
  - Provides very capable platform for Mil / Aero system development while custom hardware is developed
    - Enables proof of concept systems to be developed
    - Dual FMCs enable multi-channel synchronization to be demonstrated.
- **Wide acceptance of FMCs**
  - Widely used in Mil / Aero in prototype and final systems
  - VITA 57

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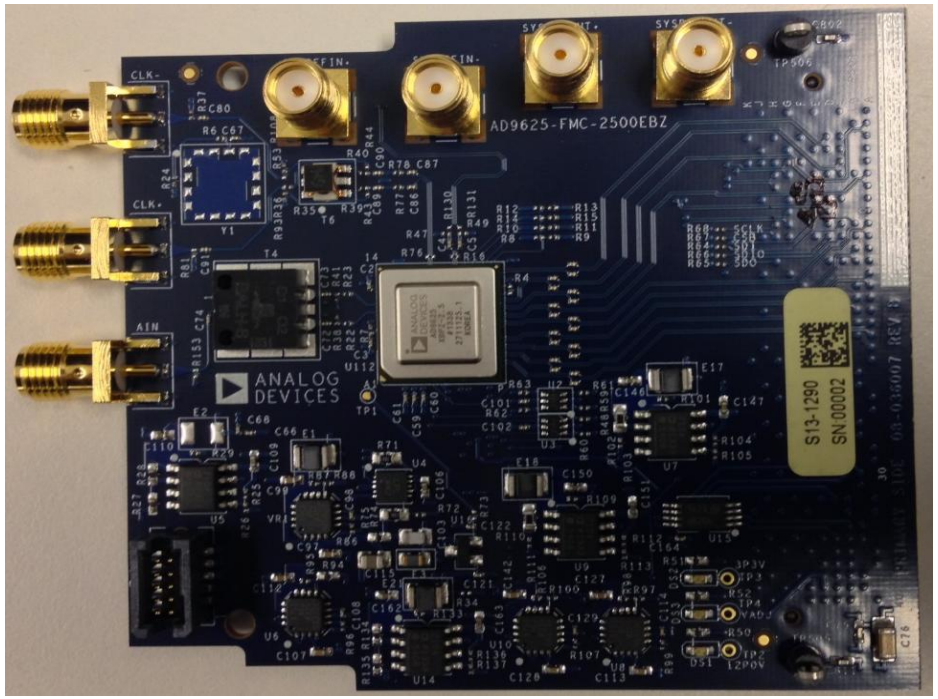
ANALOG DEVICES

AD9625 FMC Module, 12b, 2.5GSPS, Single



- AD-FMCADC2-EBZ
  - Highest in class performance and sampling rate
  - +70dB SFDR / 58dBFS SNR 12bit, 2500MSPS ADC
  - on-board power supply, clock oscillator
  - Synchronization support

AVAILABLE NOW

Validated Multi-board Synchronization to Support Phased Array and Angle of Arrival Detection

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ANALOG DEVICES

AD9625/ADA4961 FMC Module, 12b, 2.5GSPS, Single & Wideband ADC Driver

- Highest in class performance and sampling rate
- +70dB SFDR / 55dBFS SNR 12bit, 2500MSPS ADC
- on-board driver amplifier, power supply, clock oscillator
- Synchronization support

COMING IN SEPTEMBER

Validated Multi-board Synchronization to Support Phased Array and Angle of Arrival Detection

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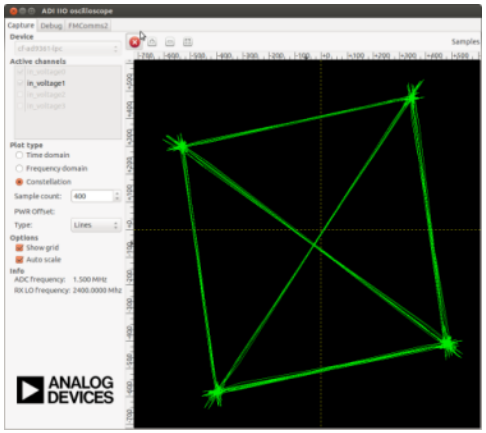
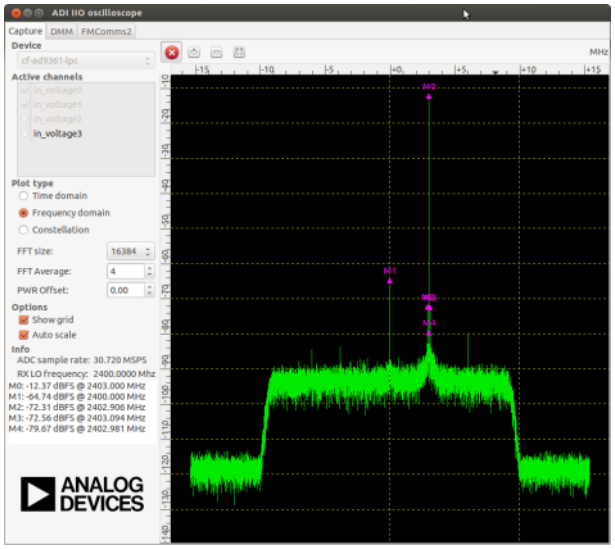
… and Software Tools

- HDL for Xilinx FPGAs:
  - KC705 (Kintex)
  - VC707 (Virtex)
  - ZC706 (Zynq)
  - KC105 (Ultrascale)
- HDL for Altera
  - Coming soon for Arria 10)
- Software
  - Device Drivers
  - User software for Zynq
  - Stream to Visual Analog





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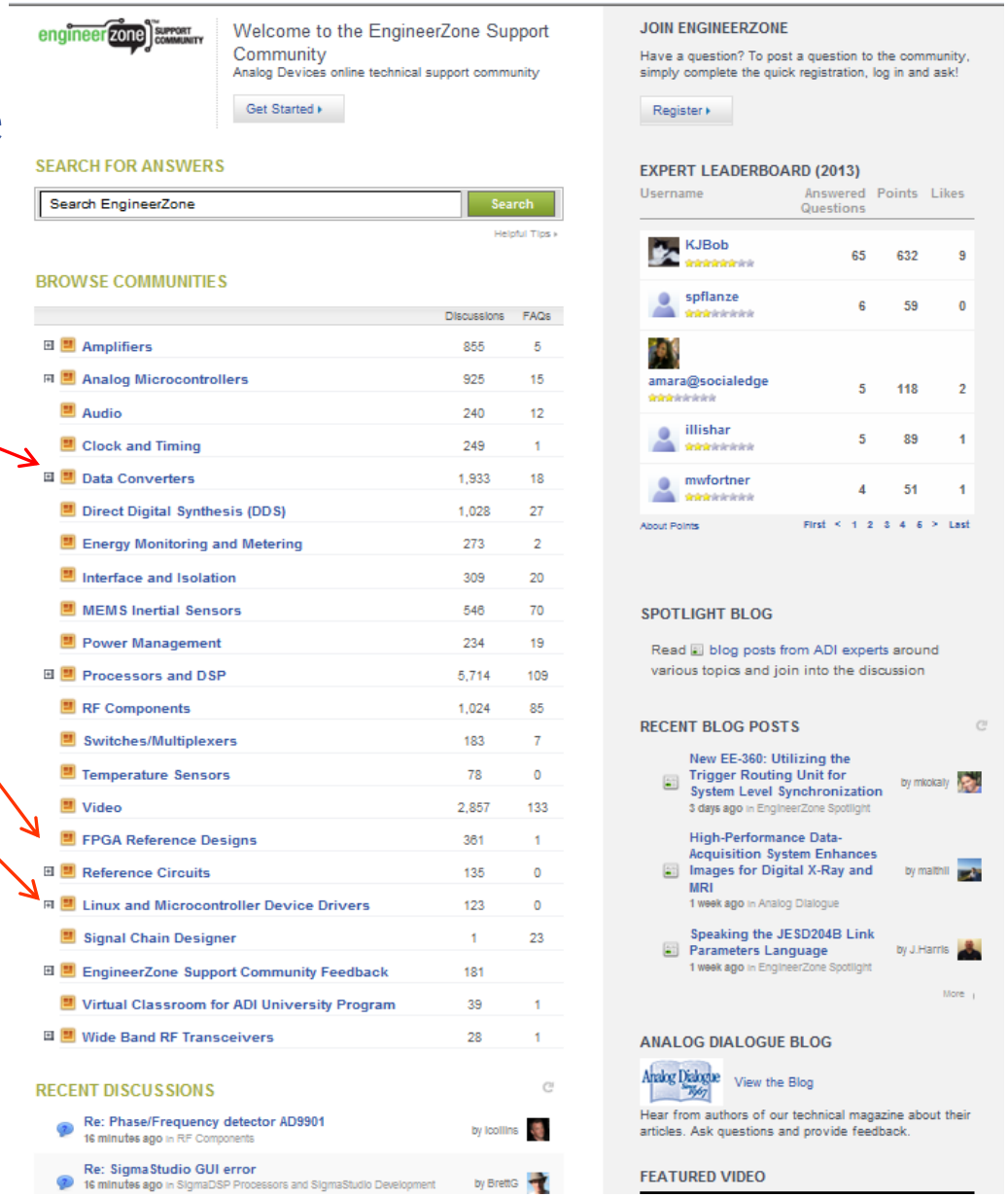
Access to ADI Experts 24x7 On EngineerZone

- Three Very Active Communities
  - High Speed ADCs
    - 416+ discussions
  - FPGA Reference Designs
    - 716 + discussions
  - Linux and No-OS Drivers
    - 257+ discussions
  - Support a variety of questions
  - High Speed converter questions
  - FPGA on FPGA Reference Designs Community
  - Software on Linux Drivers Community



ANALOG DEVICES

Related Design Resources

- www.analog.com/WidebandRF This site has technical articles, videos, additional webcasts, and a complete products listing for ADI's GSPS converters and the AD-FMCADC2-EBZ FMC module.
- www.analog.com/JESD204B This site has technical articles, videos, and webcasts on the JESD204B high-speed data converter serial interface standard. You can also download the "JESD204B Survival Guide".

- Other articles of interest:
  - Understanding Spurious-Free Dynamic Range In Wideband GSPS ADCs
    by Ian Beavers
  - High Speed Converters: An Overview of What, Why, and How
    by Dave Robertson
  - Design Wideband RF Front Ends For GSPS Converters
    by Rob Reeder

Thank You For Watching

View Additional Webcasts at

www.analog.com/webcasts

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