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Technologies and Solutions for Radar System Applications

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AEROSPACE & DEFENSE

ADI 1965 2015

Agenda

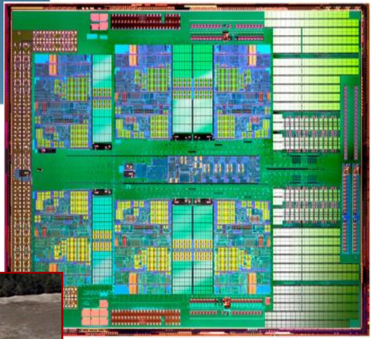
- Overview : ADI & Aerospace and Defense
- An Overview of Radar
  - System configurations and drivers
- Examining the Rx chain
  - Super heterodyne vs Direct Conversion vs RF Sampling
- Challenges & Solutions for Phased Array based systems
  - Integration
  - Multi-channel synchronization
- Summary & ADI Contacts

Overview : ADI & Aerospace & Defense

Analog & Devices and Defense

Supporting Aerospace & Defense for 50 years

- Industries most comprehensive portfolio
  - Supports complete signal chain implementation
    - RF to bits (DC to 110GHz)
    - MEMs for Nav & Stabilization
    - Precision for control & monitoring
- Industry Leading Device Reliability
- Long Product Life Cycle Support
- Advanced packaging and characterization to meet A&D environmental challenges
- Dedicated Aerospace and Defense Segment Team
  - Developing Complete Solutions and Reference Designs reducing system engineering and time to market



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Aerospace and Defense

Market Challenges

- Advanced and evolving threats drives insatiable demand for advanced technology
- Continuous drive for SWaP reduction

Solution Requirements

- Higher frequency of operation
- Operation in contested environments
- Modular and multi-function architectures

ADI Enables

- Complete uWave and mmWave solutions
- Advanced, novel & customizable architectures
- Increased integration and scalable solutions

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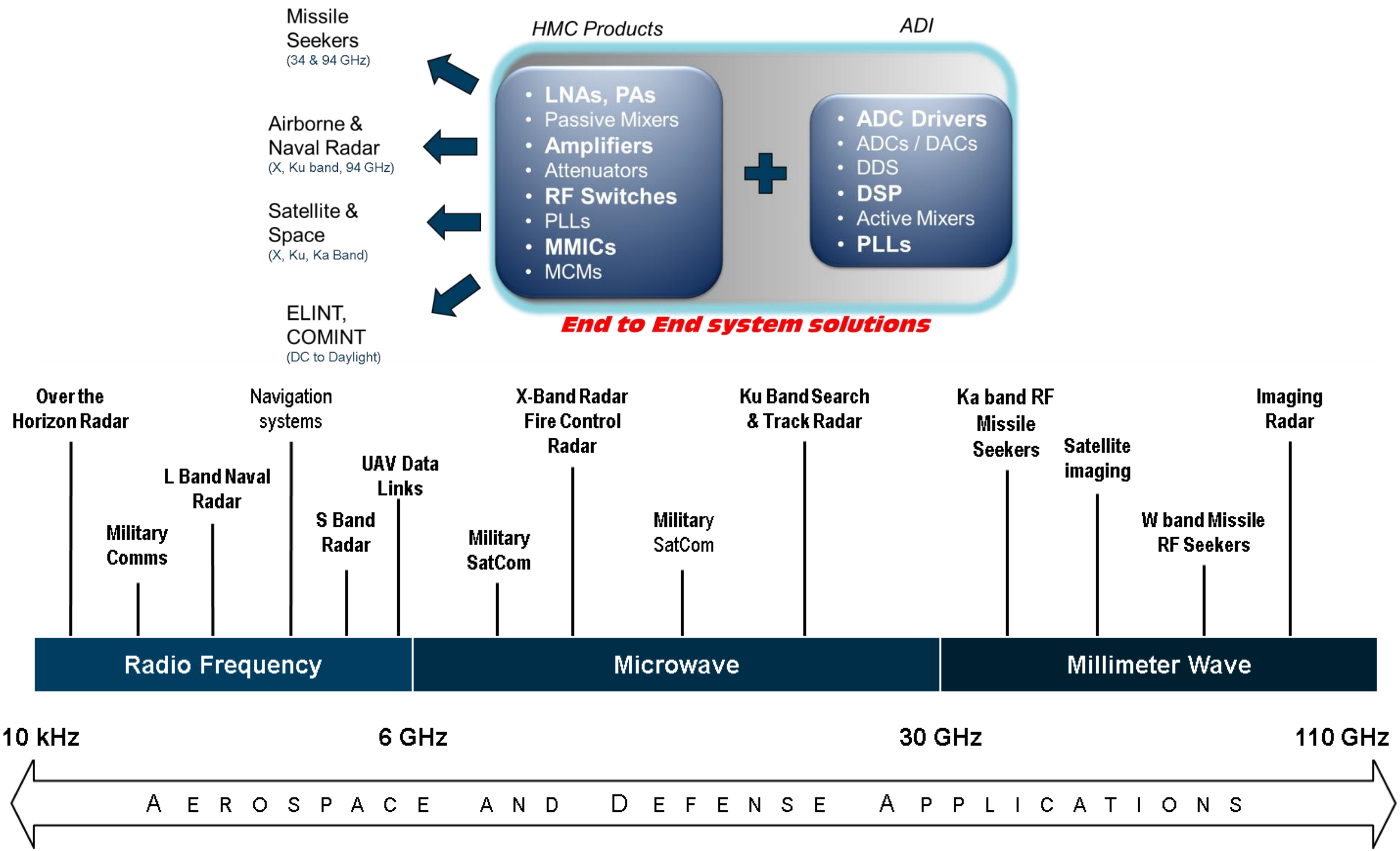
Aerospace and Defense Spectrum Usage

Complete RF to Bits Solutions for the Entire Spectrum



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Aerospace & Defense Technology
Packaging & High Reliability

Standard Products

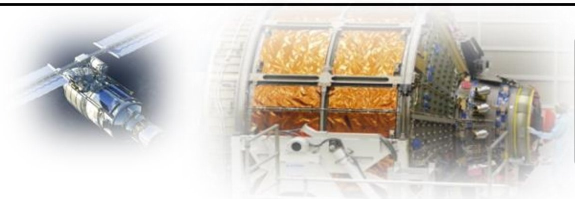
- Designed for higher performance, mission critical systems
- Increased Temperature Range
- Mitigation of Tin Whiskering

Baseline Industrial ADI Devices

-N Devices
- NiPdAu lead finish

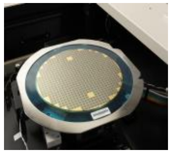
Enhanced Products
- Extended Temperature ranges
  Typically -55 to +125C
- NiPdAu Lead Finish

Class S Devices & Space Portfolio



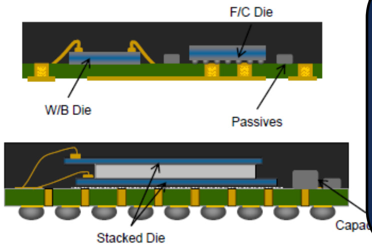
- ADI MIL-PRF-38535 QML "V" certified facilities
- Wafer lot acceptance or SEM
- Wafer lot traceability
- Hot solder dip lead finish - MIL-PRF-38535

Known Good Die

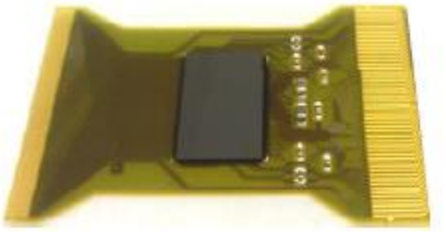


- Supporting custom developments and reduced Size Weight and Power
- Utilized for SiP Developments
- 100% Guaranteed over specified temp range

Integrated Modules & System in Package



- Supporting custom developments and reduced Size Weight and Power
- Flex and Rigid Integration
- Integrated Passive Devices



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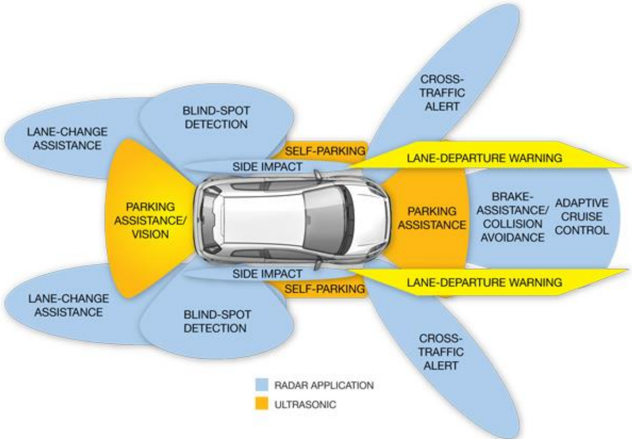
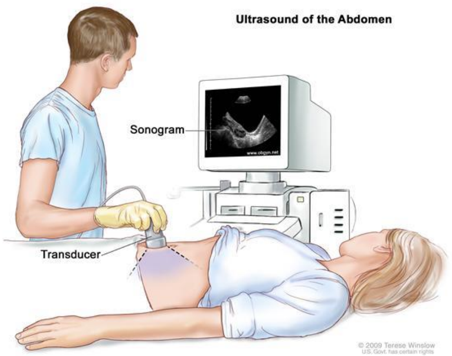
Radar Overview

Radar Applications

- Radar, originally developed during the WWII, has myriad of applications today:
  - Defense
  - Civilian – Air Traffic Control
  - Automotive
  - Derivative technology: Ultrasound in health and industrial applications





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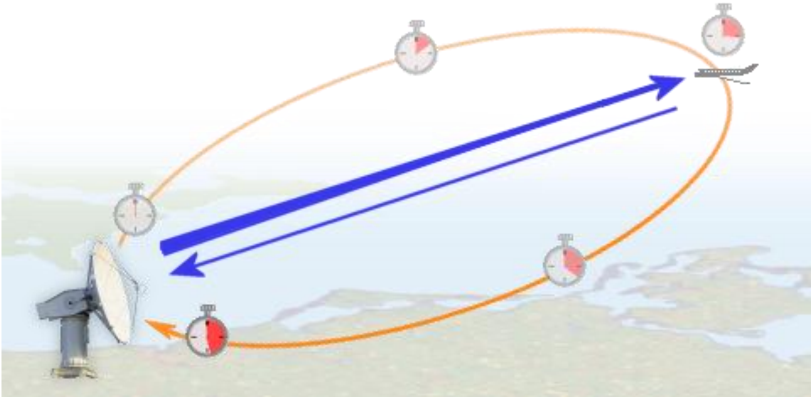
Radar – Principle of Operation

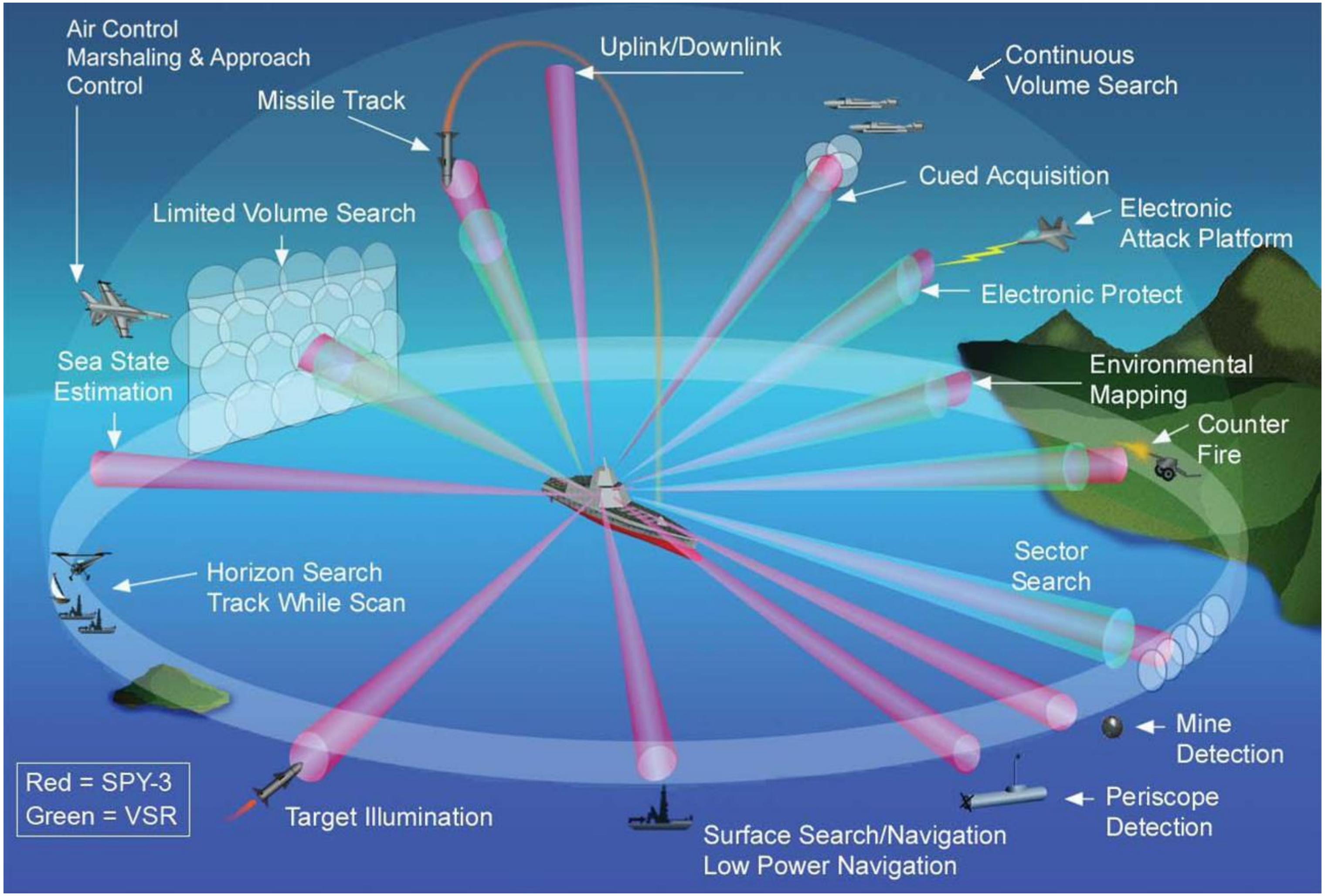
- Transmits an electromagnetic signal modulated with particular type of waveform. (modulation depends on requirements of application)
- Signal is 'reflected' from target
- Reflected signal is detected by radar receiver and analyzed to extract desired information (Distance, bearing, angular velocity)



- **Distance** can be determined by measuring the time difference between transmission and reception
- **Angle** (or relative bearing) can be determined by measuring the angle of arrival (AOA) of the signal (usually by highly directive antenna)
- If there is a radial component of **relative velocity** between radar and target it can be determined from the *Doppler Shift* of the carrier

Most of Defense Radar applications are in the L (1-2GHz), S (2-4GHz), C (4-8GHz), X (8-12GHz) and Ku (12-18GHz) bands.

Multifunction Radar Drive System Performance



Key Radar System Performance Parameter: Range

$$\text{Max. Range} = R_{max.} = \left[\frac{E_t * \text{Gain} * \lambda^2}{(4\pi)^3 * L * kT * F_r * D_o} * \sigma_t \right]^{1/4}$$

Transmitted Energy (E_t), Wavelength (λ), Loss (L), Receiver Noise Figure (F_r), Target Cross-section (σ_t)

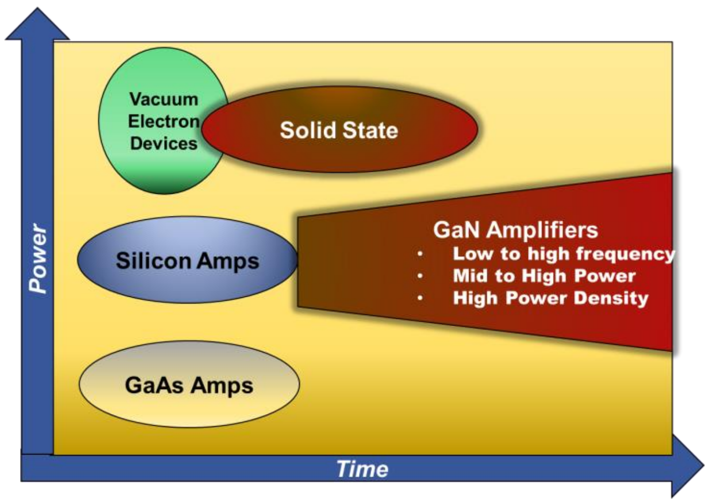
Where, D_o = Detectability Factor = $(SNR_{out}) * BW$ (@ Receiver output)

A key objective of a radar system is to have its Rmax. As far as possible - to see things as soon as possible!

Key Radar Technology : Power Amplifiers

Solid State & GaN Amplifiers

GaN



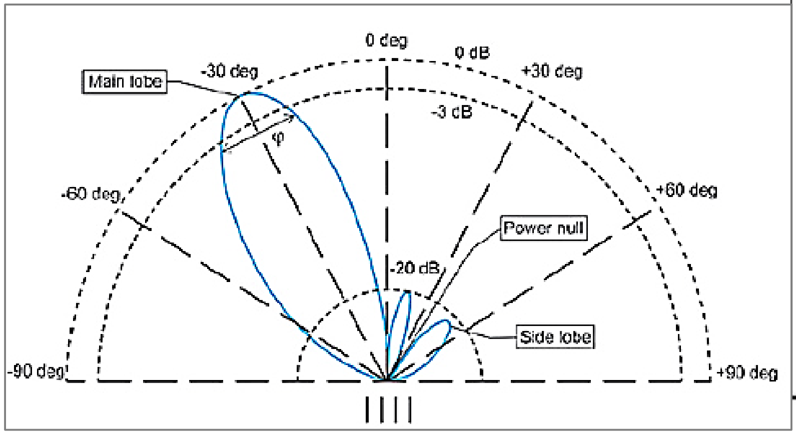
- Radar Systems Migrating from Silicon & GaAs to GaN
- Increased Power Efficiency
- HMC GaN Power Amplifiers up to 25W and from L to Ku band

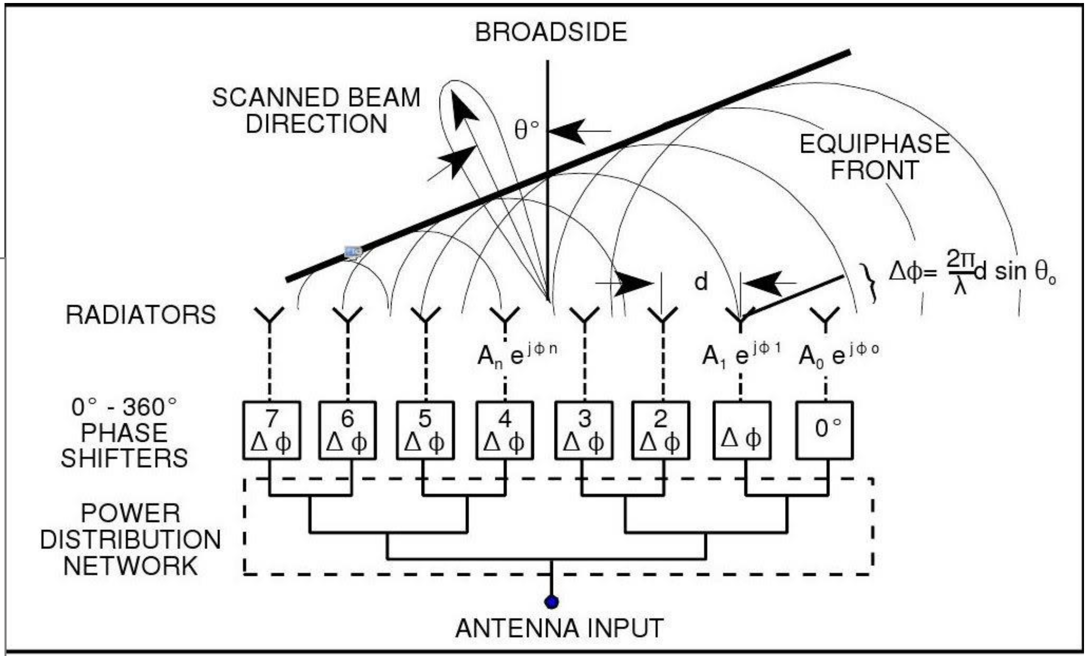
Solid State

- Radar & EW High power, wideband amplifiers
  - Upto 8 kW Solid-state Broadband Power Amplifiers
  - X-band (8-11 GHz)
  - Compact & Efficient

Phased Array Radar Concept

- An array of antenna elements where the relative phase of each element is varied
- Effective radiation pattern is constructively reinforced in the desired direction (main lobe) and suppressed in undesired directions (side lobes)
- Allows the radar to concentrate energy in one place and maintain stealth elsewhere.





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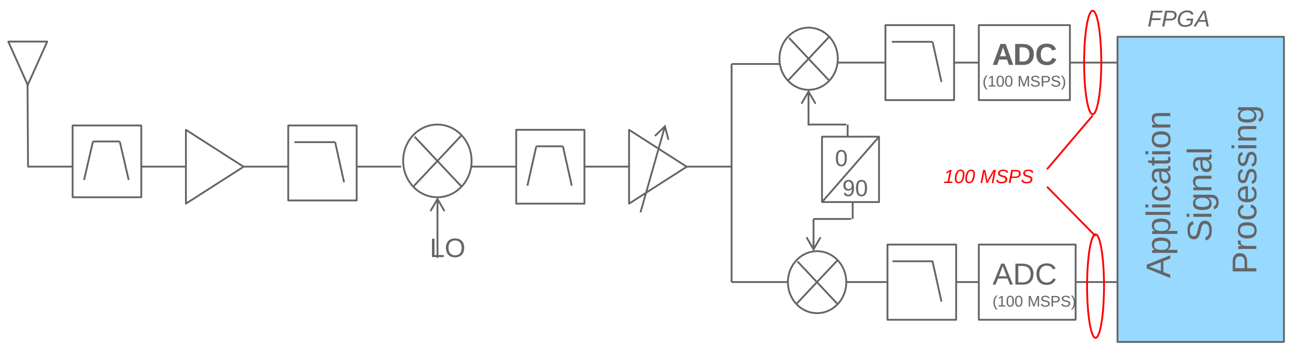
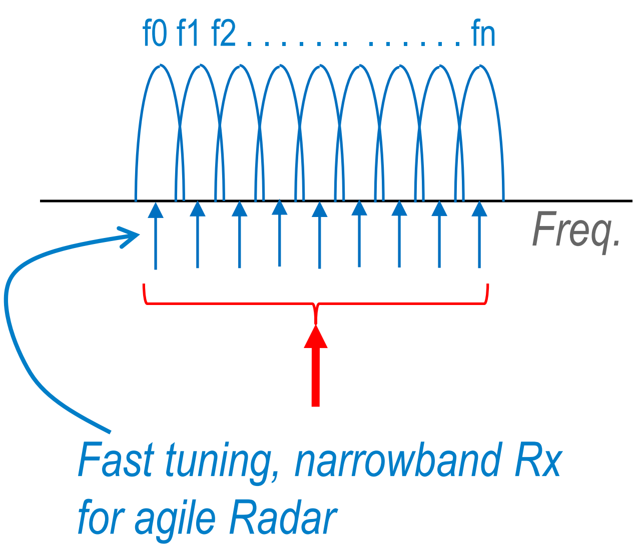
Superheterodyne Architectures

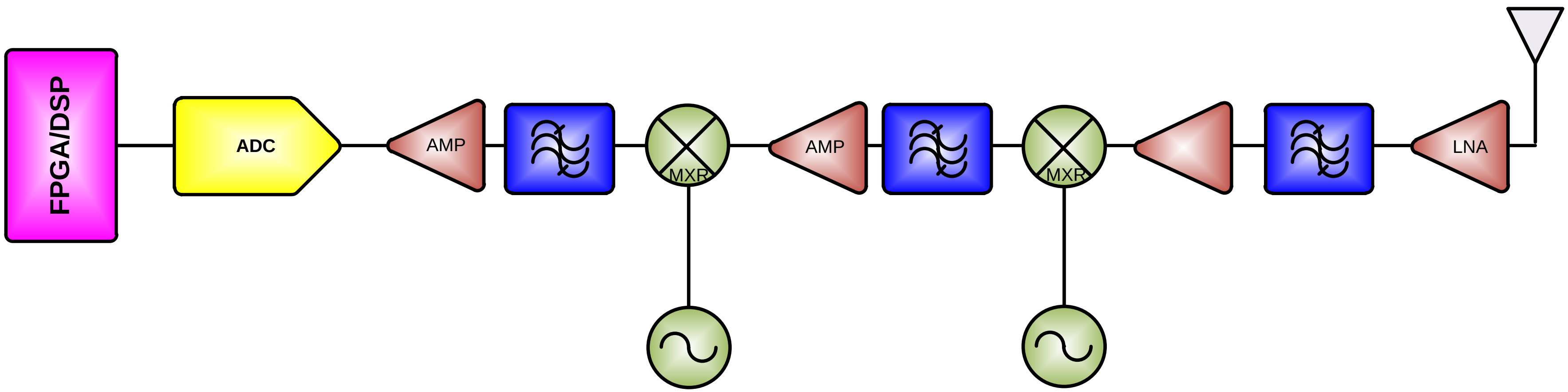
A Closer Look at The Traditional Radar Receiver Architecture



- Typical Super Heterodyne Receiver Architecture
  - Dual Mixing stages to reduce data first to an IF and then to baseband.
    - Second stage could be complex (IQ) or real depending on requirements
  - Application specific functionality implemented inside the FPGA.
    - FPGA functionality may include a Digital Down Conversion (DDC). Assuming digitization rates are <100 MHz, the DDC is relatively simple to implement as minimal parallelization needed.



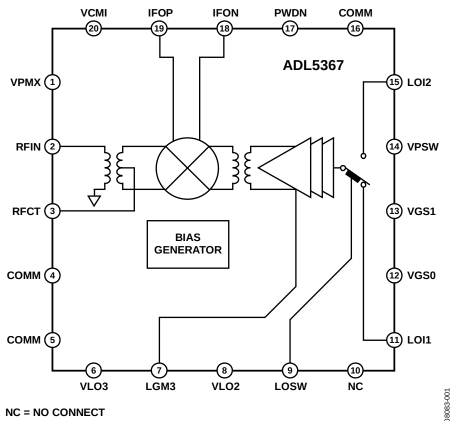
Superheterodyne Rx



- Example: X-band input 8-12 GHz
  - First IF stage : X band to L band
  - Second IF stage : L band to 180 MHz
  - Analog to Digital Conversion at 250 MSPS
    - Supports Rx BW of upto approx. 80 MHz with anti-aliasing filter
- Amplifiers & filters to meet sensitivity and rejection
- L & S band systems use mix up / down approach – frequency planning & filtering
- Analog Pulse Compression potentially included

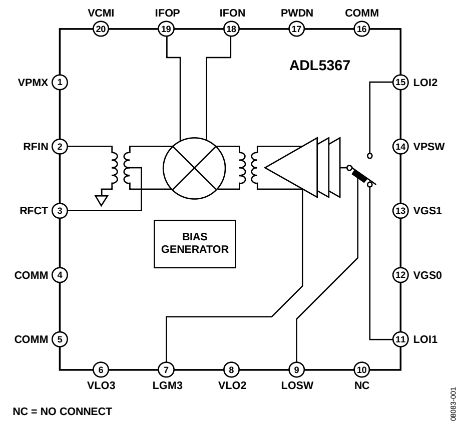
Example Components for X-band Superheterodyne

HMC558



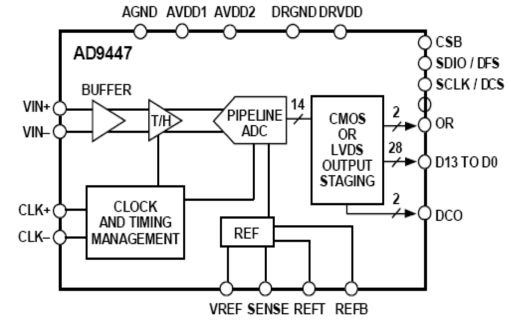
- Double Balanced Mixer
- Features
  - RF input: 5.5 to 12 GHz
  - High LO/RF Isolation: 45 dB
  - Wide IF Bandwidth: DC - 6 GHz
  - Passive Double Balanced Topology
  - Low Conversion Loss: 7 dB
  - Small Size: 0.91 x 0.94 x 0.1 mm

ADL5367



- 0.5 to 1.7 GHz Mixer
- Input IP3: +34 dBm
- Low Conversion Loss: 7.7 dB
- SSB Noise Figure: 8.3 dB
- Small Size: Package: 20-lead LFCSP (5 mm × 5 mm)

AD9467



- SNR = 76.5 / 74 dBFS @ Fin = 125 MHz & 250 MSPS
- ENOB > 14 Bits / 12 Bits
- SFDR = 90 dBc @ Fin = 125 MHz & 250 MSPS (at -6dBFs)
- IF sampling up to 400 MHz
- Excellent Linearity

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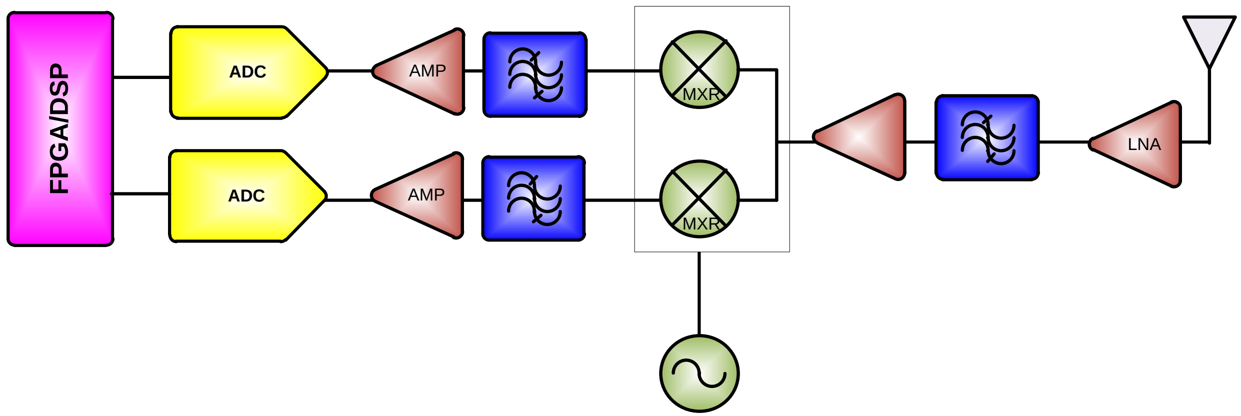
Benefits of IQ demodulation

IQ Demodulation

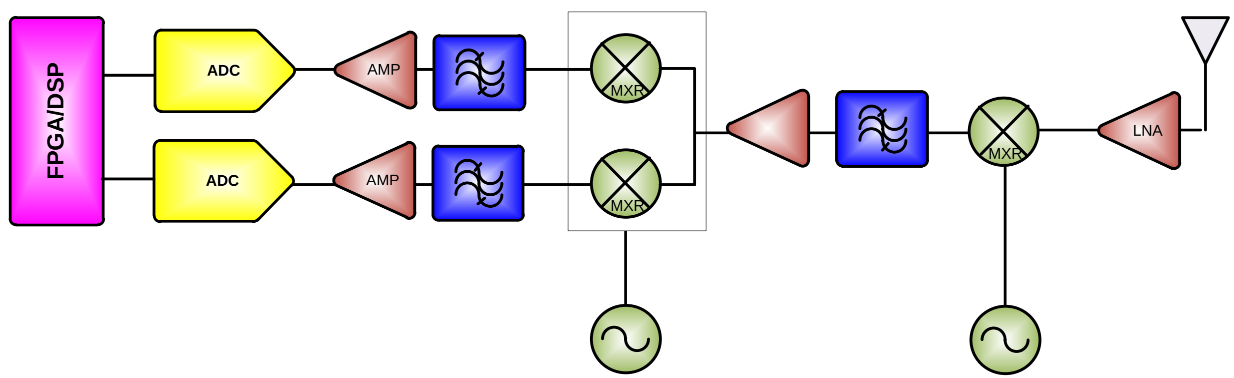
- Direct Conversion for L & S Band
  - IQ demodulator
  - Dual ADC
- Conversion to Baseband
  - Complex BW allows for slower lower power ADCs



IQ demo introduces with Quadrature Error

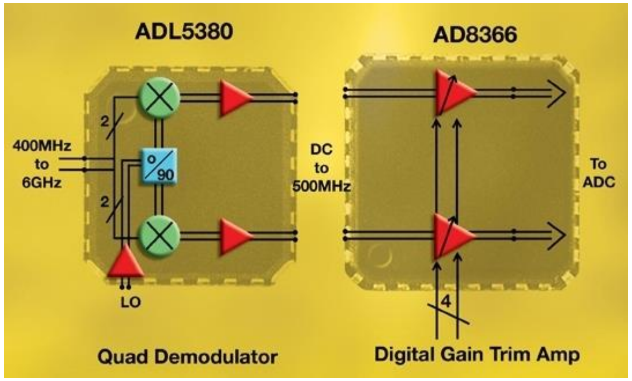
DC Offset, Phase & Gain compensated in Digital Domain

- Second IF conversion to baseband for X-band
  - First IF Mixer – X band to L Band
  - IQ demodulator – L band to Basband
  - Dual ADC



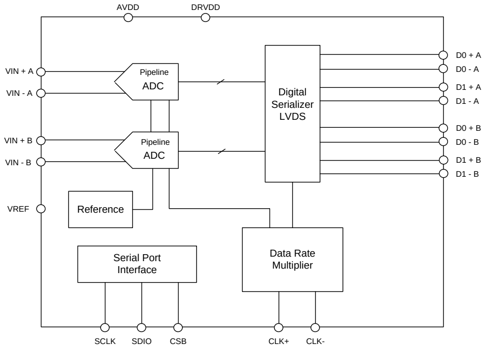
Key Component Examples

ADL5380
400 MHz to 6 GHz Demod



- Frequency Range: 400 MHz to 6 GHz
- Wide LO input range -10 to +5 dBm
- IIP3 +28 dBm, IIP2 +60 dBm @ 2600 MHz
- Input P1dB +12 dBm @ 2600 MHz
- NF 13 dB @ 2500 MHz
- Quadrature demodulation accuracy
  - Phase accuracy 0.2°
  - Amplitude balance 0.07 dB
- Package 24-lead LFCSP

AD9655
16Bit 125Msps Dual ADC



- Dual 125 MSPS 16 bit ADC
- Serial LVDS output interface
- SNR: 77 dBFS @ 70 MHz (2Vpp analog input)
- 80 dBFS @ 70 MHz (2.8Vpp analog input
- Low power: 150mW/ch @ 125 MSPS
- SFDR = 90 dBc @ 70 MHz
- DNL: +/-1,0 LSB, INL: +/-4.5 LSB

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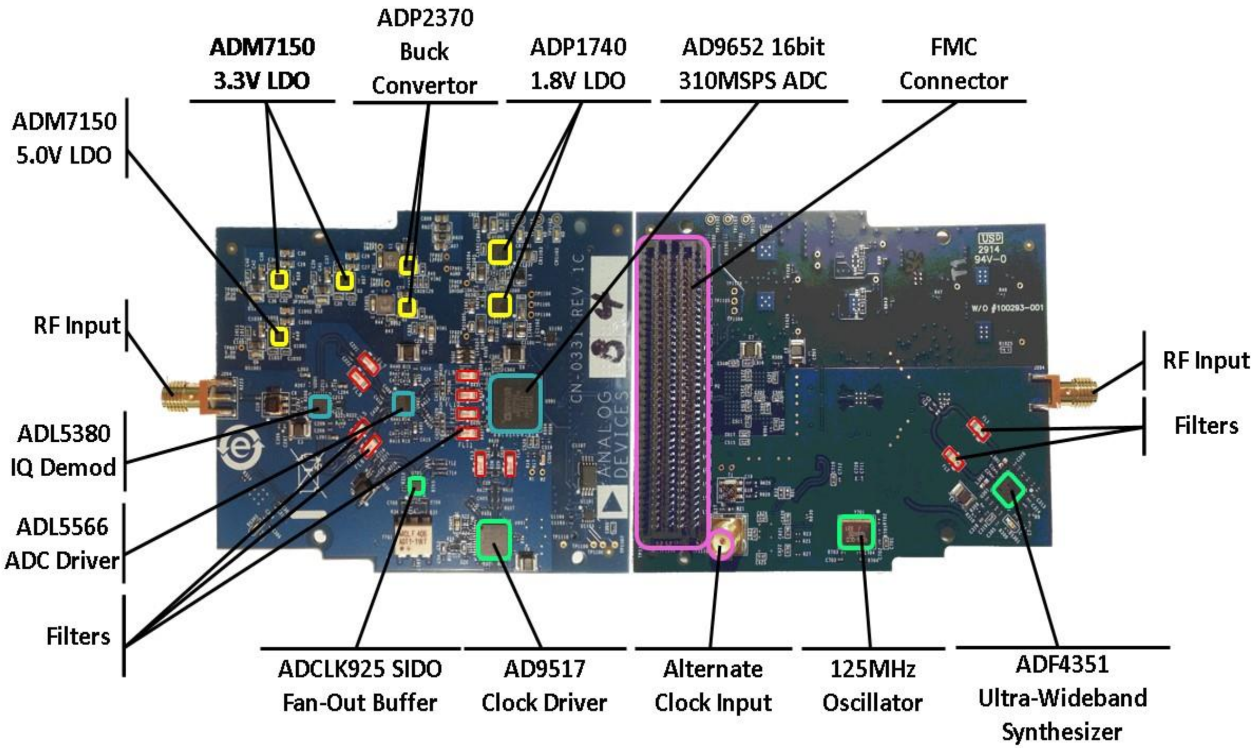
FMCOMMS6 – Direct Conversion L & S Band Receiver

- **L&S Band Direction Conversion Architecture Prototyping Systems**
  - **Image rejection reduces or eliminates the need for an anti-aliasing filter.**
    - Digital error correction is a viable method to remove correlated (non-random) errors.
    - Wafer level process advancements allow for phase and amplitude stability over temperature and voltage.
    - Real-time correlation, calibration and corrections made possible



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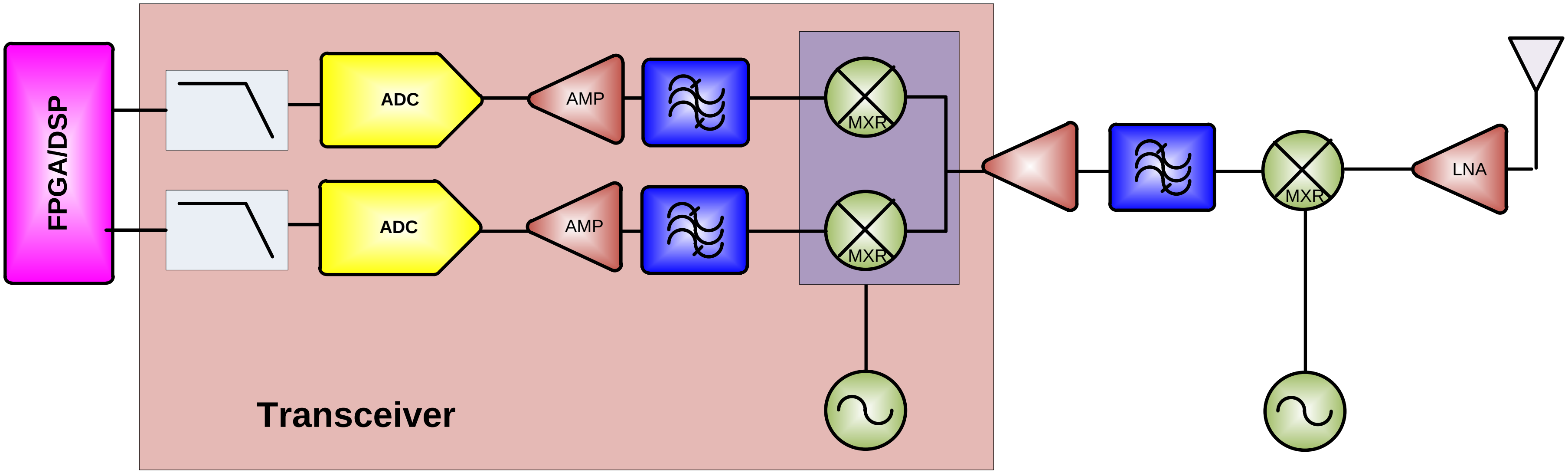
Integrated Solution



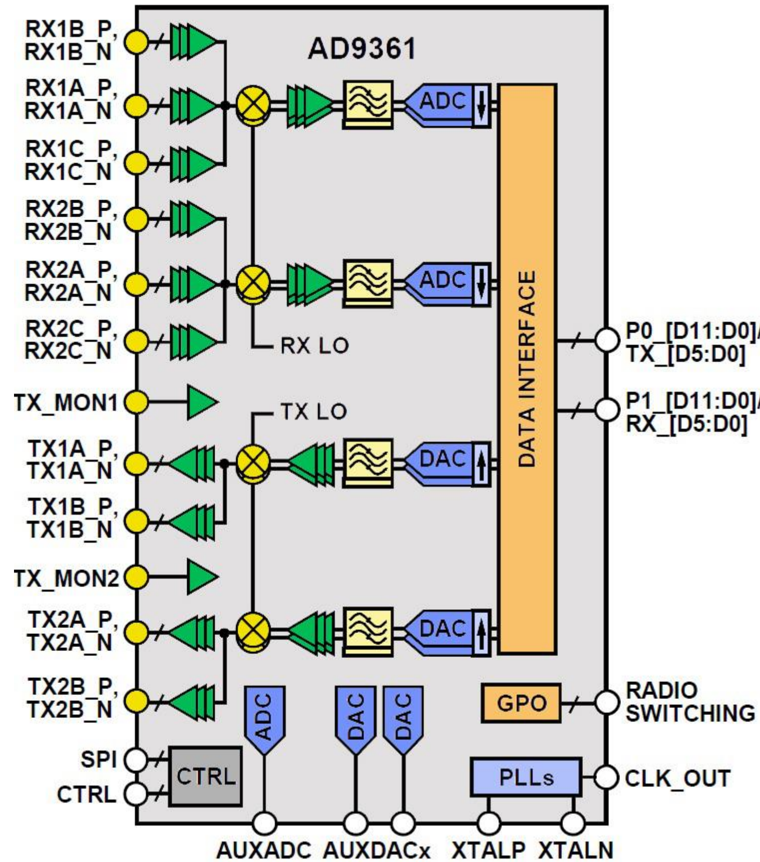
- Integrated ADI transceiver replaces signal chain
  - Highly integrated for significant SWaP reduction
  - Integrated QEC Calibration reduces complexity of IQ demod solution

AD9361 2x2 SW-Defined RF Transceiver IC

Increased Integration

10x10mm
144-Ball Chip
Scale Package
Ball Grid Array

- High-performance 2 X 2 I/Q transceiver
- Integrated 12-bit ADCs and DACs
- Tunable 70 MHz to 6.0 GHz
- 200 kHz to 56 MHz channel bandwidth
- Superior receiver sensitivity with noise figure <2.5 dB
- Highly-linear broadband transmitter with EVM: ≤ -40 dB
- Integrated fractional-N synthesizers



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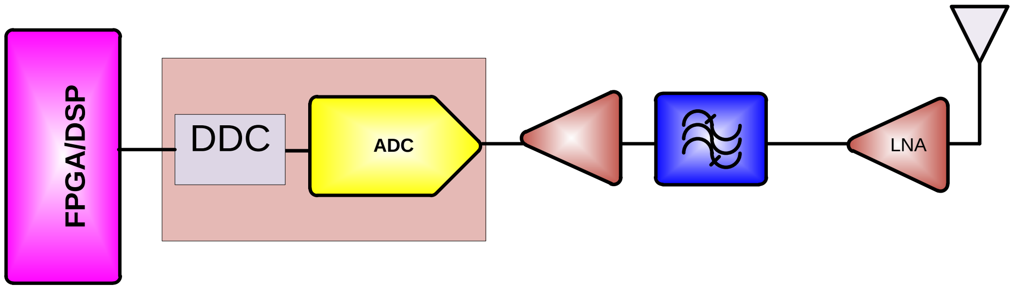
Direct RF & Higher IF Sampling

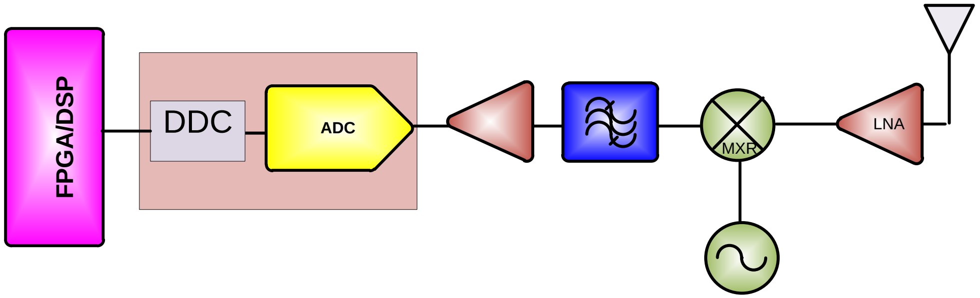
RF Sampling & Higher IF Conversion

- Moves to a more digital approach
- L&S band systems
  - Direct RF sampling
  - No Mixing stages
- X, Ku and Higher
  - Removes second IF
  - System size reduced to single analog mixer
  - Second analog mixer replaced by Digital Down Conversion (DDC).
- DDCs
  - Increase system configurability
  - Increased Agility
  - Dynamic changing from Wideband to Narrowband system

RF sampling L & S band

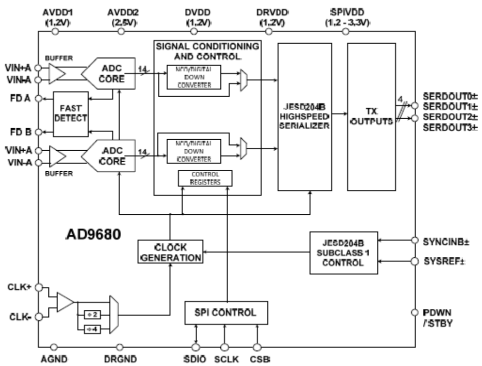


X & Ku band with no 2nd IF



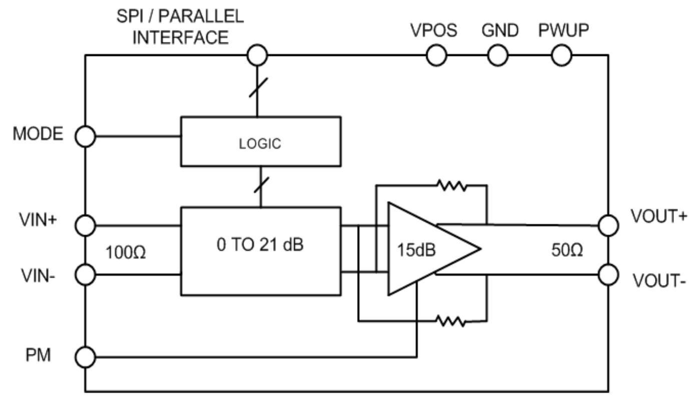
Key Component Examples

AD9680
Dual 14-bit 1250MSPS ADC



- JESD204B (subclass 1) serial digital outputs, 4 lanes
- 1.65W total power per channel at 1GSPS
- Noise Density = -154dBFs/Hz
- SFDR = 81 dBc at 340MHz Fin (1Gsps)
- SFDR = 78 dBc at 1000MHz Fin (1Gsps)
- ENOB = 10.9 bits
- +/-0.5 LSB DNL, +/-1.0 LSB INL
- 2GHz analog input bandwidth

ADA4961
DVGA for Driving GSPS ADCs



- Voltage gain range: −6 dB to +15 dB
- Power gain range: -3 dB to + 18 dB
- 5.8 dB noise figure at maximum gain
- RTO noise 7 nV/√Hz
- IMD3: -100 dB at 1 GHz (max gain)
- OIP3: 50 dBm at 1 GHz (max gain)
- −3 dB bandwidth of 25 MHz to 2.5 GHz
- Single 3.3 V to 5 V supply operation
- 150 mA supply current

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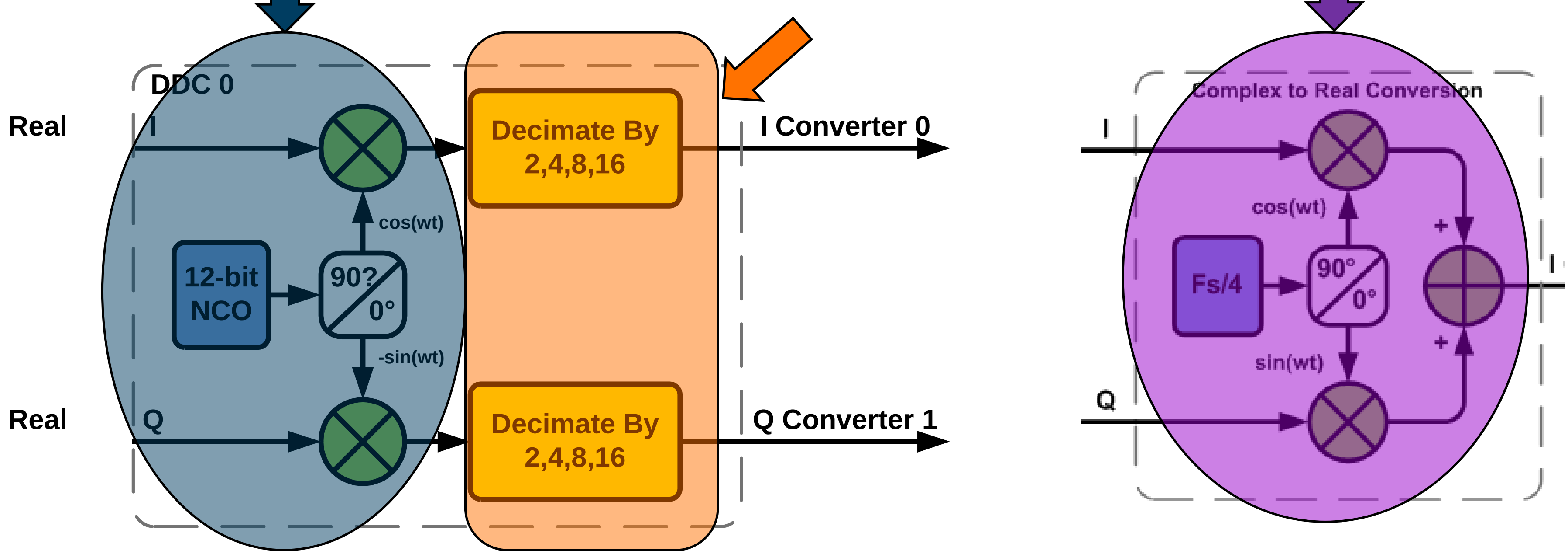
Conceptual Description of Integrated DDC

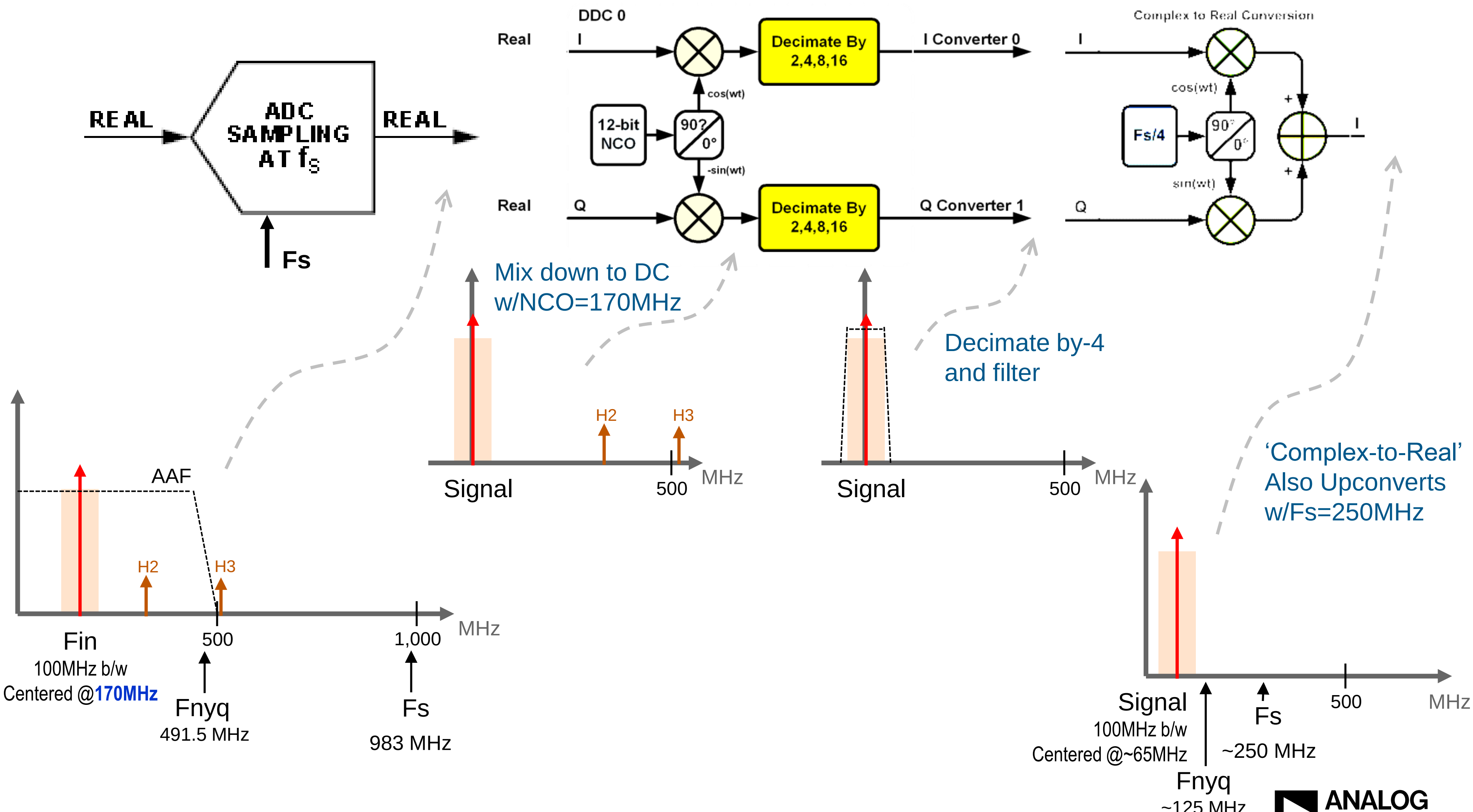
- NCO/Mixer
  - Effectively tunes the analog input signal
  - 12 bit NCO resolution

- **Decimation**
  - Decimates and filters to reduce data rate and provide processing gain
  - %fs bandwidth

- **Complex to Real**
  - Removes the complex portion for real outputs



Conceptual Description of Integrated DDC



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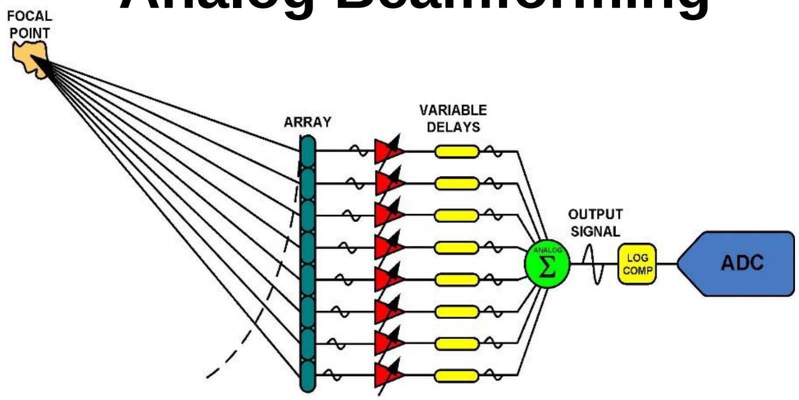
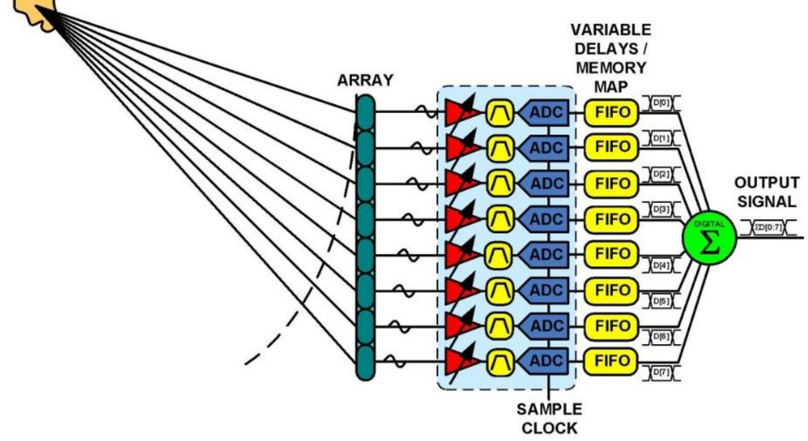
Phased Array Systems

Digital vs Analog Beamforming

Analog Beamforming



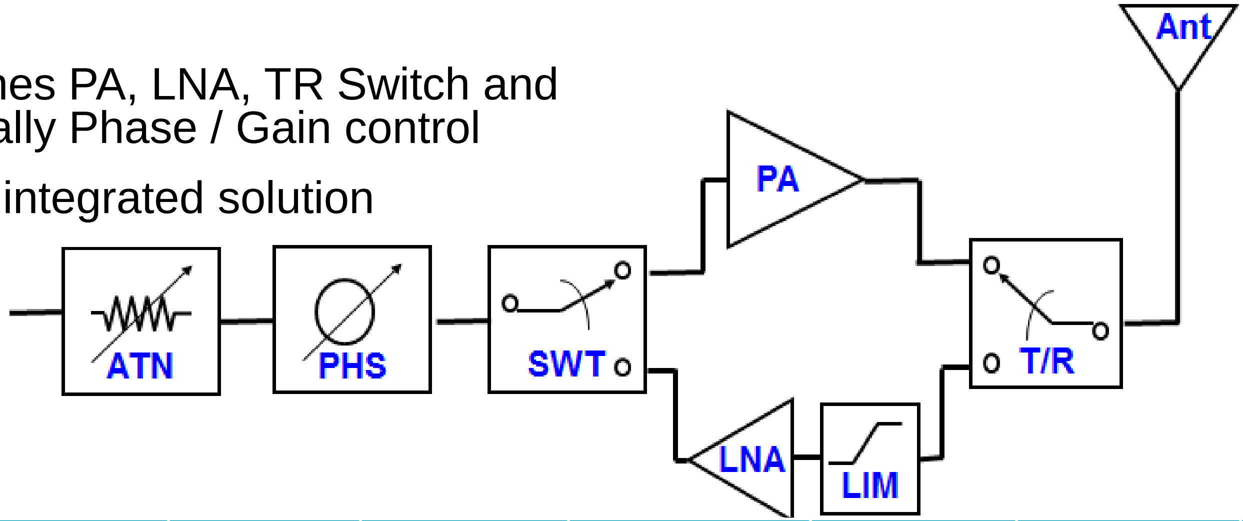
Digital Beamforming



- ***Beamforming systems essentially multiple instantiations of signal chains shown with phase control added in analog or in digital domains***
- **Digital Beam Forming system provide most flexibility**
- **Challenged by current SWaP**
  - **Digital processing of all data requires significant power**
  - **Difficult to implement close to the antenna**
- **Current systems use a mix**
  - **Analog Sub-arrays with reduced digital channels and digital beamforming**

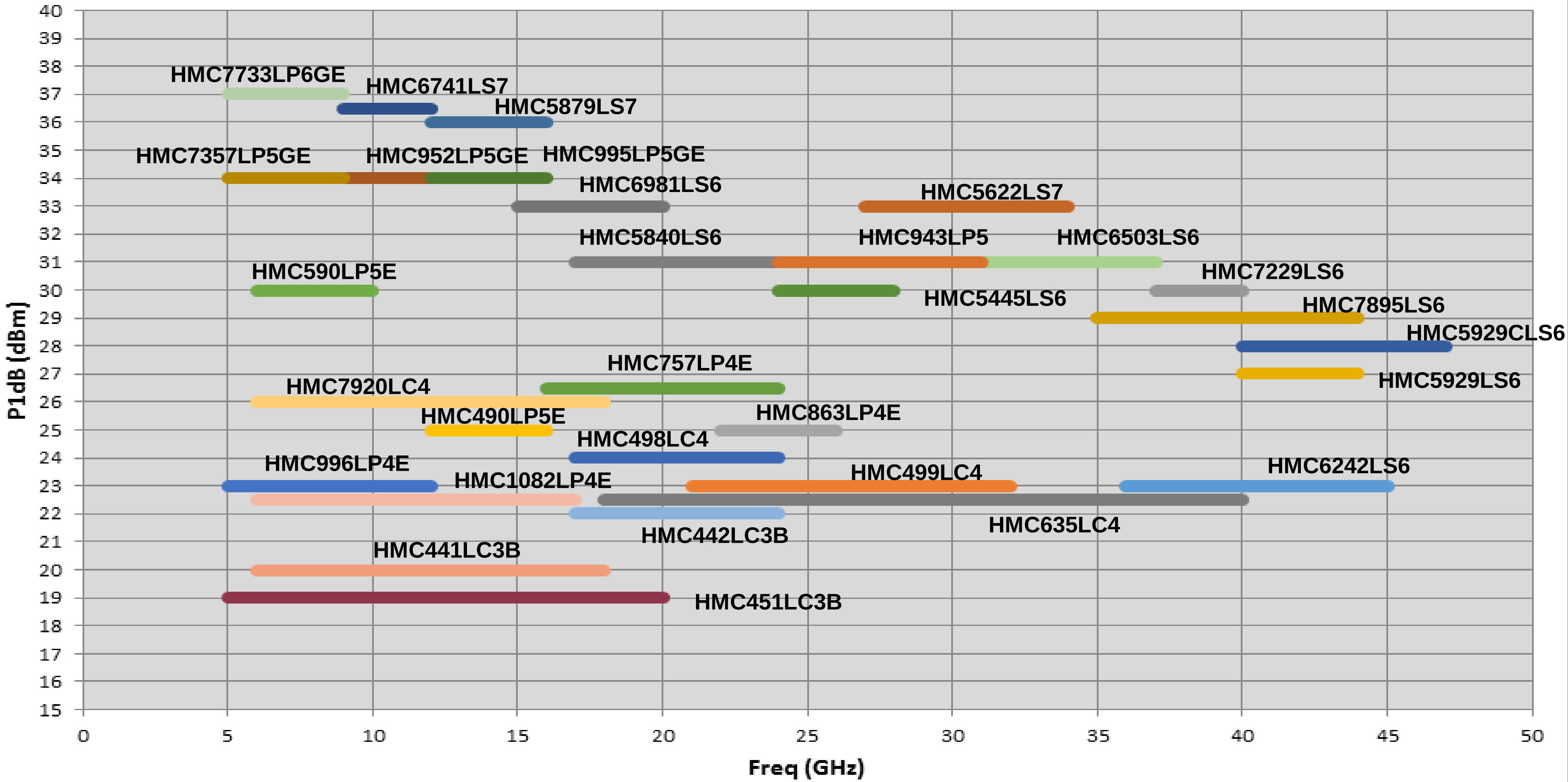
Basic Radar Transmit & Receive Module (TRM) Diagram

- TRM
  - Combines PA, LNA, TR Switch and potentially Phase / Gain control
  - Highly integrated solution



Freq Band	Digital Phase Shifter	Digital Atten	SPDT Switch	LNA	Gain Blocks	Driver Amplifier	Power Amplifier
S	HMC647	HMC472 HMC624 HMC425	HMC349 HMC849	HMC73123	HMC740 HMC741 HMC474 HMC589	HMC789 HMC414	HMC921 HMC1086
X	HMC642 HMC643	HMC424	HMC232	HMC902 HMC753	HMC788 HMC365	HMC441 HMC608	HMC487 HMC952 HMC1053

ADI Driver / Power Driver & Power Amplifiers for Defense Applications



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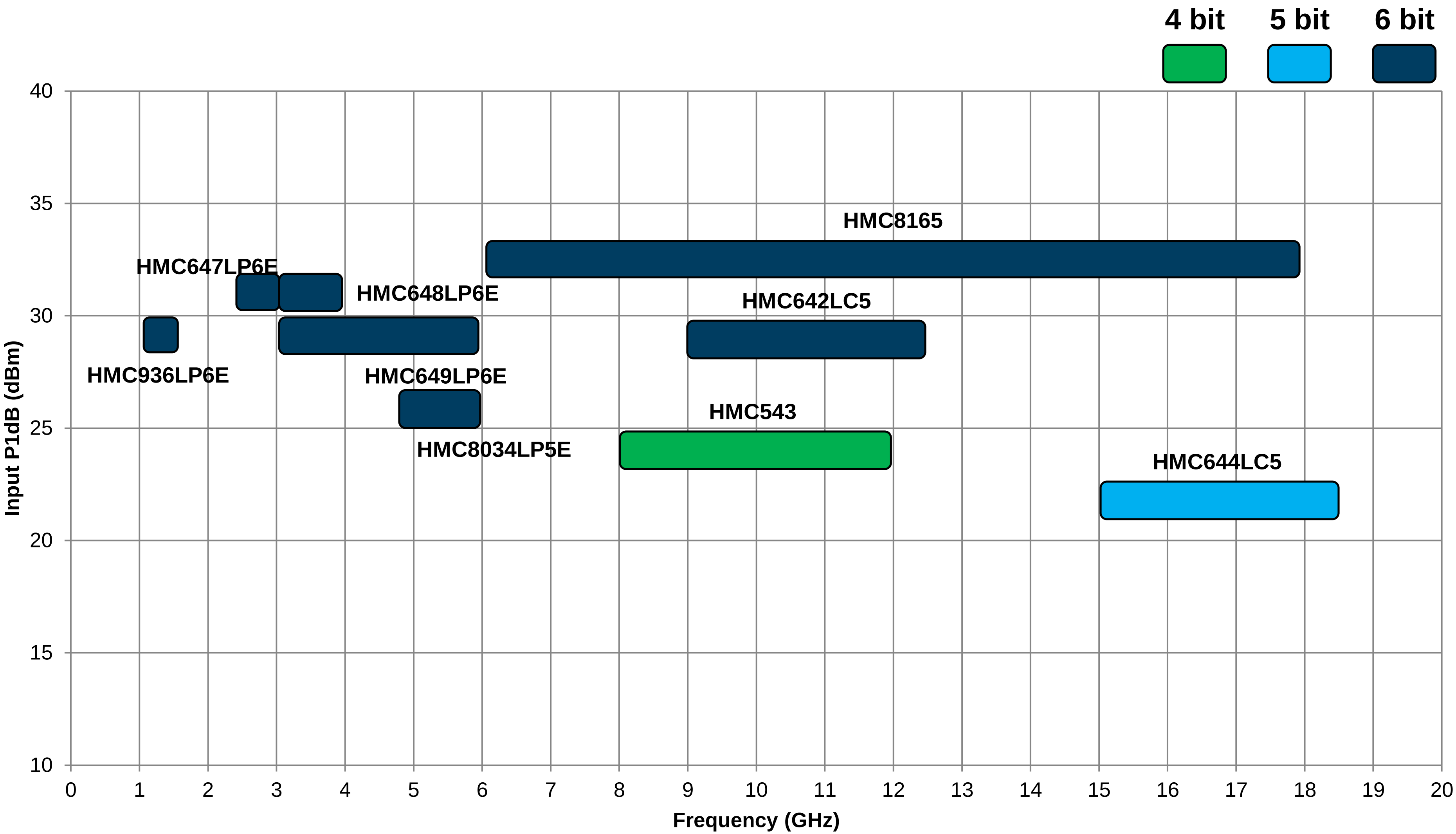
Digital phase shifters Frequency coverage



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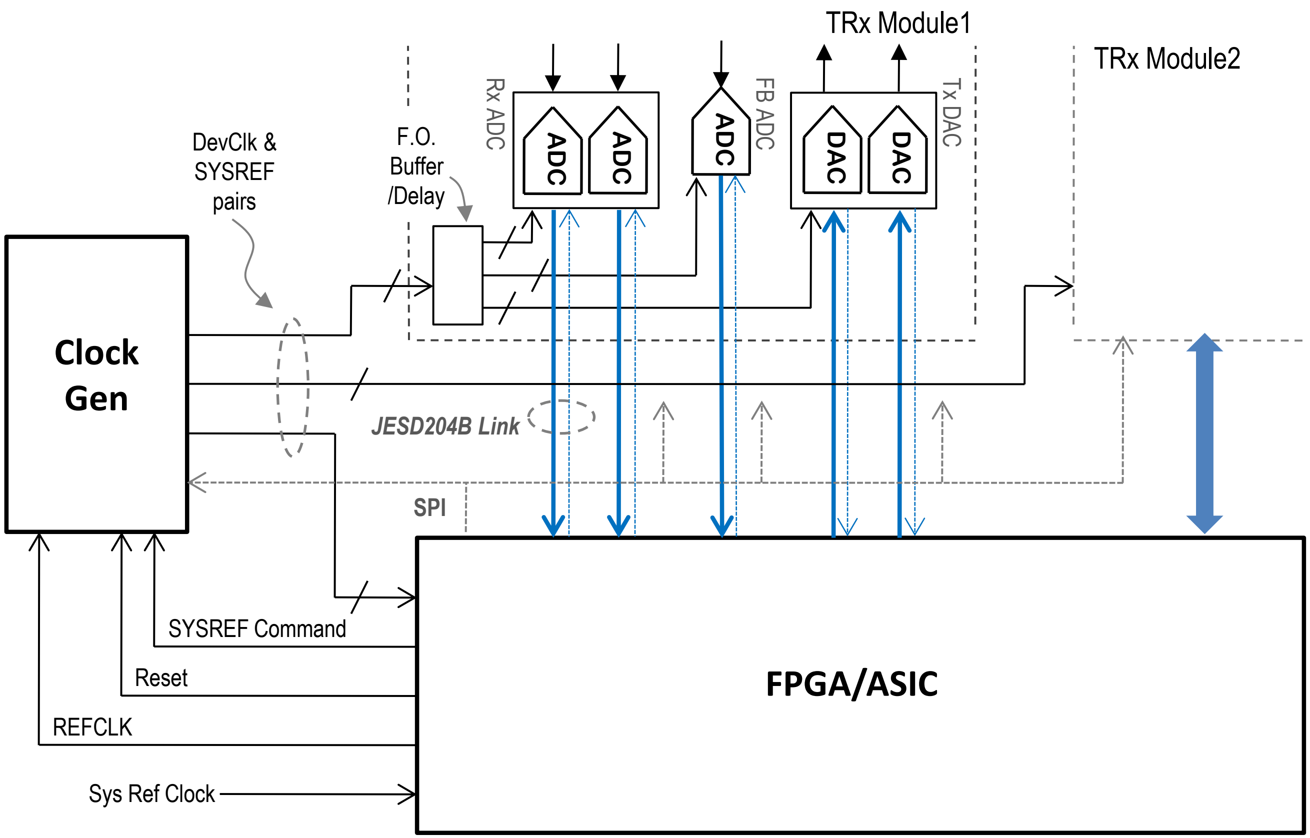
JESD204B: Typical System Architecture



- ADI Clock Generation Devices & ADCs support mult-channel synchronization using JESD204B
- JESD204B Interface Reduces Interface complexity

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HMC7044: 14-output, Ultra Low Jitter Clock Generator with JESD204B Support

Features:

- **Output Frequency Range: 0.5 - 3000 MHz**
- **Input Frequency Range: 10 – 750 MHz**
- **14 Clock Outputs**
  - » Up to 7 may be used as SysRef outputs matched to their associated DeviceClock output
- **Dual loop architecture for 'jitter attenuation' applications**
- **Excellent jitter and phase noise floor performance**
  - ✓ 53 fsec jitter (typical) (integ. RMS, 12kHz to 20MHz)
- **Coarse** (1/2 VCO period steps) **and Fine** (25ps nominal steps) **delay available at each output**
- **Choice of LVDS, CML, LVPECL or CMOS outputs**
- **+3.3V power supply**
- **Approx. 1.6 to 2.8W active mode power**

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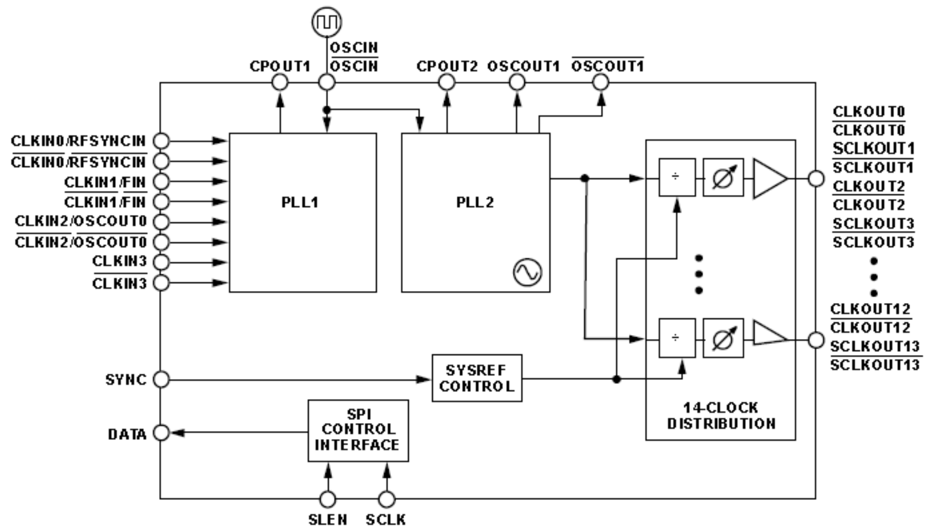
Key Benefit
◆ *Industry-best jitter performance*



Temp	Package
-40°C – +85°C	68-pin, 10x10mm QFN

Target Sampling	Target Release
Now	Q4, 2015

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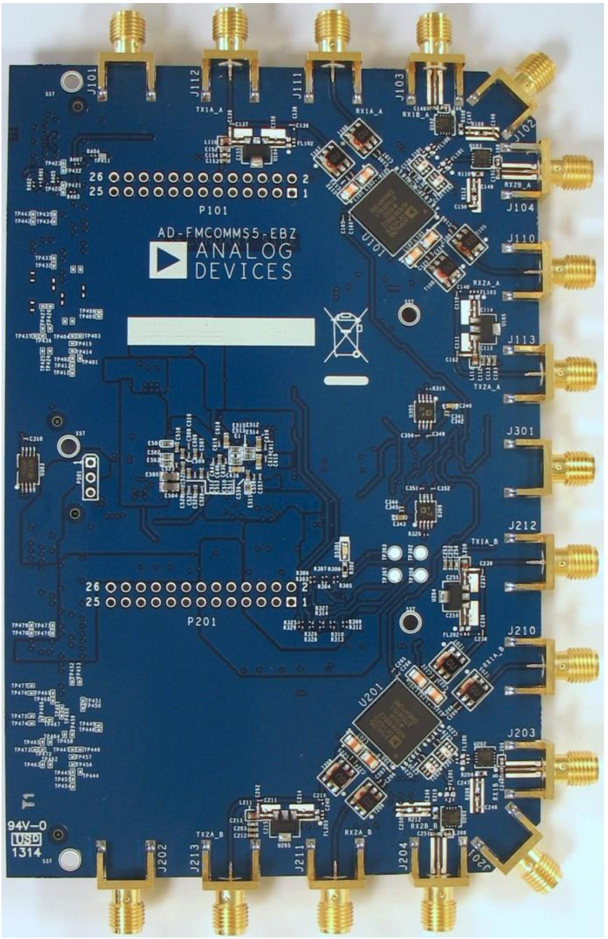
FMCOMMS5 – MIMO Prototyping Platform
Solves Synchronization challenge!

- Dual AD9361, 4Rx 4Tx MIMO operation
  - Any subset of 4R4T supported (eg 4R0T, etc)
- Phase calibration network on board
  - Required hardware in place
  - Software calibration control is open source
- Option to use external LO source
  - Single PLL can drive all Rx and Tx paths
  - Potential phase noise improvement
  - Allows for phase calibration to be a single shot calibration
- Multiple RF ports with connectivity
  - Some ports are wideband
    - Direct balun connectivity
  - Some ports are 2.4GHz narrowband
    - In line bandpass filter and amplifier
- Mates to the Xilinx ZC706 FPGA platform



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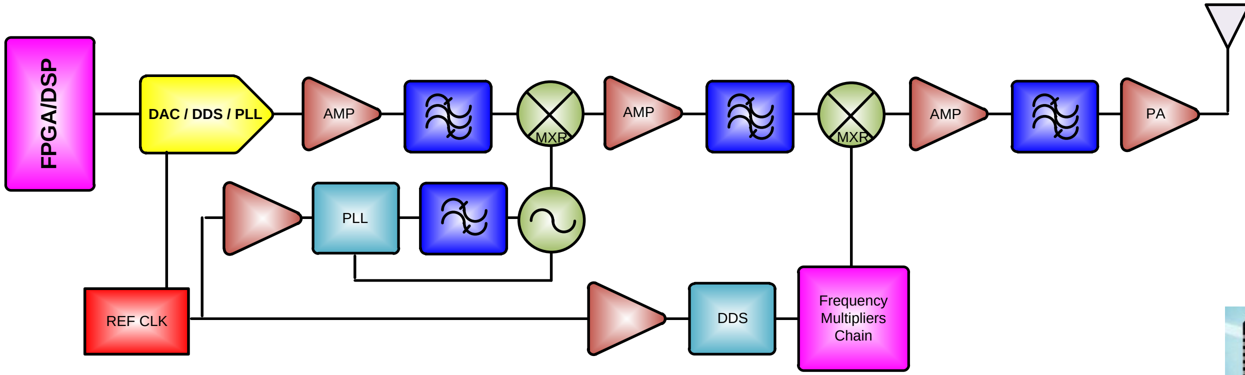
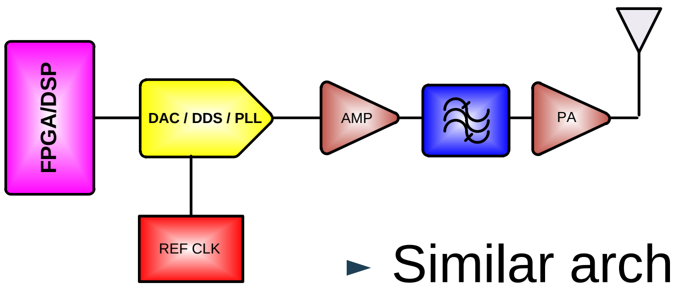
Radar Exciters



Classical Exciter Architecture



Direct RF Synthesis

- Similar architecture to Rx chains
- Waveform Generation undertaken by
  - RF & IF DACs – AD9144 / AD9739 / AD9129 DACs
  - DDS Devices – AD9914
  - PLL – ADF4159

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Primary Products We Talked About Today

HMC558	GaAs MMIC FUNDAMENTAL MIXER
ADL5367	500 MHz to 1700 MHz Balanced Mixer
AD9467	16-Bit, 200 MSPS/250 MSPS A/D Converter
ADL5380	400 MHz TO 6000 MHz Quadrature Demodulator
AD9655	Dual, 16-Bit, 125 MSPS Serial LVDS, 1.8 V A/D Converter
AD9361	RF Agile Transceiver
AD9680	14-Bit, 1 GSPS/820 MSPS/500 MSPS JESD204B, Dual ADC
ADA4961	Low Distortion, 3.2 GHz, RF DGA
HMC7044	High Performance, 3.2 GHz, 14-Output Jitter Attenuator with JESD204B
AD9914	3.5 GSPS Direct Digital Synthesizer with 12-bit DAC
AD9129	14-Bit, 5.6 GSPS, RF Digital-to-Analog Converter
ADF4159	Direct Modulation/Fast Waveform Generating, 13 GHz, Fractional-N Frequency Synthesizer
AD-FMCOMMS5-EBZ	
AD-FMCOMMS6-EBZ	

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Summary

- Future Advanced Radar Systems looking at Multi-mode and Multi-function operation
- Cognitive and configurability drive architectures from Superhetrodyne to Direct Conversion and RF Sampling architectures with increase in digital signal process
- ADI devices, solutions and modules provide comprehensive options to the range of signal chains used today, tomorrow and into the future

- To learn more about ADI’s capabilities in radar applications, visit www.analog.com/ADEF

Thank You For Watching!

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