Keysight Measurement Forum 2016

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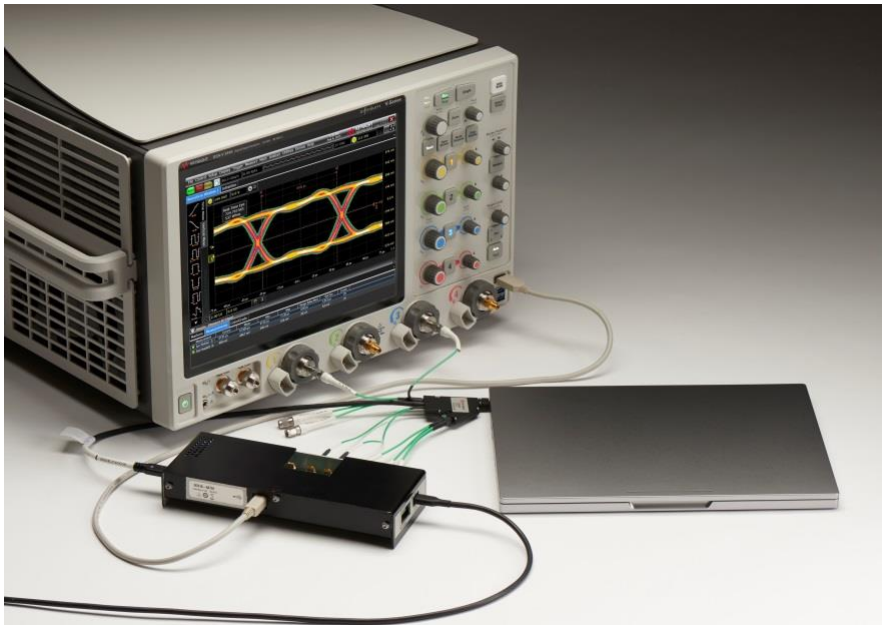
USB3.1 / Type-C / Power Delivery Test Challenge and Solution

KEYSIGHT TECHNOLOGIES

HARDWARE+SOFTWARE+PEOPLE=INSIGHTS

USB Type C Connector and USB3.1 Test Solution



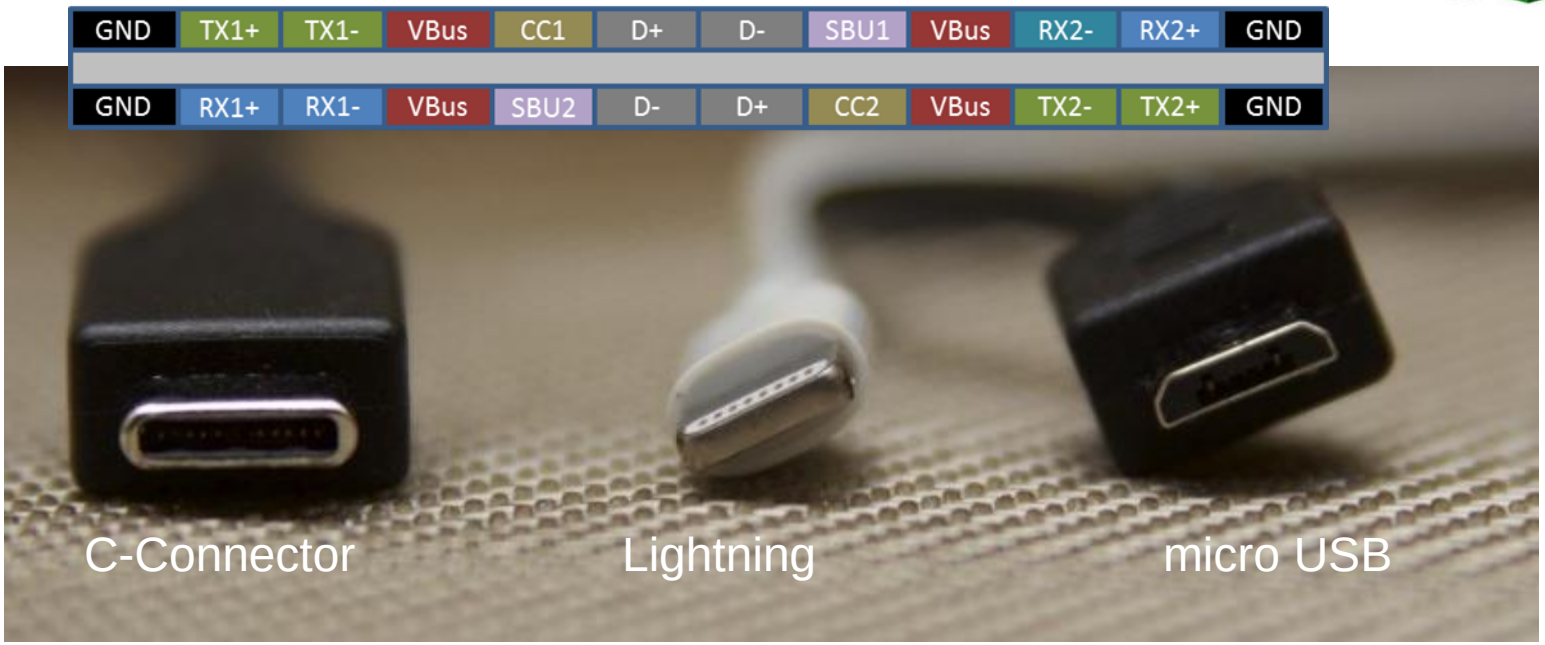
KEYSIGHT TECHNOLOGIES

Agenda

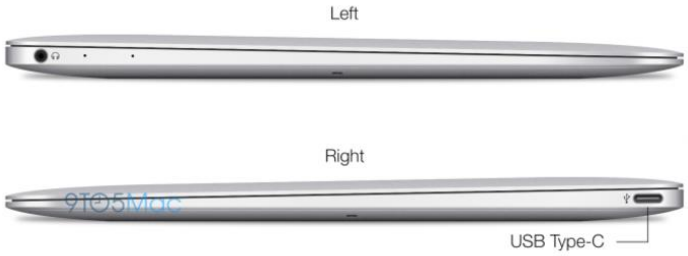
- **Introduction to the USB Type C Connector**
- USB3.1 Type C Test challenge
- USB3.1 Transmitter Test solution
- USB3.1 Receiver Test Solution
- Summary

What is the USB C-Connector?

"One connector to rule them all"

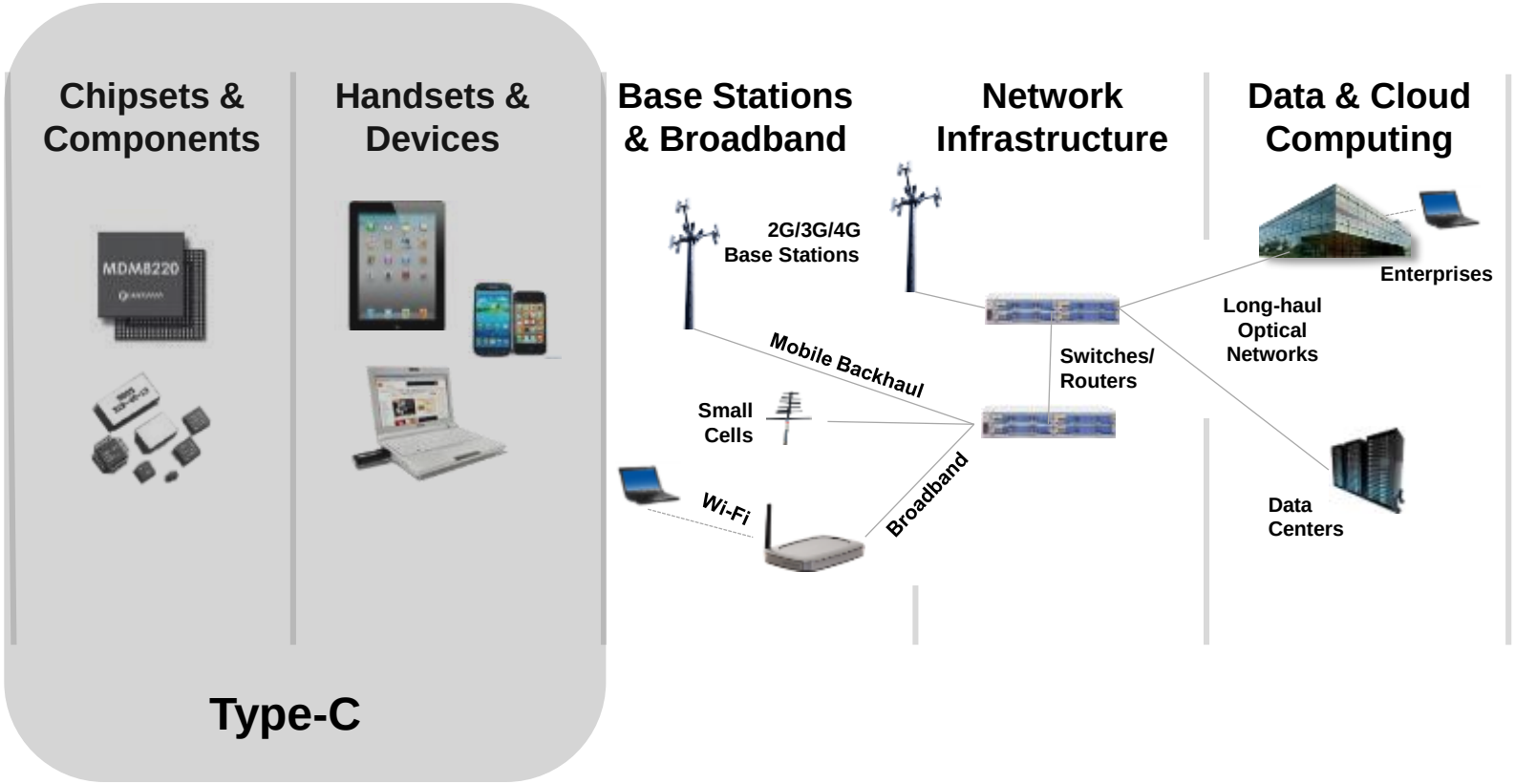


Ethernet, DisplayPort, Power, SATA, VGA, USB2 replaced by **C type connector**. Computers and tablets will have only one connector for data transport and that will be the USB Type C



- ✓ **Reversible (can be flipped)**
- ✓ **Can handle 5 Amps at 20Volts**
- ✓ **Broad application in standards**
- ✓ **Low Profile**
- ✓ **10Gbs with way to 40Gbs**

The Communications Ecosystem
Where does USB-C fit?



USB Type-C Cable and Connector

Key Features:

- USB 2.0 (HS, FS, LS)
- USB 3.1 (Gen1, Gen2)
- Reversible plug orientation and direction
- Smaller size
- Extra pins for VBUS to achieve higher power (up to 100W)
- Display standards are looking at this as the next Gen display connector

Figure 2-1 USB Type-C Receptacle Interface (Front View)

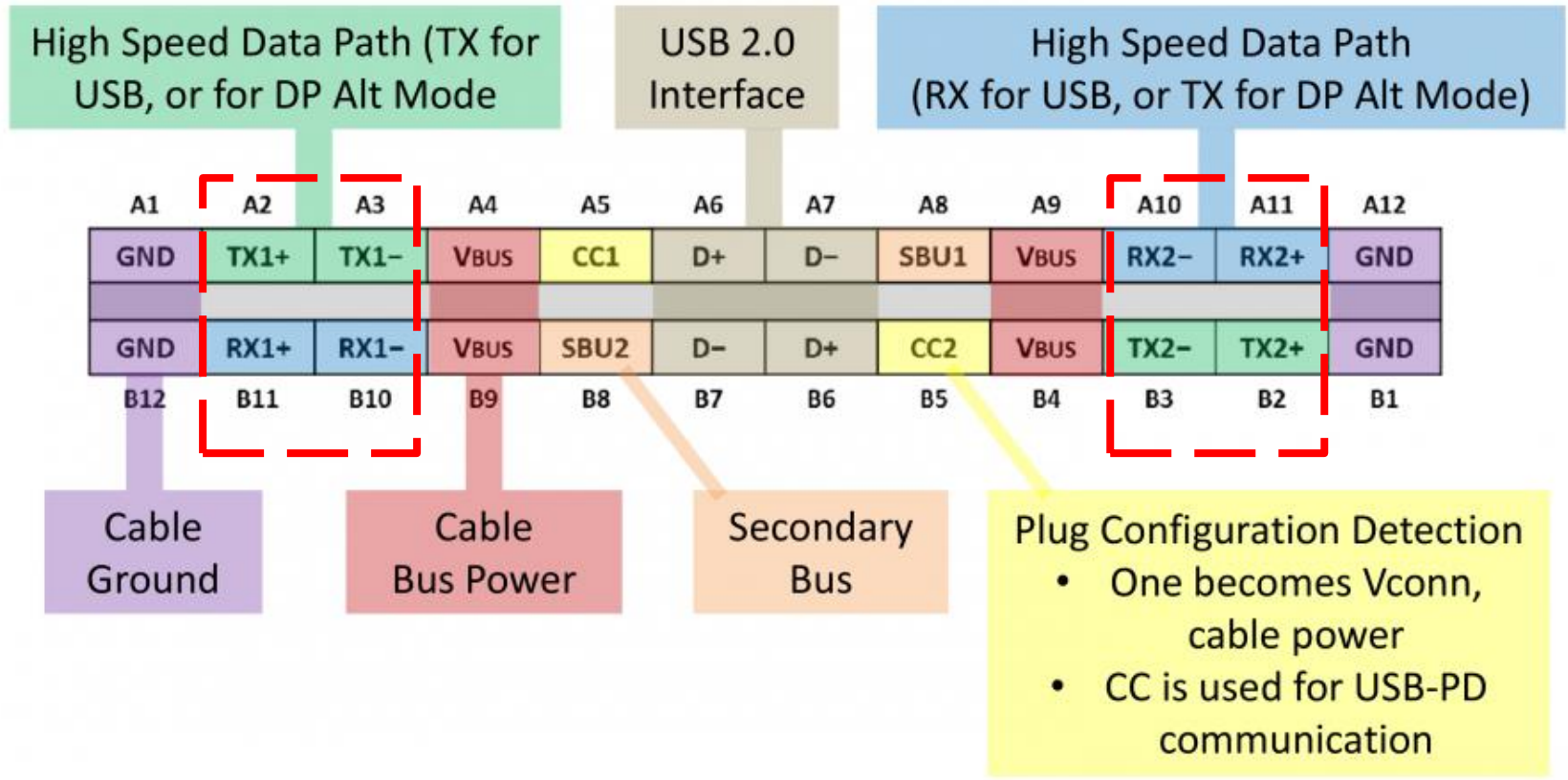
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1−	VBUS	CC1	D+	D−	SBU1	VBUS	RX2−	RX2+	GND
GND	RX1+	RX1−	VBUS	SBU2	D−	D+	CC2	VBUS	TX2−	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

Figure 2-2 USB Full-Featured Type-C Plug Interface (Front View)

A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2−	VBUS	SBU1	D−	D+	CC	VBUS	TX1−	TX1+	GND
GND	TX2+	TX2−	VBUS	VCONN			SBU2	VBUS	RX1−	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

Source: IDF14 (NETS002), Intel

USB Type C-Signal Plan



Alt Mode

A port could wake up as USB 3.1, then get configured to DisplayPort 1.3

SUPERSPEED+ CERTIFIED USB 10Gbps

MHL Mobile High-Definition Link

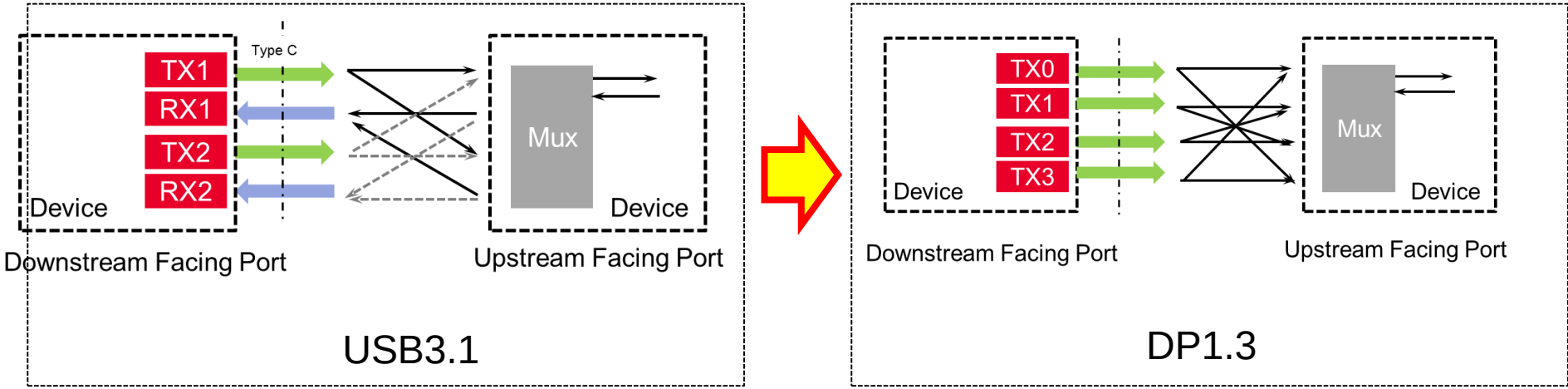
THUNDERBOLT™

DisplayPort 1.3

Alternate Mode

– An operational mode of devices on a link that dynamically reassigns USB Type-C pin functionality by communication via the Power Delivery channel to change the character of the link.

Example: a 'device' can wake up USB3.1 and change to DP1.3



DisplayPort 1.3, MHL, & Thunderbolt

Agenda

- Introduction to the USB Type C Connector
- **USB3.1 Type C Test challenge**
- USB3.1 Transmitter Test solution
- USB3.1 Receiver Test Solution
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Why Does It Matter?

Simplicity and Capability to consumer….

……Complexity to Designers, Integrators, and Validators

Speed

Speeds of the Future and
Backwards Compatibility

Power

Up to 100 W

Power direction no longer fixed

Standards Integration

MHL Mobile High-Definition Link

DisplayPort

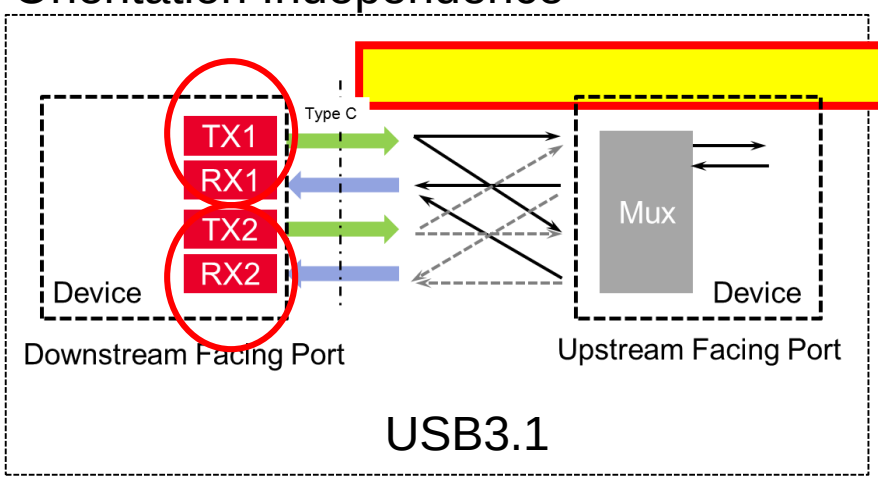
SUPERSPEED+ USB 10Gbps

THUNDERBOLT

KEYSIGHT TECHNOLOGIES

Implications of Type C for Compliance Testing

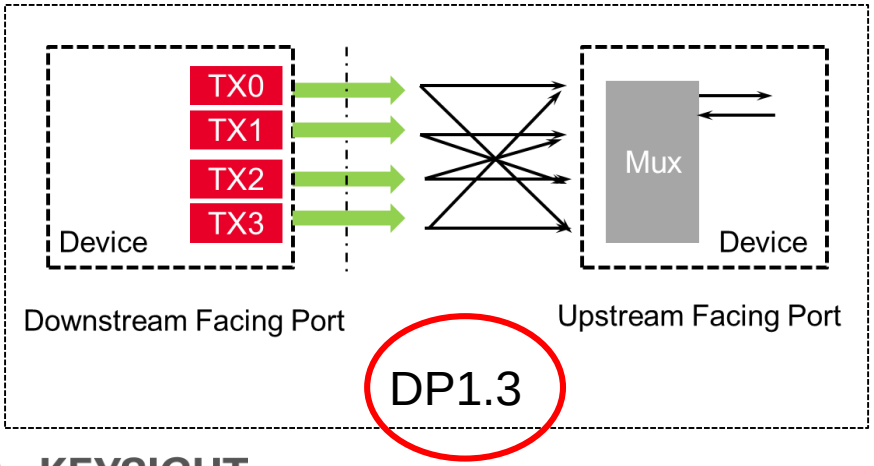
Orientation Independence



Test time ***DOUBLES !***

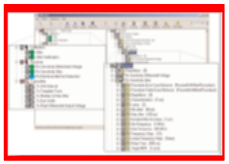
Test *USB3.1* ***Twice !***, THEN

Alternate Mode



Test ***DisplayPort !***

Test System Changes

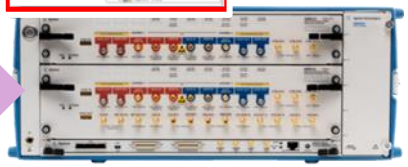


Application Software RX Test

Type C connector

Test Signal Breakout

Switch Matrix

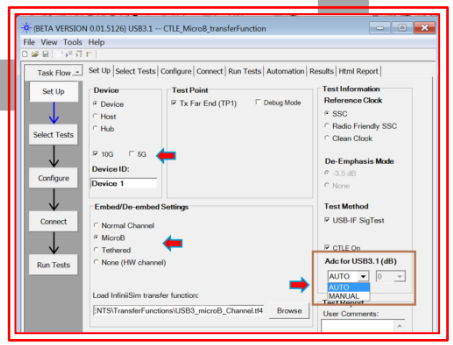


Pattern Generator, BERT

Oscilloscope

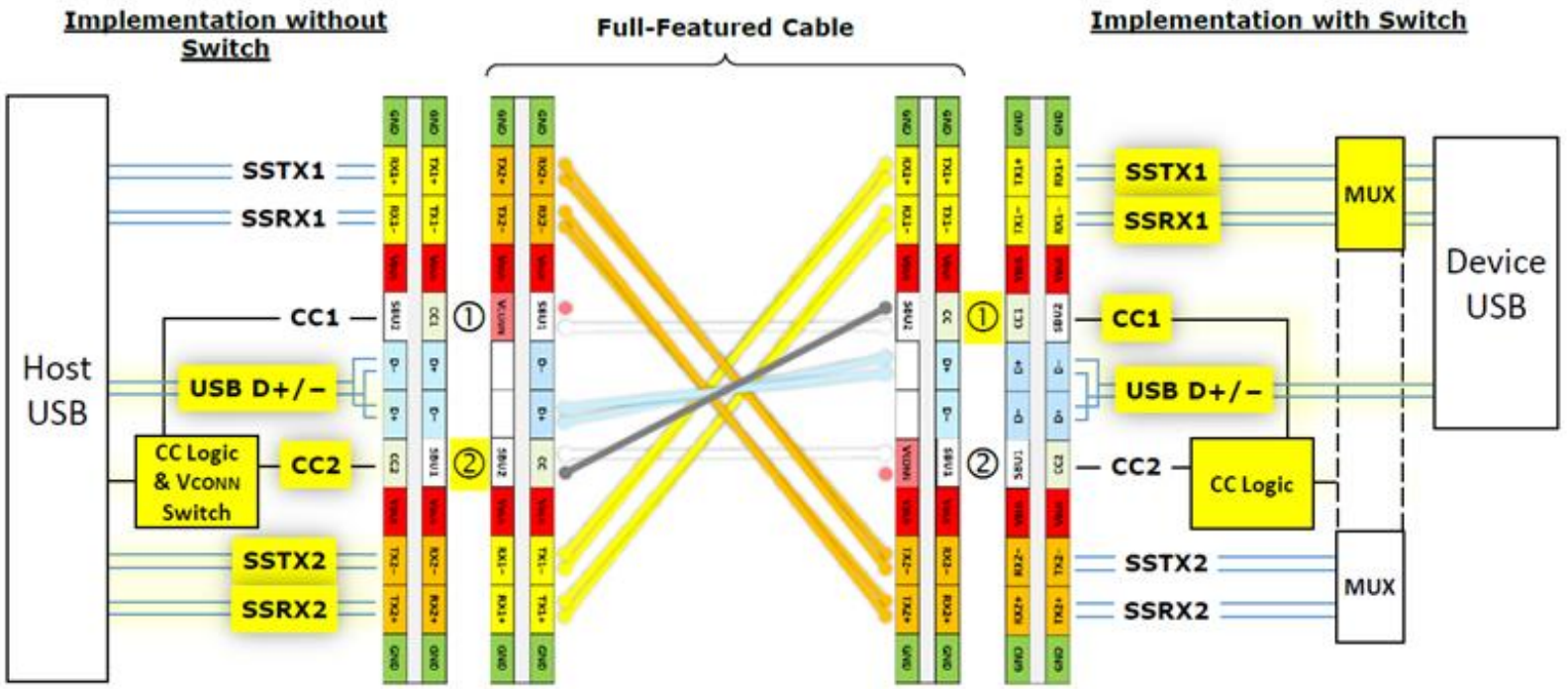
Power Supply

Power Delivery Controller



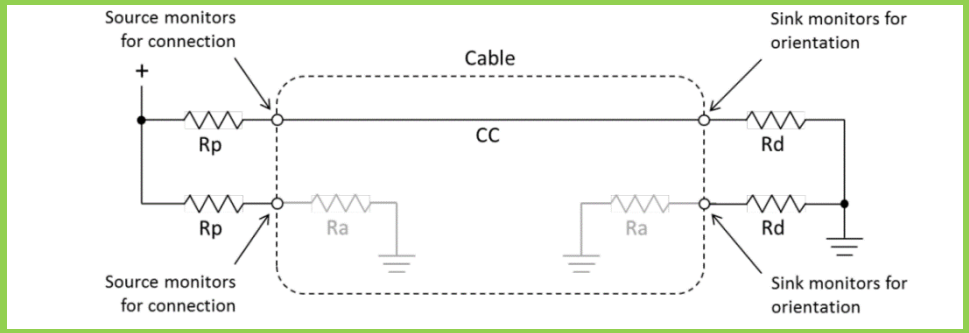
Application Software TX Test

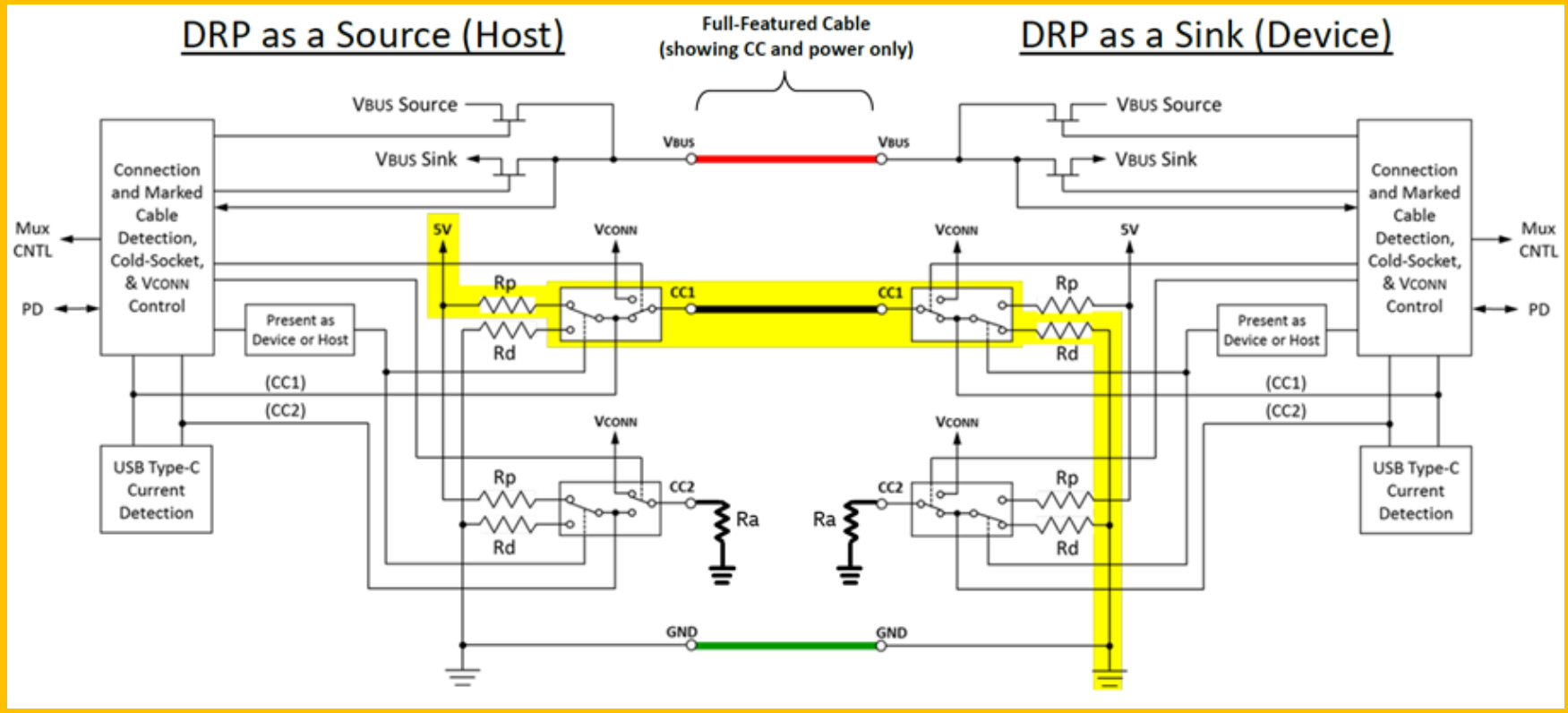
Type-C Implementation Challenges



- ⇨ Flipped twisted through – Position ② ⇔ Position ①

USB-PD CC Challenges





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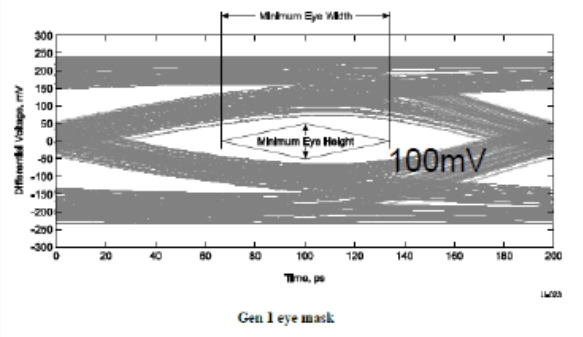
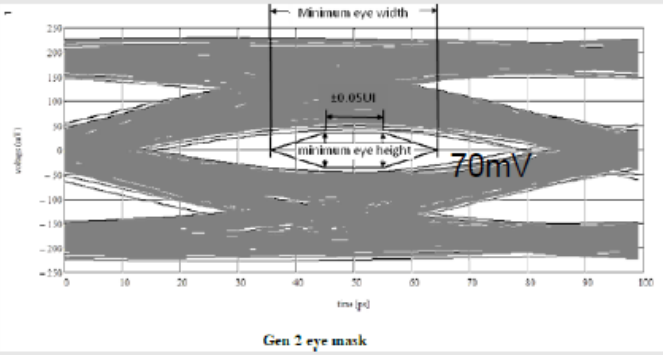
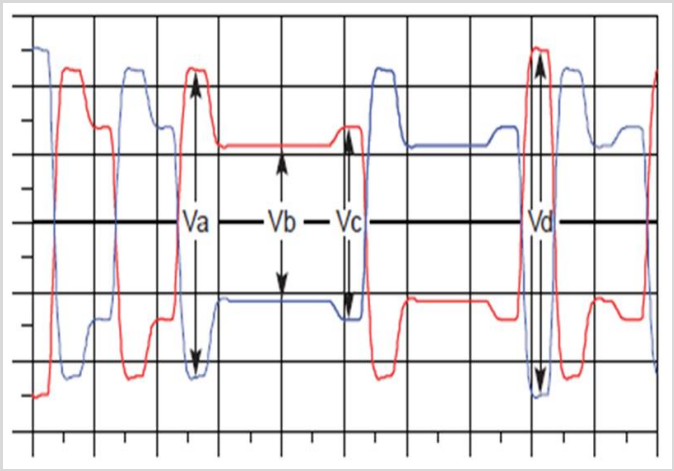
USB 3.1 Gen1 vs Gen2

	Gen1	Gen2
Data rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b (20% additional bandwidth over 8b/10b)
Tx REF EQ	Normative Post: -3 dB	Informative Pre: 2.2 dB Post: -3.1 dB
Rx REF EQ	CTLE	CTLE (6 level) + 1 tap DFE
CDR (JTF BW)	4.9 MHz	7.5 MHz
Eye Height / Mask	 Gen 1 eye mask	 Gen 2 eye mask
TJ	132 psec (0.66 UI)	71.4 psec (0.714 UI)
Target Channel	3 meter (-17 dB @ 2.5 GHz)	1 meter -23 dB @ 5 GHz

USB 3.1 Requires Tx and Rx Equalization

It's all about creating clean eyes

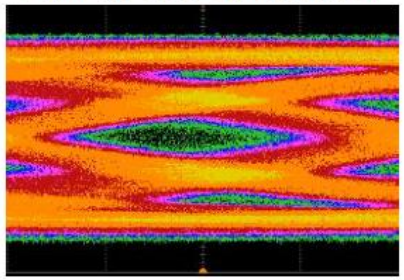
- Tx Equalization
  - Pre-shoot
  - De-emphasis
  - Pre-emphasis



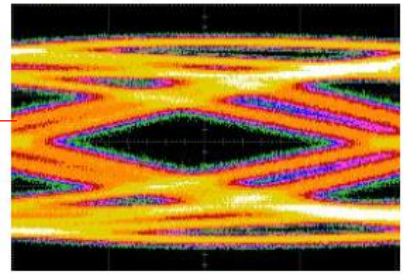
Tx → Rx

- Rx Equalization
  - CTLE
  - DFE
  - FFE

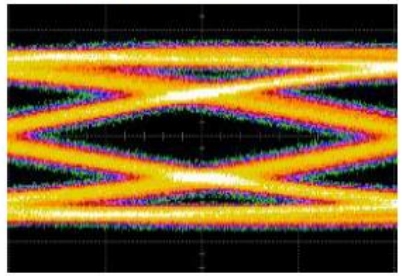
Eye at end of channel



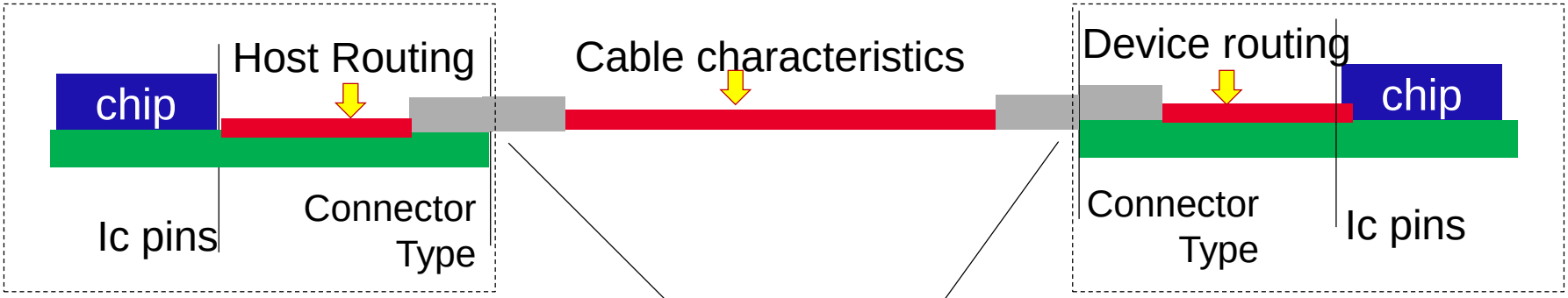
CTLE (-6dB)



+ 1 tap DFE

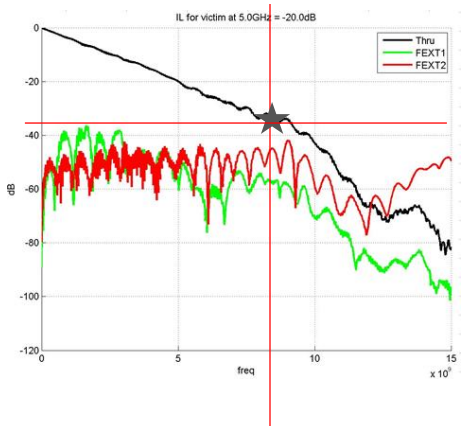


USB3.1 Channel Budget

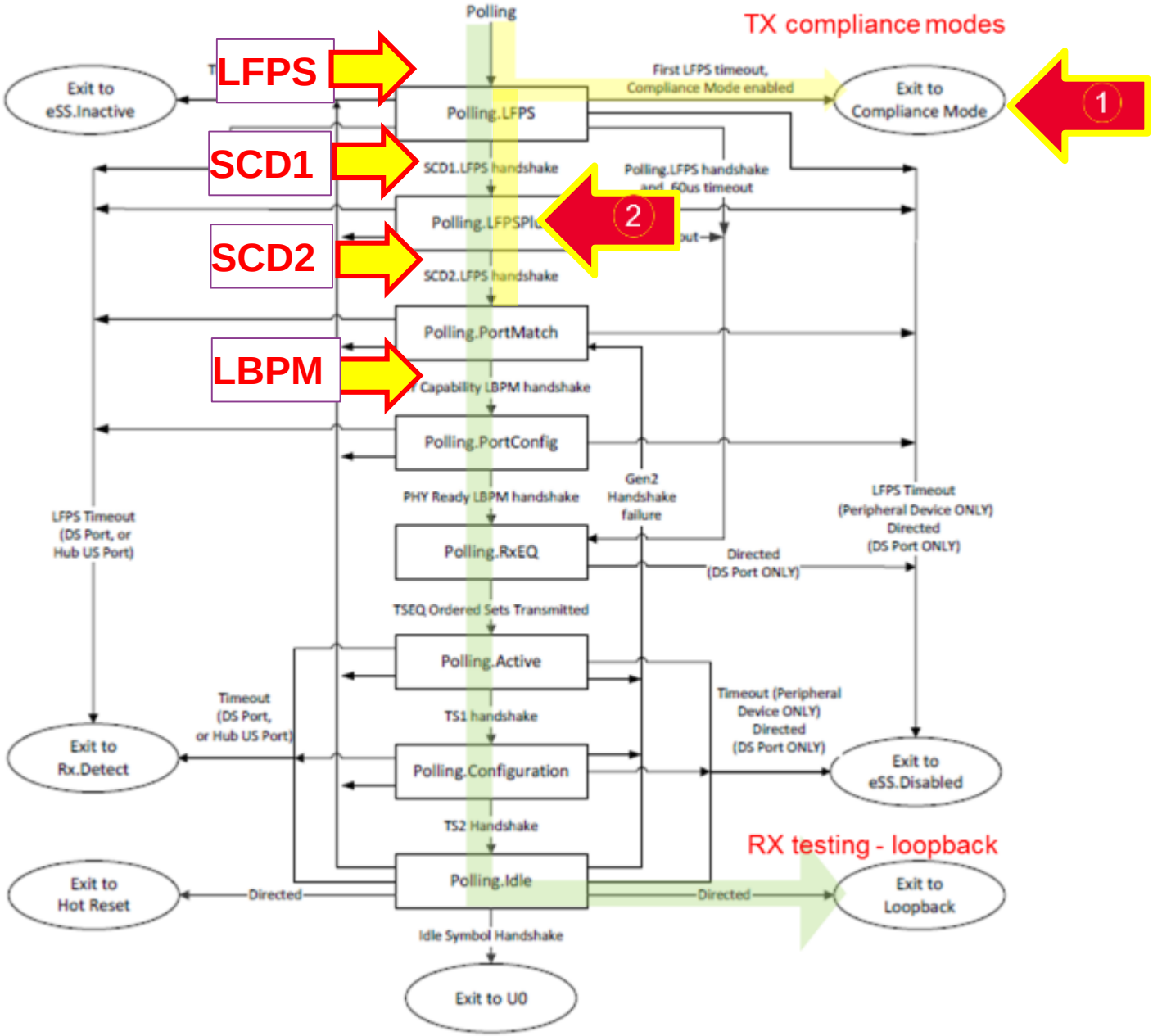


Loss at Nyquist is identified here. Channel Models (s-parameters) required.

Data Rate	Host	Connector	Cable	Connector	Device
5G	10dB	Std A	7.5dB	Std B	2.5dB
5G	10dB	Std A	3.5dB	Micro B	6.5dB
5G	6.5dB	C	7dB	C	6.5dB
5G	10dB	Std A	3.5dB	C	6.5dB
5G	6.5dB	C	4dB	Std B	2.5dB
5G	6.5dB	C	4dB	Micro B	6.5dB
10G	8.5dB	Std A	6dB	Std B	8.5dB
10G	8.5dB	Std A	6dB	Micro B	8.5dB
10G	8.5dB	Std A	6dB	C	8.5dB
10G	8.5dB	C	6dB	Std B	8.5dB
10G	8.5dB	C	6dB	Micro B	8.5dB
10G	8.5dB	C	6dB	C	8.5dB



USB 3.1 State Machine



KEYSIGHT TECHNOLOGIES

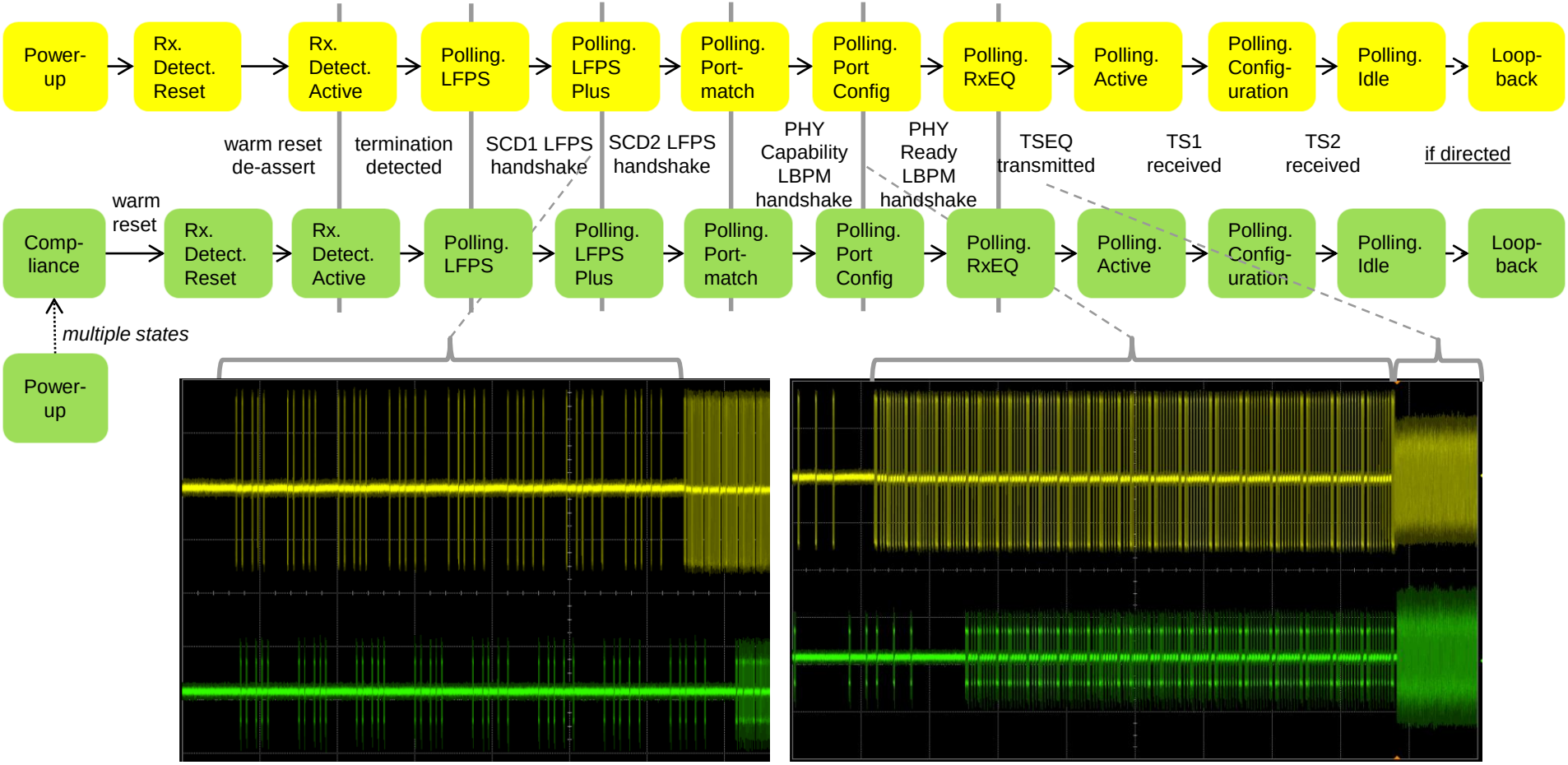
USB 3.1 Compliance Patterns

Table 6-13. Compliance Pattern Sequences

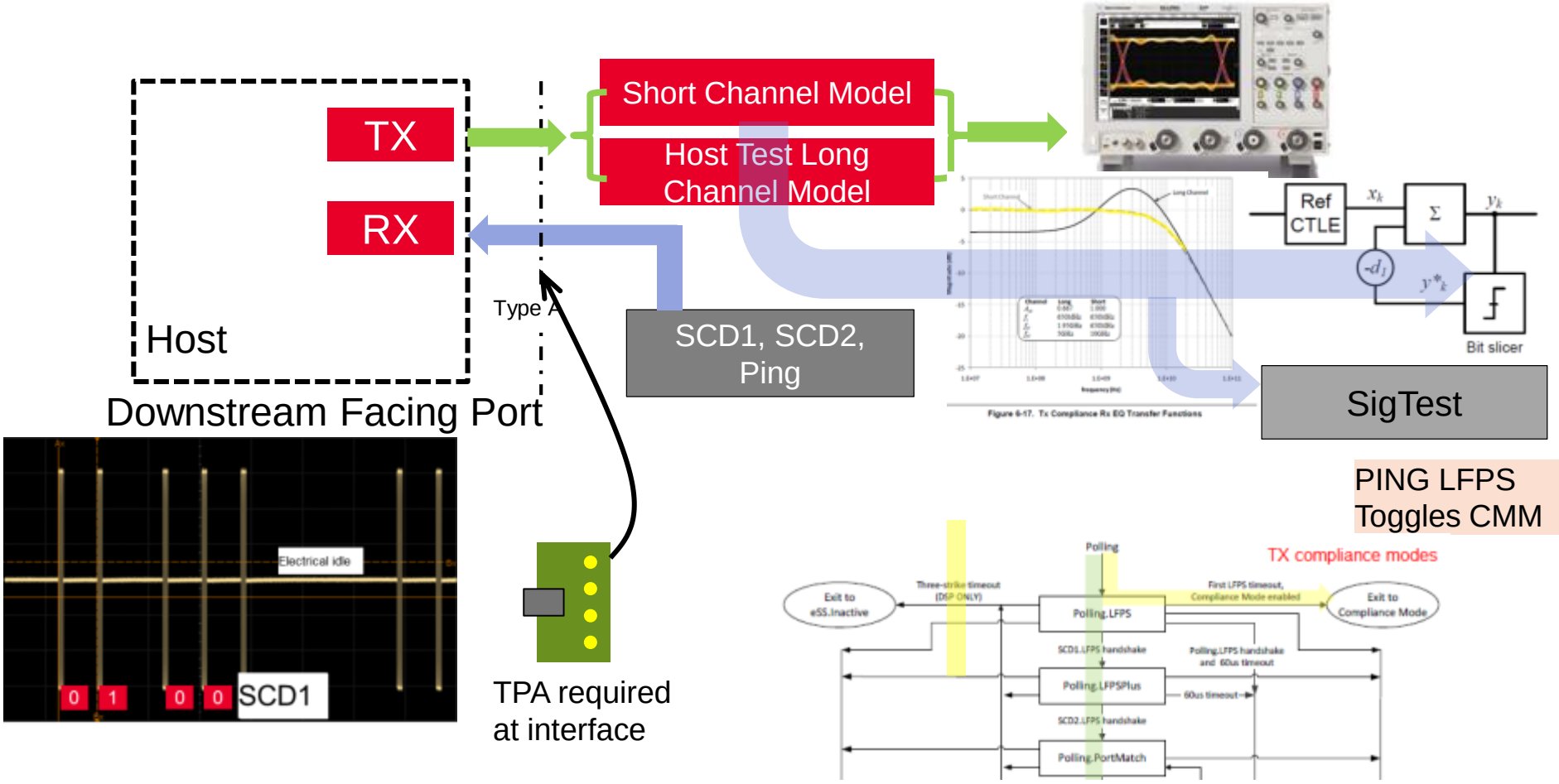
Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences.
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	~~With ~~wWithout de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP9		Pseudo-random data pattern (see section 6.4.4.1)
CP10	AAh	Nyquist pattern at 10Gb/s. This is not 128b132b encoded.
CP11	CCh	Nyquist/2 at 10Gb/s, This is not 128b132b encoded.
CP12	LFSR15	Uncoded LFSR15 for PHY level testing and fault isolation. This is not 128b132b encoded. The polynomial is x^15+x^14+1.
CP13	64 1's and 0's	With pre-shoot defined in section 6.7.5.2 (no de-emphasis). Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP14	64 1's and 0's	With de-emphasis defined in section 6.7.5.2 (no pre-shoot). Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP15	64 1's and 0's	With pre-shoot and de-emphasis defined in section 6.7.5.2. Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP16	64 1's and 0's	No de-emphasis or pre-shoot. Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.

USB 3.1 Link Turn-on Sequence

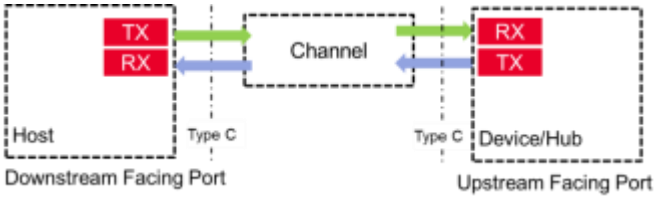
LTSSM states:



Testing USB 3.1 TX

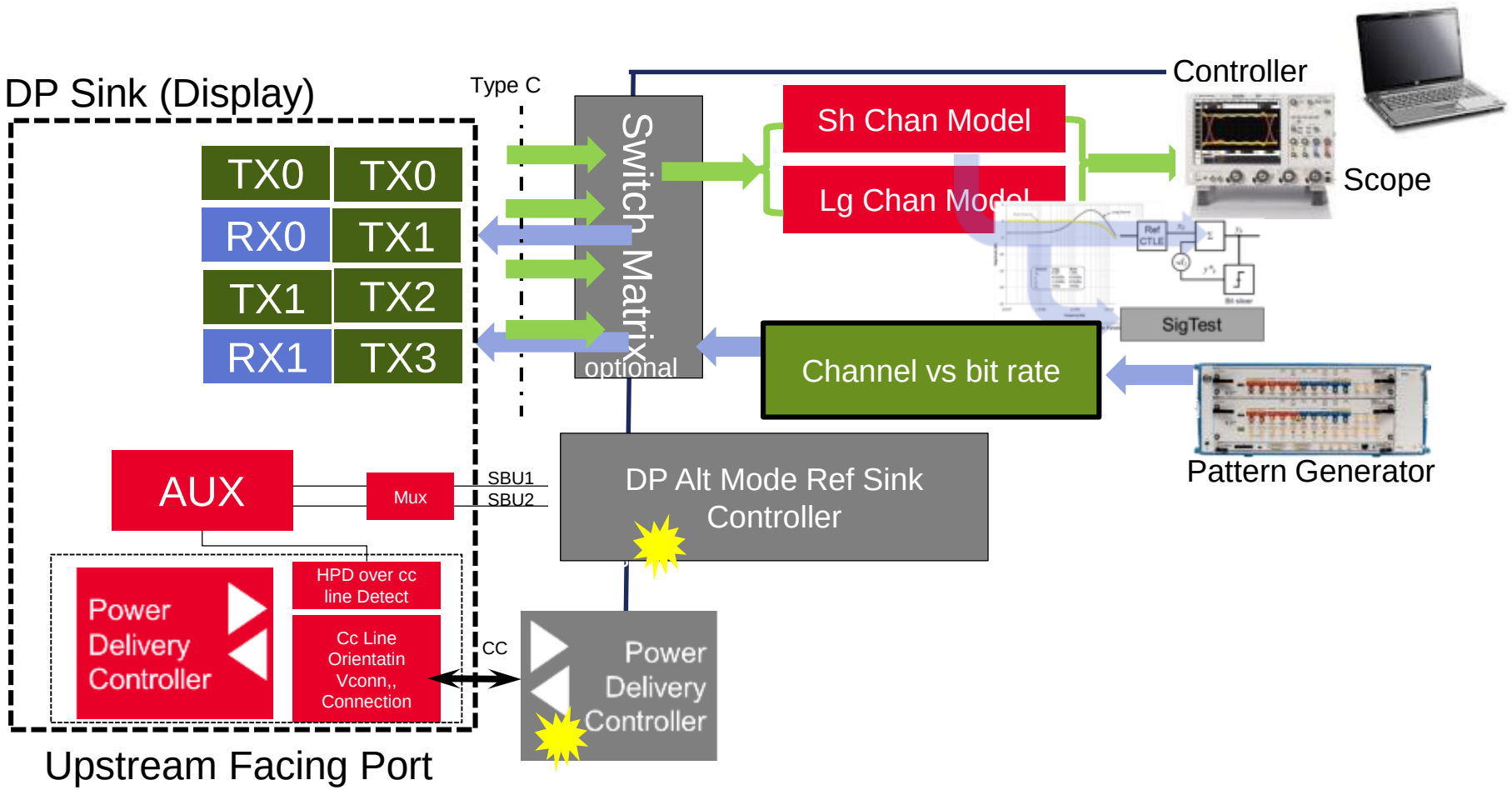


Testing USB 3.1 TX **w/Type C**

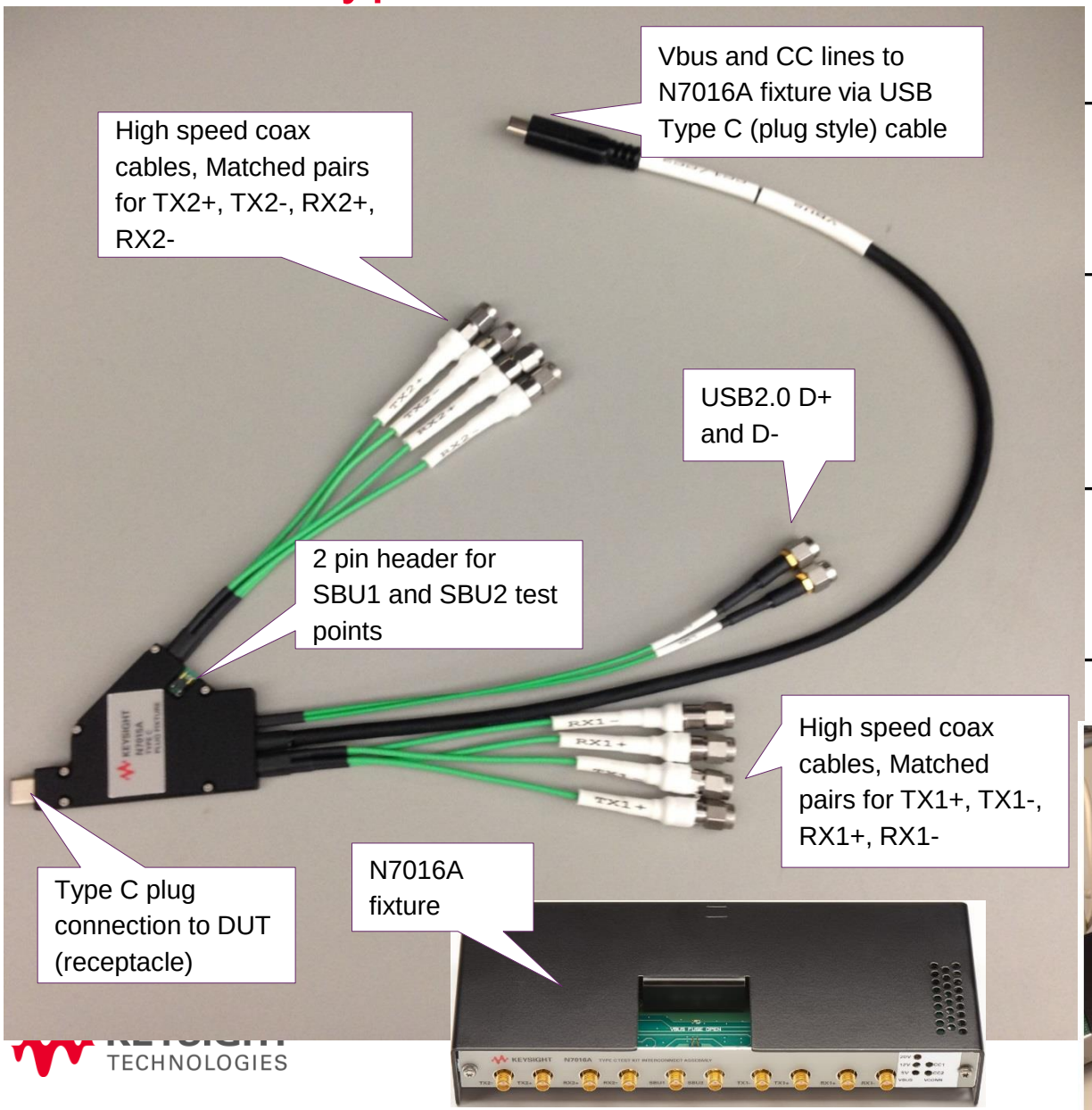


PING LFPS
Toggles CMM

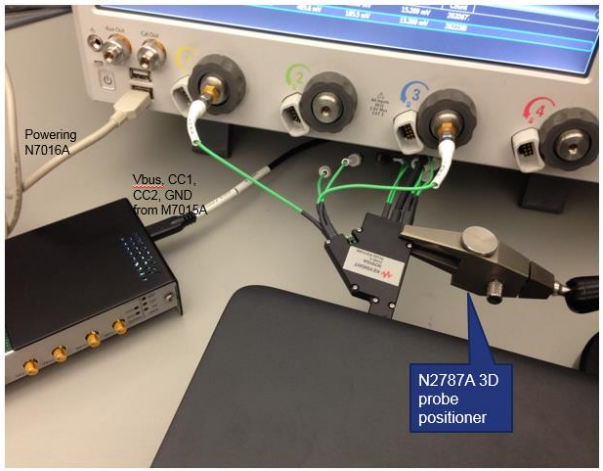
Testing USB 3.1 & DisplayPort TX **w/Type C**



N7015A Type C Test Fixture



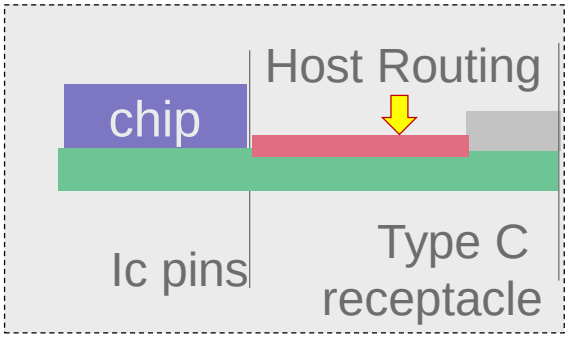
- High speed (TX/RX) and D+/D- lanes to scope through coax cables
- N7015A de-embedding models will be created and integrated in to compliance applications and Infiniium baseline software
- Power and Control signals to low speed N7016A fixture though type C cable
- View SBU1/2 signals

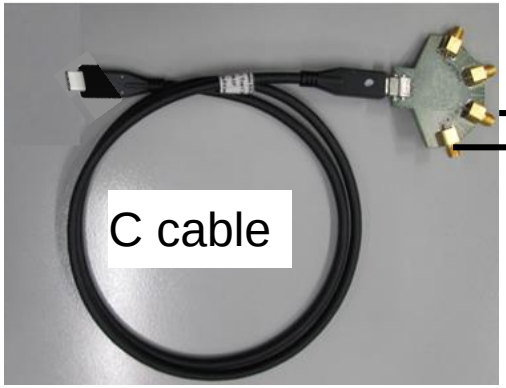


USB3.1 Transmitter Testing

SSSTest

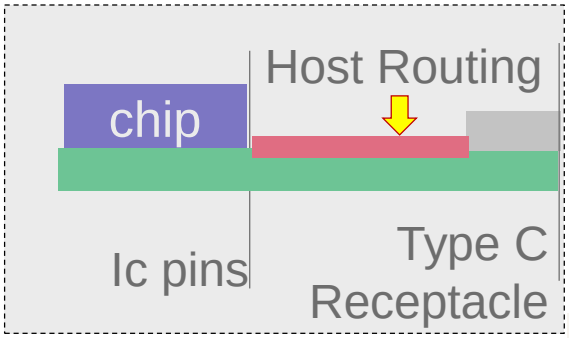
- **Superspeed Type C**

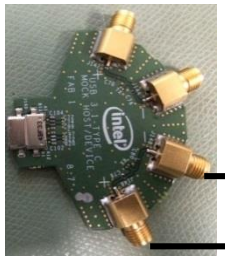




Mathematically Embed
Device Routing Model
+ CTLE and DFE
(Sigtest or Keysight)

OR

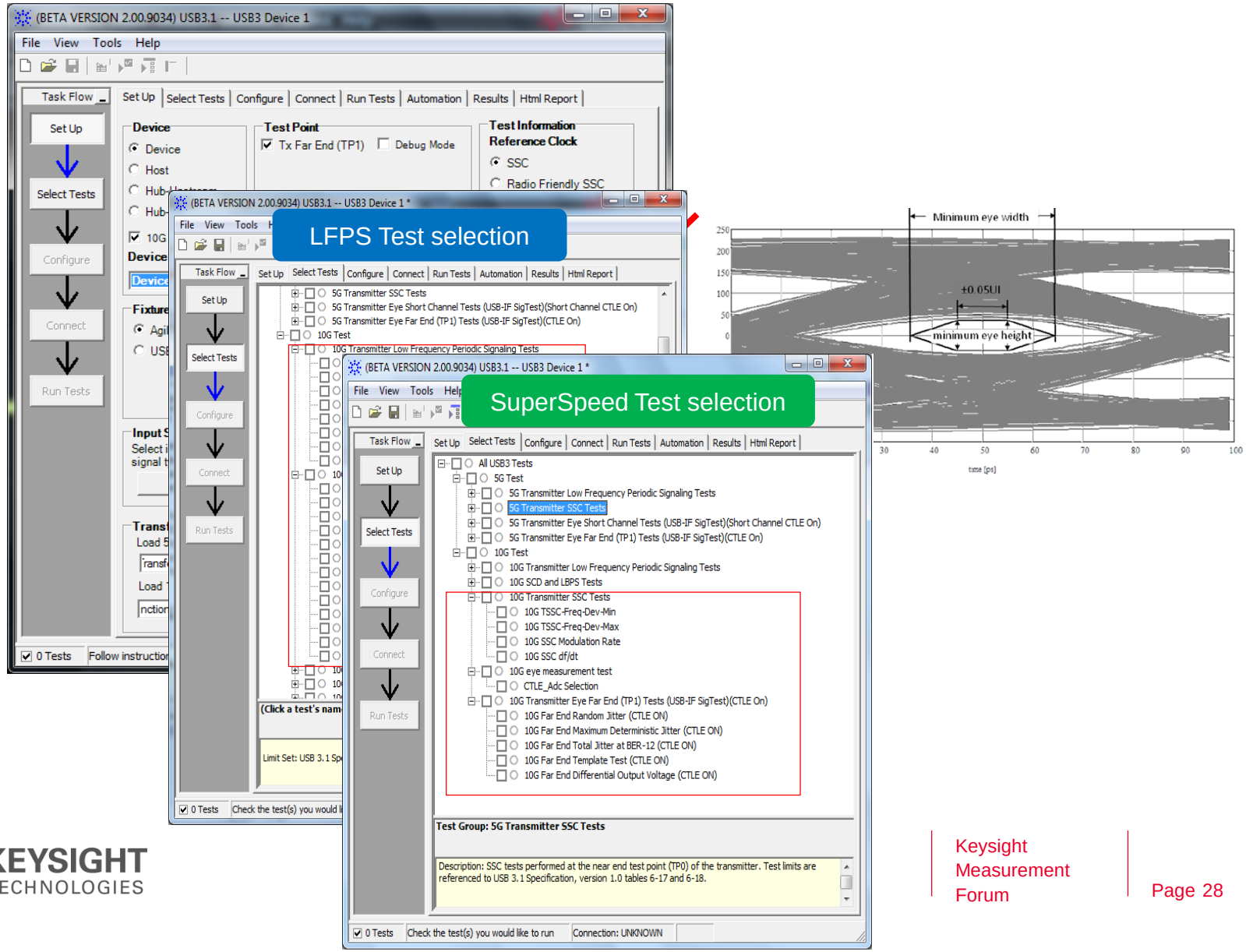




Mathematically Embed
C cable model
+ Device Routing Model
+ CTLE and DFE
(Sigtest or Keysight)

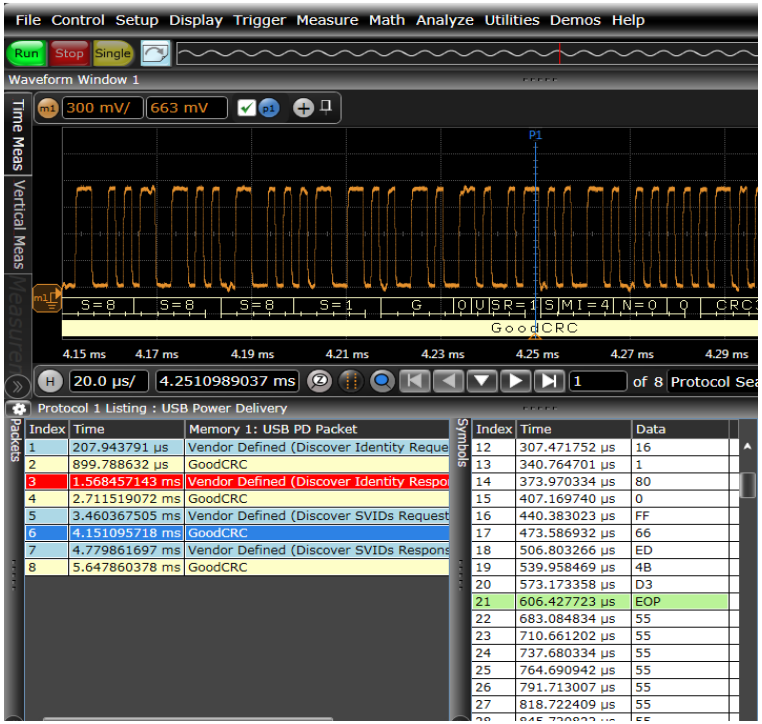
Testing USB3.1 Transmitters

U7243B Compliance SW



N8821A/B USB 3.1 Gen1/Gen2 Protocol Trigger & Decode

- USB 3.1 Gen1 and Gen 2 protocol decode in less than 30 seconds
- Integrated software-based protocol-level triggers
- Save time and eliminate errors by viewing packets at the protocol level
- Use time-correlated views to quickly troubleshoot serial protocol problems back to their timing or signal integrity root cause



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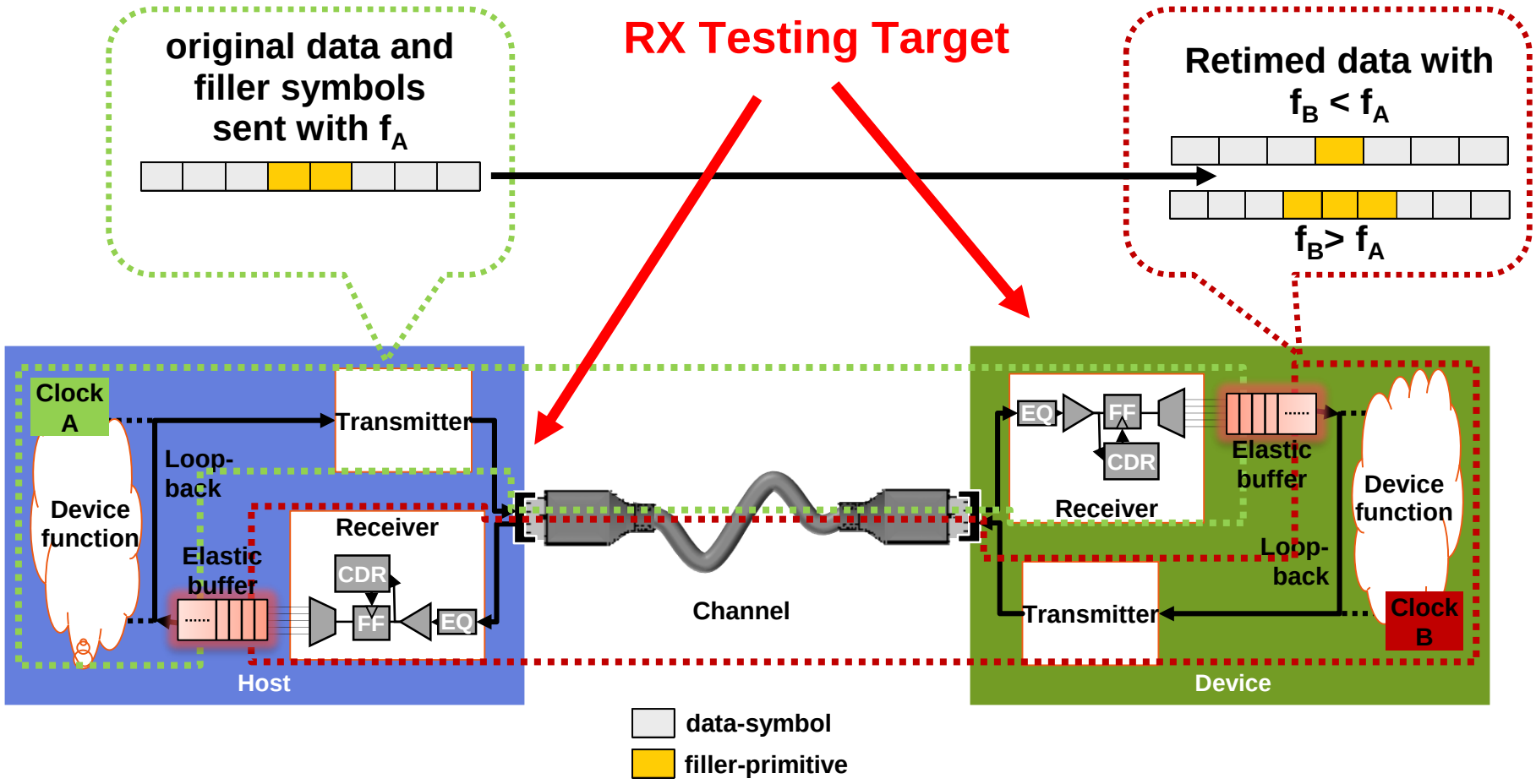
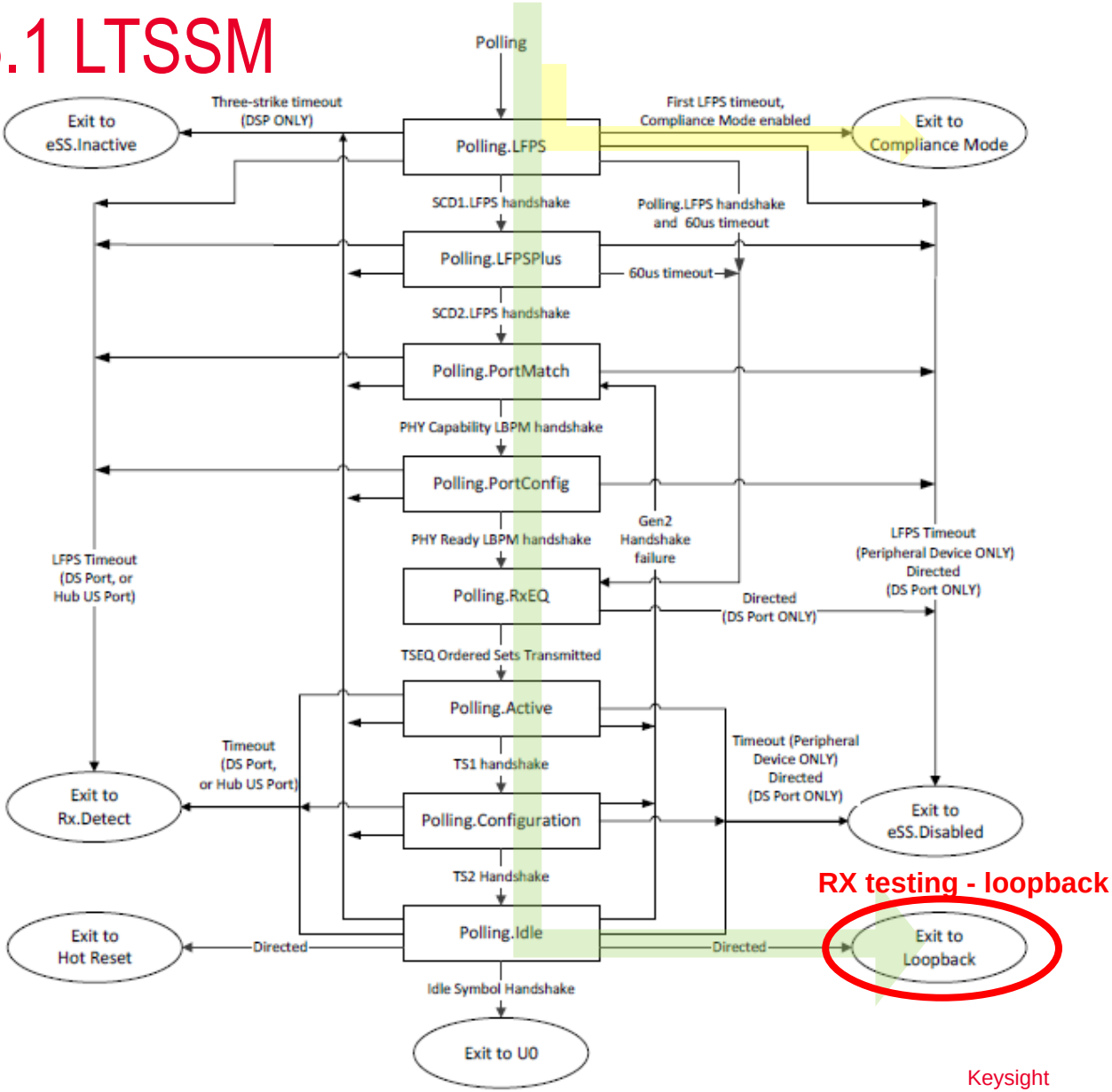
- USB3.1 Transmitter Test solution
- **USB3.1 Receiver Test Solution**
- Summary

USB 3.1 Fundamental Setup

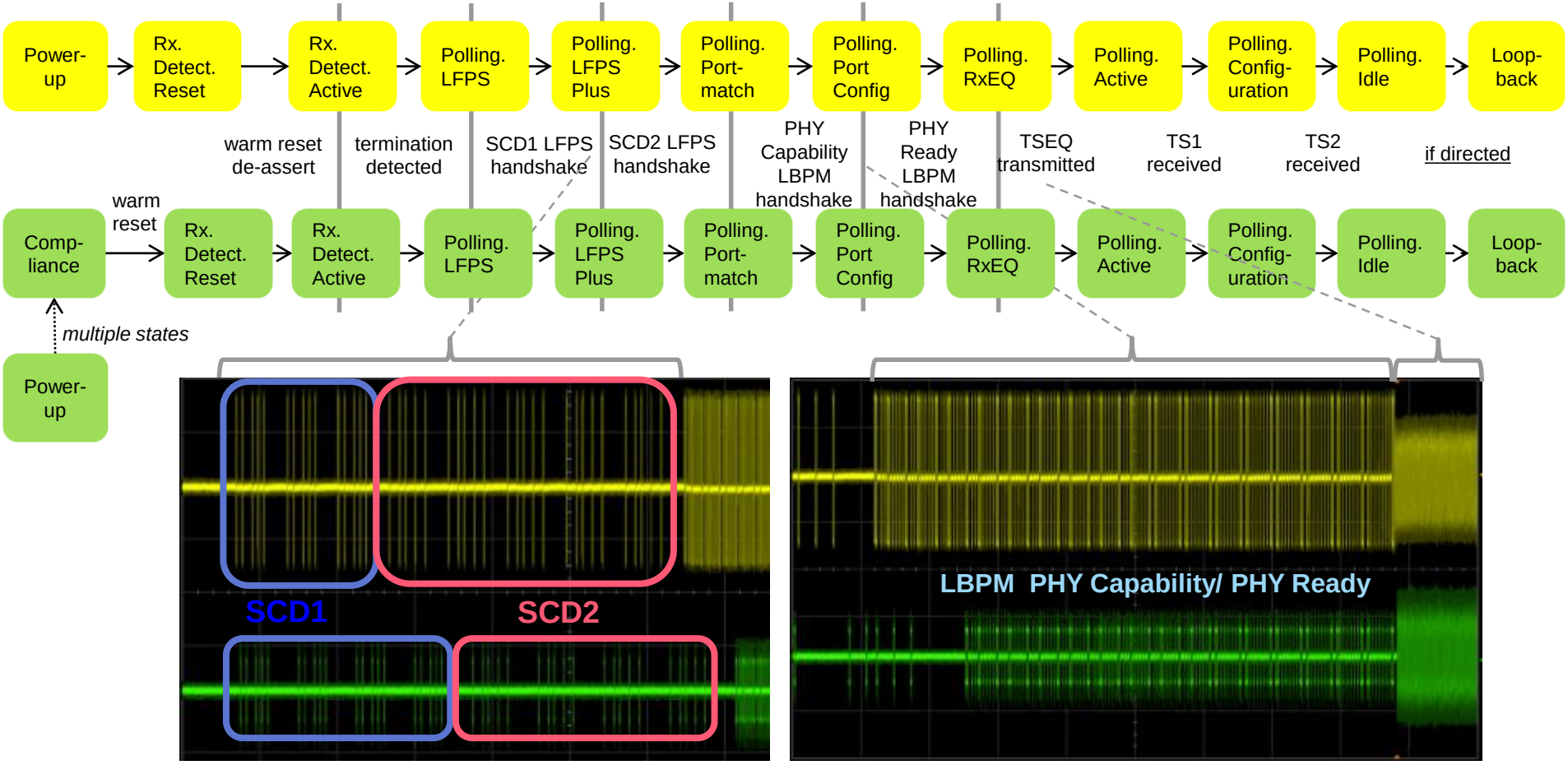


USB 3.1 LTSSM

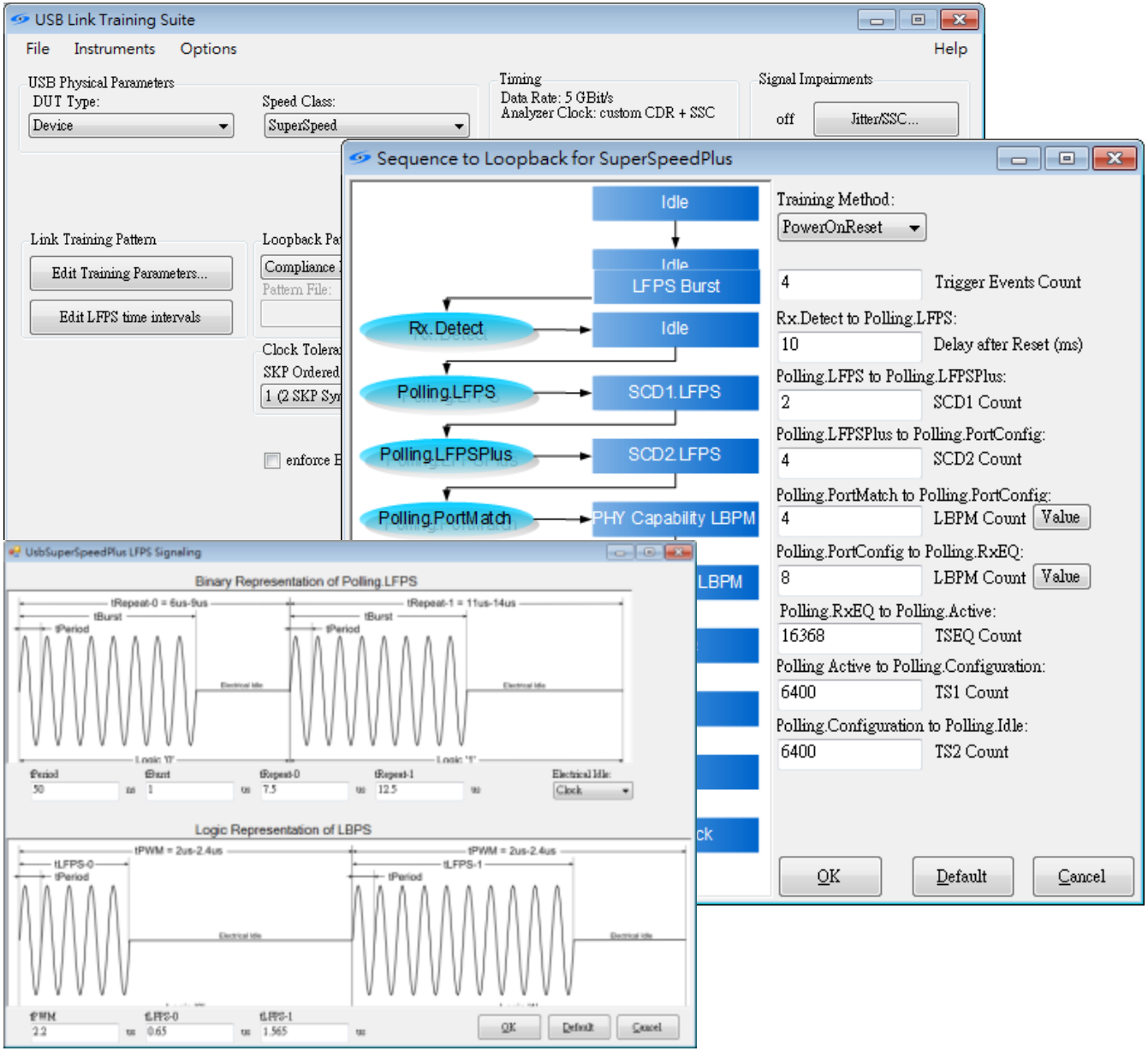

Polling
Polling.LFPS
Three-strike timeout (DSP ONLY)
Exit to eSS.Inactive
First LFPS timeout, Compliance Mode enabled
Exit to Compliance Mode
SCD1.LFPS handshake
Polling.LFPS handshake and 60us timeout
Polling.LFPSPlus
60us timeout
SCD2.LFPS handshake
Polling.PortMatch
PHY Capability LBPM handshake
Polling.PortConfig
PHY Ready LBPM handshake
Gen2 Handshake failure
LFPS Timeout (DS Port, or Hub US Port)
LFPS Timeout (Peripheral Device ONLY) Directed (DS Port ONLY)
Polling.RxEQ
Directed (DS Port ONLY)
TSEQ Ordered Sets Transmitted
Polling.Active
Timeout (DS Port, or Hub US Port)
TS1 handshake
Timeout (Peripheral Device ONLY) Directed (DS Port ONLY)
Exit to Rx.Detect
Polling.Configuration
Exit to eSS.Disabled
TS2 Handshake
RX testing - loopback
Exit to Hot Reset
Directed
Polling.Idle
Directed
Exit to Loopback
Idle Symbol Handshake
Exit to U0

Typical USB 3.1 Link Turn-on Sequence

LTSSM states:



Loopback Training – USB 3.1 LTS tool



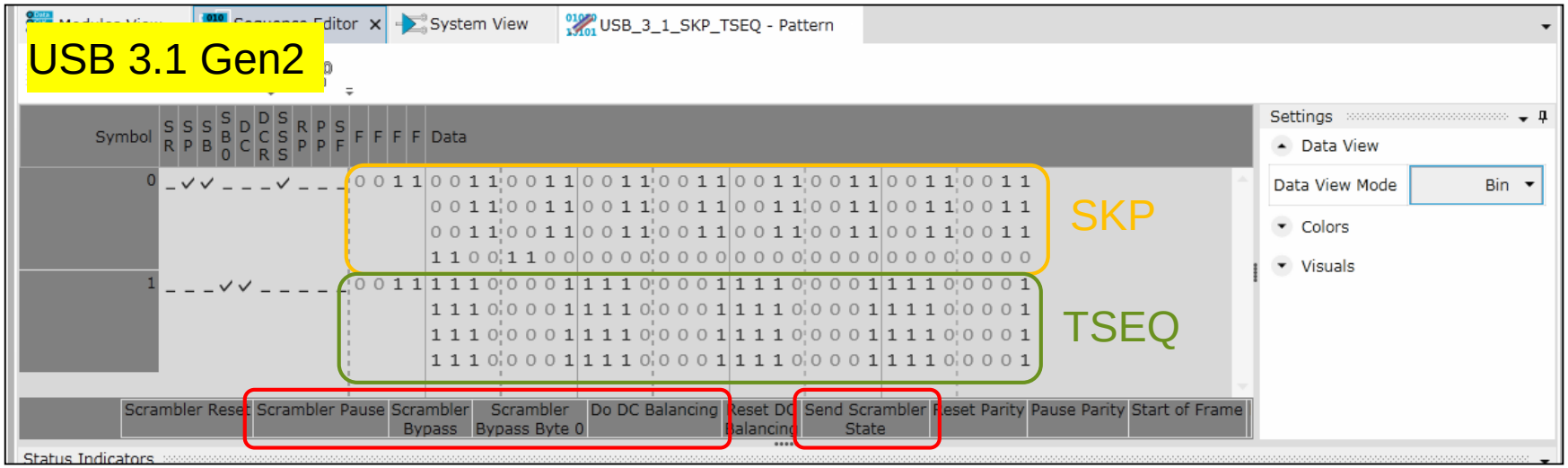
- USB Link Training Suite is a trainings sequence generation tool for USB3.1 Gen1/2
- Easy manipulation of
  - SCD1/SCD2/LBPM cycles
  - TSEQ count
  - TS1 count
  - TS2 count
- LFPS parameters adjustment:
  - tPeriod, tBurst, tRepeat, tPWM….
- Choice of:
  - Power On sequence
  - Warm Reset sequence

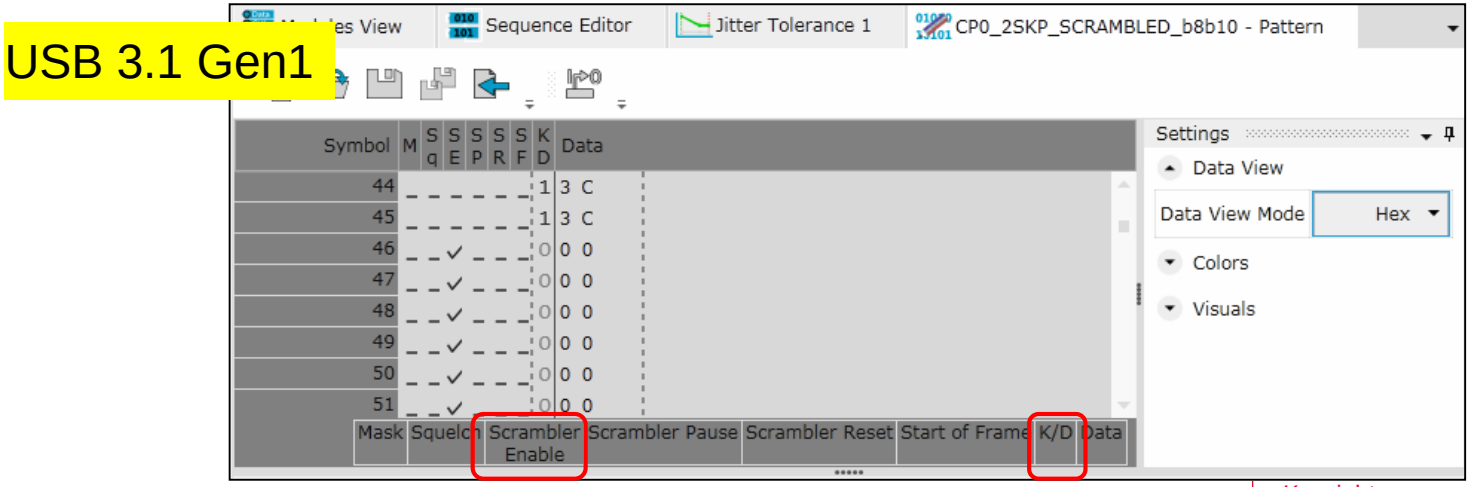
USB 3.1 Gen 2 coding - 128b/132b Coding

- 4 bit header to avoid link reset problems from PCIe 8G
- 0011 marks a data block and 1100 a command block
- **SYNC block** is used to reset scrambler and to gain block alignment
- Same scrambler polynomial as PCIE 8G:
  $G(X) = X^{23} + X^{21} + X^{16} + X^{8} + X^{5} + X^{2} + 1$
  Block header bypasses scrambler and does not advance scrambler
- Command block scrambler rules
  - TS1, TS2, TSEQ
    - symbol 0 bypasses but advances scrambler
    - symbols 1 to 13 are scrambled
    - symbols 14 and 15 bypass scrambler but advance scrambler if used for DC balance otherwise they are scrambled
  - SKP OS bypasses scrambler and does not advance scrambler
  - SDS OS bypasses scrambler but advance scrambler
- All blocks are 132 bit long except SKP OS which can be shorter or longer
- SKP END symbol is used to regain block alignment

M8000 HW coding, Scrambling capability

Pattern editor support 8b/10b & 128b/132b coding





Receiver Jitter Tolerance curve

Gen1 vs Gen2

- Rx Jtol RJ & Tx EQ updated by ECN
- Gen 2 define **7 SJ points** in spec.
- Gen 1 define 5 SJ points in Spec, but 8 points in CTS

Symbol	Parameter	Gen 1	Gen 2	Units
f1	Tolerance corner	4.9	7.5	MHz
J_{Rj}	Random Jitter	0.0121	0.0100	UI rms
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	0.141	UI p-p
J_{Pj_500kHZ}	Sinusoidal Jitter	2	2.56	UI p-p
J_{Pj_1Mhz}		1	1.28	UI p-p
J_{Pj_2MHz}		0.5	0.64	UI p-p
J_{Pj_4MHz}		N/A	0.32	UI p-p
J_{Pj_f1}		0.2	0.17	UI p-p
J_{Pj_50MHz}		0.2	0.17	UI p-p
J_{Pj_100MHz}		N/A	0.17	UI p-p
V_full_swing	Transition bit differential voltage swing	0.75	TBD	V p-p
V_EQ_level	Non transition bit voltage (equalization)	-3	Pre=2.2 Post= -3.1	dB

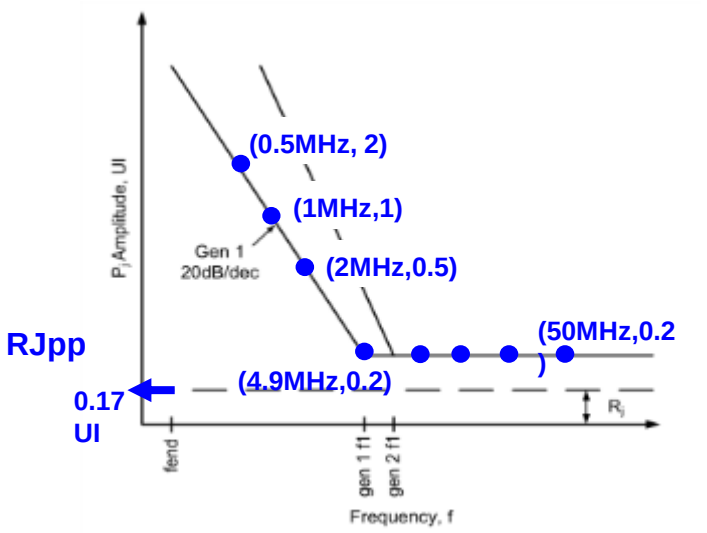


Figure 6-28. Jitter Tolerance Curve

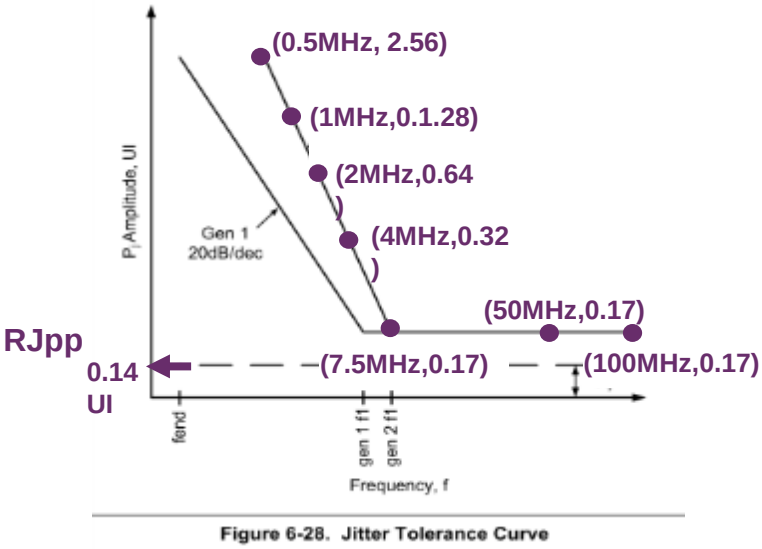


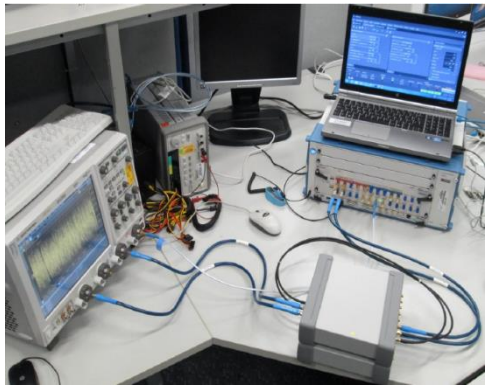
Figure 6-28. Jitter Tolerance Curve

USB 3.1 gen2 10Gb/s

RX Calibration Procedure

Before Channel Cal Steps:

- Channel Verification
- De-emphasis signal calibration before channel
- Calibration of RJ before channel
- Calibration of SJ before channel



23dB Channel Cal Steps:

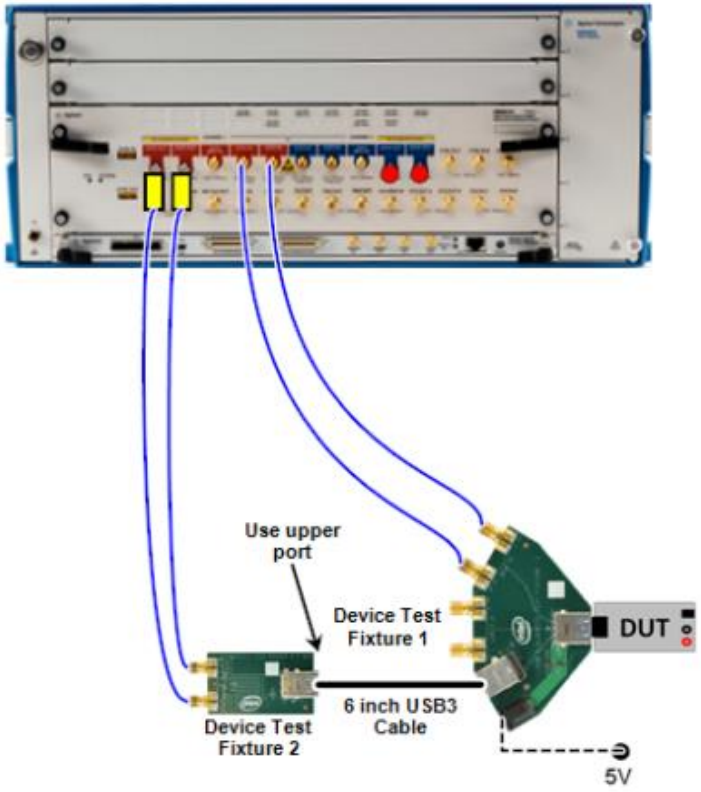
- Eye width and eye height calibration after a 23dB channel
- Pre-calibration with fixed de-emphasis to select correct CLB, measure is EH
- EW tuning by adjusting de-emphasis and if necessary SJ2
- EH fine tuning by adjusting amplitude

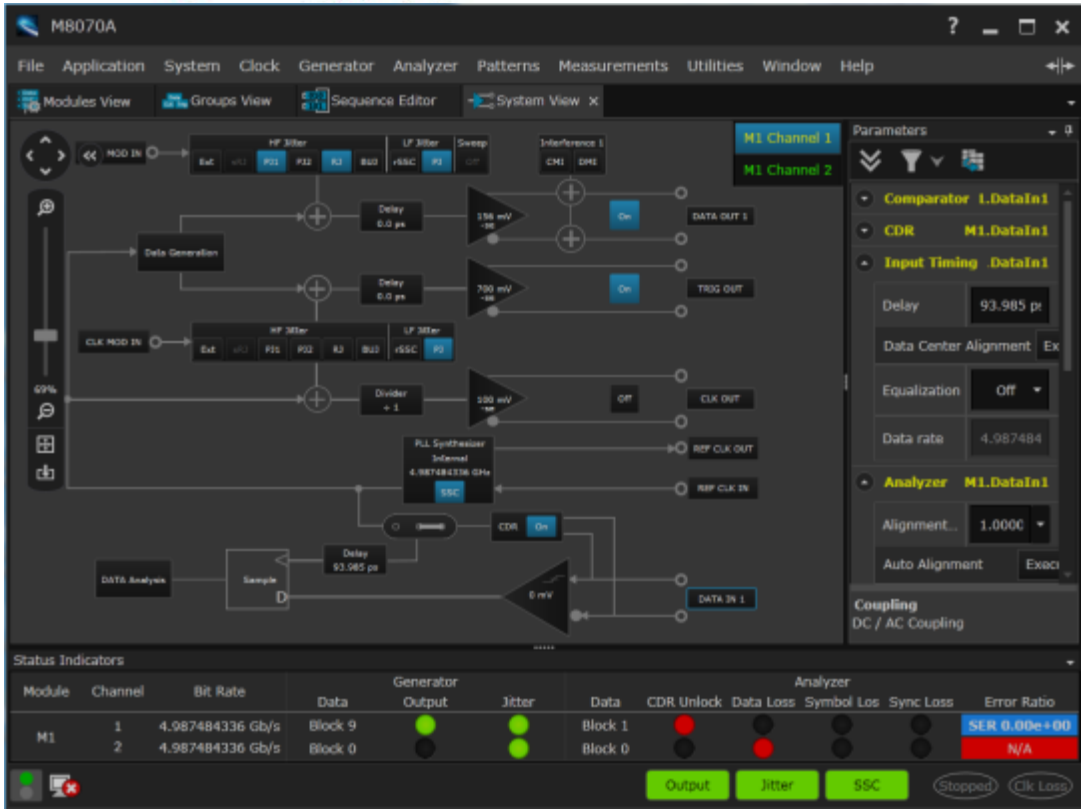
USB 3.1 Gen 2 N5990A Rx Auto Calibration SW

RX Cal Targets

Parameter	Min	Nominal	Max	Unit	SigTest	
					Technology	Template
Calibration channel	22.5	23	23.5	dB@5GHz	N/A	N/A
Test	14	14.5	15	dB@5GHz	N/A	N/A
V_{pp}		800		mV	N/A	N/A
Pre-shoot	2.1	2.2	2.3	dB	N/A	N/A
De-emphasis	-3.0	-3.1	-3.2	dB	N/A	N/A
RJ (Random Jitter)	0.9	1.0	1.0	ps RMS	usb_3_10gb	USB_3_10Gb_Rj_Sj_CAL
SJ (Sinusoidal Jitter) **500kHz** **1MHz** **2MHz** **4MHz** **7.5MHz** **10MHz** **20MHz** **33MHz** **50MHz** **100MHz**	 4.284 1.827 0.873 0.333 0.153 0.153 0.153 0.153 0.153 0.153	 4.76 2.03 0.87 0.37 0.17 0.17 0.17 0.17 0.17 0.17	 4.76 2.03 0.87 0.37 0.17 0.17 0.17 0.17 0.17 0.17	UI pp	usb_3_10gb	USB_3_10Gb_Rj_Sj_CAL
Eye Height	70 (10^{-6})	70 (10^{-6})	75 (10^{-6})	mV	usb_3_10gb	USB_3_10_CP9_RX_CAL_CTLE_N5dB
Eye Width	48 (10^{-6})	48 (10^{-6})	50 (10^{-6})	ps	usb_3_10gb	USB_3_10_CP9_RX_CAL_CTLE_N5dB

USB 3.1 Gen1/Gen2 M8020A Receiver Test Setup





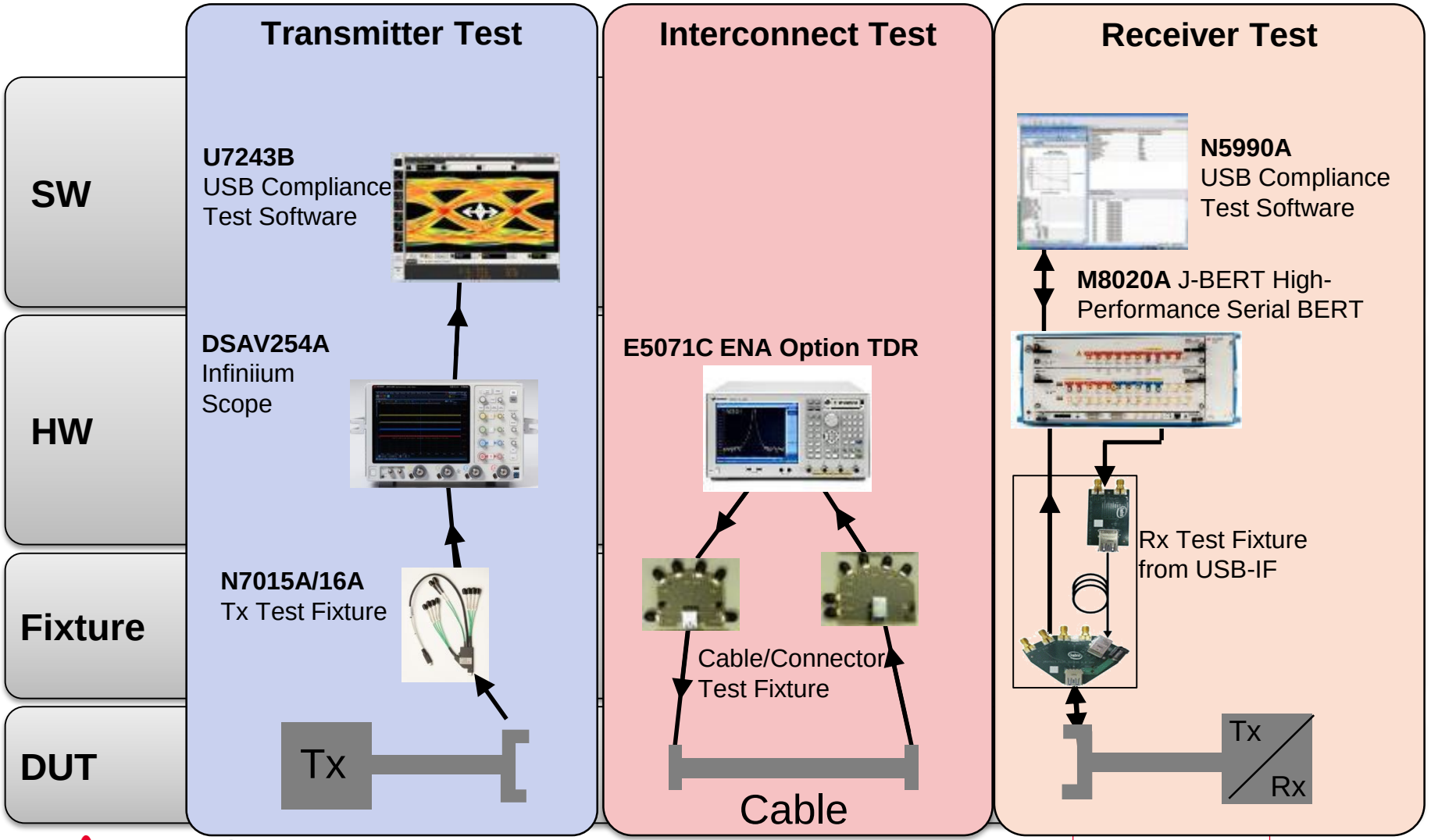
Key capabilities:

- Analysis of coded & retimed data
- Support of **8b/10b and 128b/132b HW** coding and decoding as well as HW scrambling
- Generates calibrated stress conditions for RX test (SSC, SJ, RJ, De-emphasis, ISI)
- **Emulate LFPS 3-level signals** with built-in electrical idle for loopback training and via channel
- **Integrated Link Training, Tx Eq, Noise Impairment, Variable ISI, Receiver Equalizer/Eye Opener**

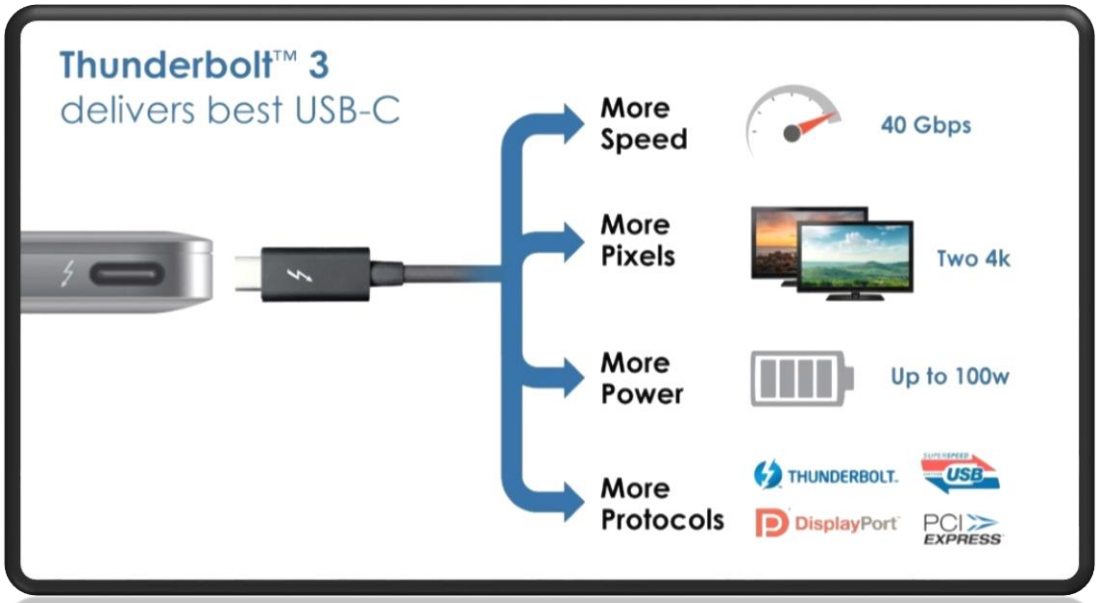
Agenda

- Introduction to the USB Type C Connector
- USB3.1 Type C Test challenge
- USB3.1 Transmitter Test solution
- USB3.1 Receiver Test Solution
- **Summary**

Keysight USB 3.1 Type-C Total Test Solution



Keysight USB Type-C PD(Power delivery) solution



KEYSIGHT TECHNOLOGIES

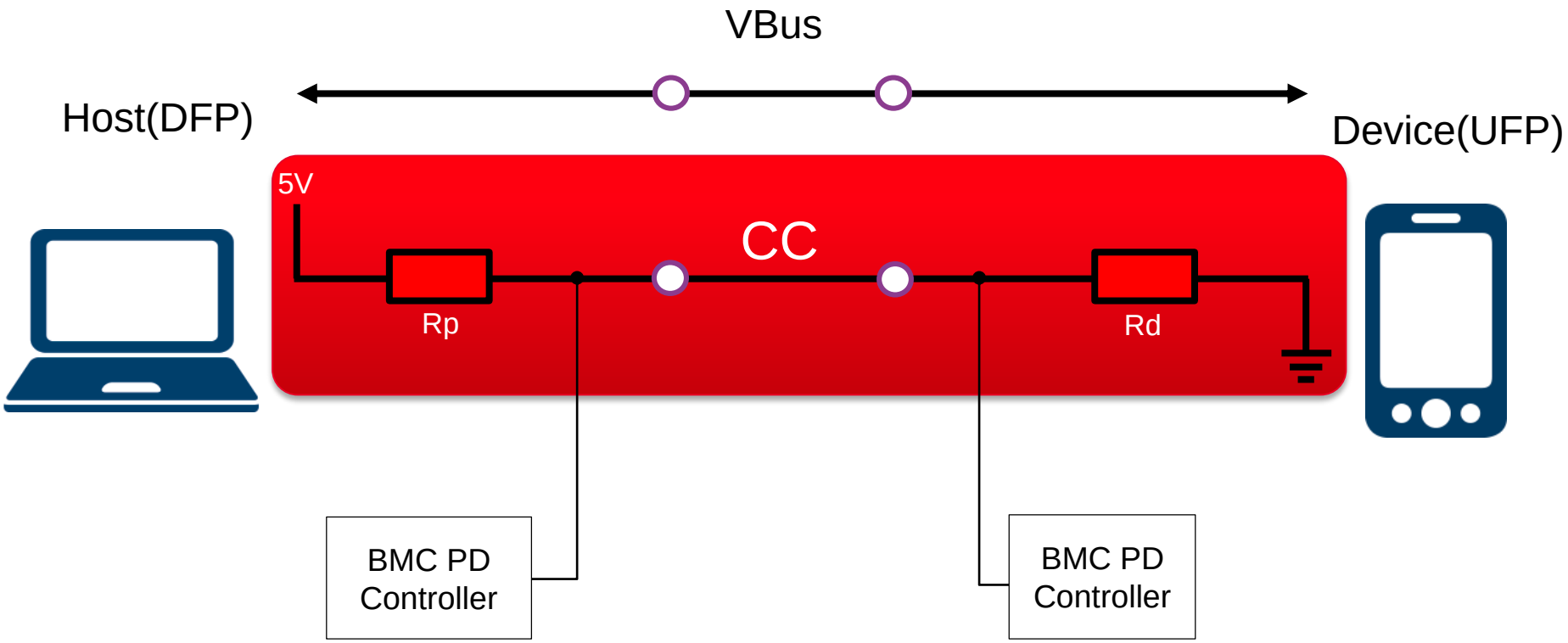
Agenda

- Power Delivery
- PD protocol solution
  - N8837A Keysight USB-PD protocol decoding/triggering solution
  - N8840A Keysight USB-PD electrical & protocol compliance
- N8840A PD Compliance solution
  - eMark Cable
  - Power delivery Provider/Consumer and Dual Role Power

The familiar USB "trident" logo gets new meanings. Overlaid on a battery, it means the USB port is good for charging or running devices that need lots of electrical power. The SS denotes the 5Gbps data-transfer rate of USB 3.0; SS and 10 denotes the 10Gbps speed of USB 3.1.

Power Delivery

Configuration channel



Rp : Pull up Resister
Rd : Pull down Register

Power Delivery

Type-C Cable Type

– Standard(Unmarked) Cables (Limited to 3A@20V peration)

  • USB Full-Featured Type-C cable

  • USB 2.0 features only Type-C cable

  • USB Type-C captive cable

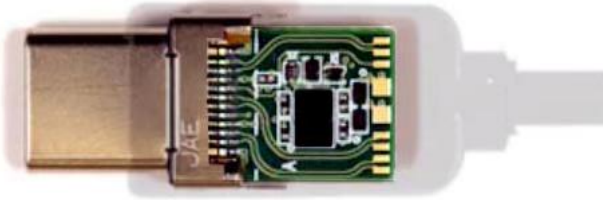
– Electronically-Marked(eMarker) Cables(Required for 5A@20V operation

  • USB Full-featured Type-C cable

  • USB 2.0 featured Type-C cable

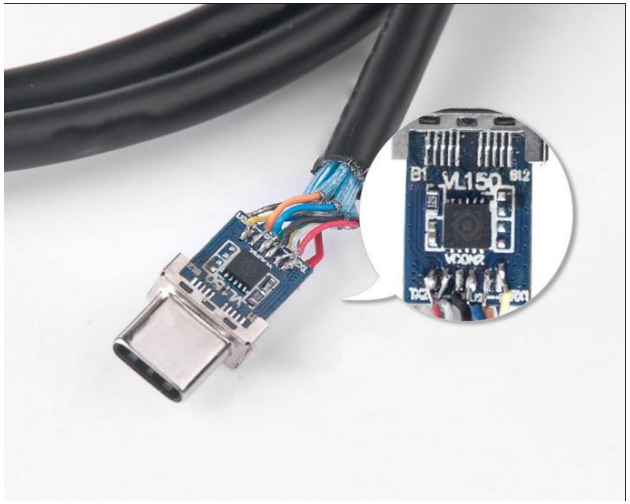
    - Passive cable : electrical marked cable with no signal conditioning chip

    - Active cable : electrical marked cable with signal conditioning chip

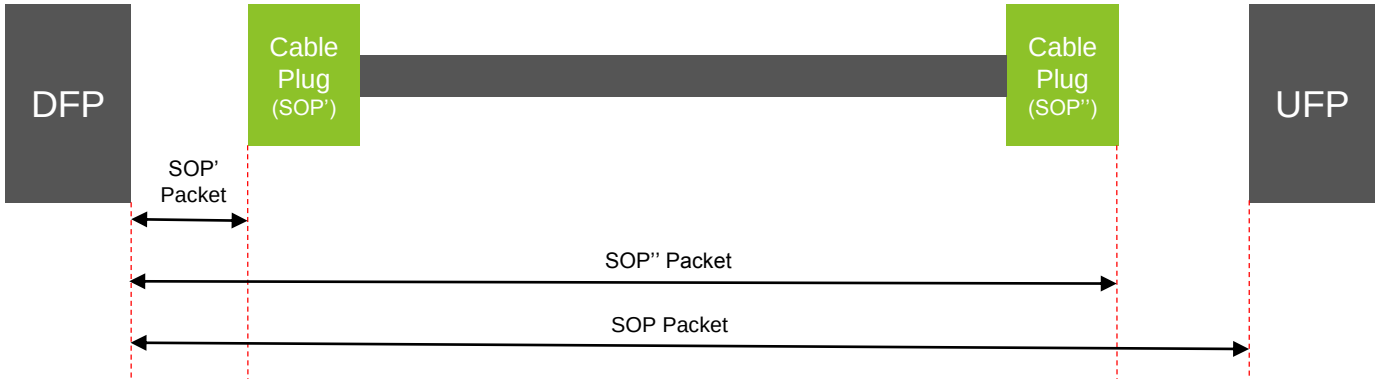


USB-PD ‘eMarker’ Cable

Active cable



- eMarker cable has chip inside of cable
- Chip active power received from Vconn
- Can support 20V, 5A
- To communicate with DFP, it use SOP’ (SOP prime) or SOP’’(SOP double prime)



SOP* Communication

Image source : http://www.apple-usb.com/index.php/product/index/id/48.html

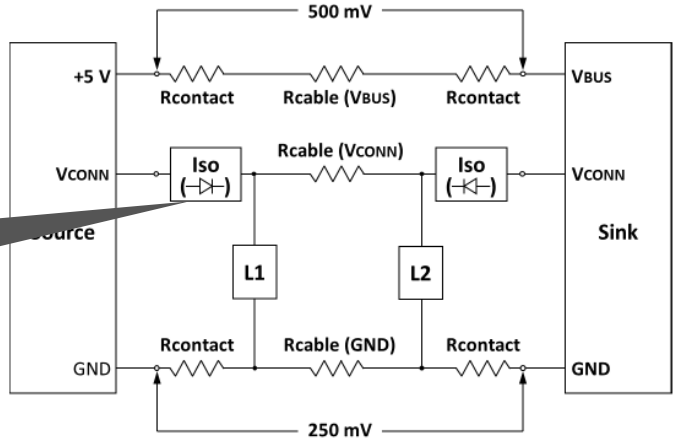
USB Type-C power

VBUS and VCONN Power

- VBUS
  - Supplied from Source to Sink
  - Voltage range : 5V ~ 20V
  - Current : 1.5A ~ 5A
- VCONN
  - eMarker Cable and VCONN Powered accessory ONLY
  - Voltage : 5V(Sourced by DFP)

Vconn power blocked by powered cable

Figure 4-2 Cable IR Drop for powered cables



Power Delivery

Essential Acronym

DFP	Downstream Facing Port (data role –PD and USB)
UFP	Upstream Facing Port (data role – PD and USB)
DRP	Dual-Role Power, Capability of operating as either a Source or Sink
DRD	Dual-Role Device, Capability of operating as either a DFP or UFP
Provider	A capability of a PD Port (typically a Host, Hub, or Wall Wart DFP) to source power over the power conductor (power role)
Consumer	The capability of a PD Port (typically a Device's UFP) to sink power from the power conductor (power role)
SOP/EOP	Start of Packet, End of Packet
VDM/VDO	Vendor Defined Message/Vendor Data Object
BIST	Built In Self-Test, Power Delivery testing mechanism for PHY layer
CC	Configuration channel

Agenda

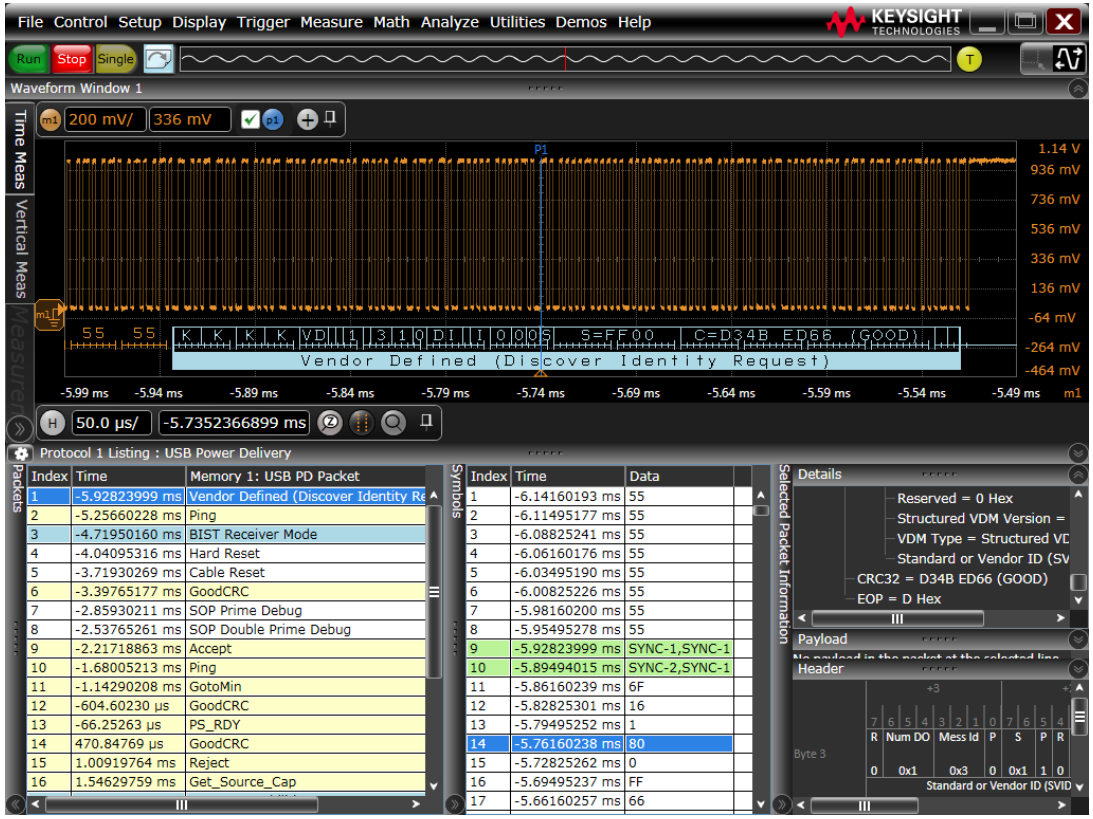
- Power Delivery
- PD protocol solution
  - N8837A Keysight USB-PD protocol decoding/triggering solution
  - N8840A Keysight USB-PD electrical & protocol compliance
- N8840A PD Compliance solution
  - eMark Cable
  - Power delivery Provider/Consumer and Dual Role Power

The familiar USB "trident" logo gets new meanings. Overlaid on a battery, it means the USB port is good for charging or running devices that need lots of electrical power. The SS denotes the 5Gbps data-transfer rate of USB 3.0; SS and 10 denotes the 10Gbps speed of USB 3.1.

KEYSIGHT TECHNOLOGIES

Power Delivery protocol solution

Keysight USB PD protocol triggering and decoding



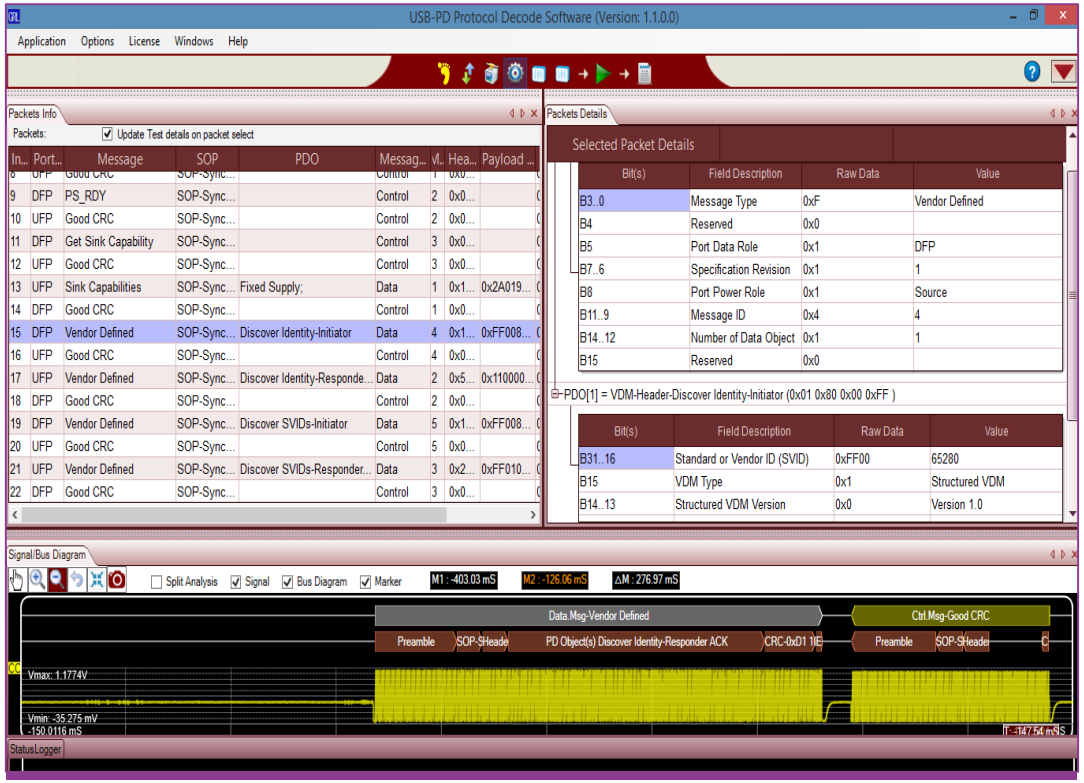
USB PD protocol decoding window example

USB PD CC and Vbus line signal

Hardware serial trigger in S-Series

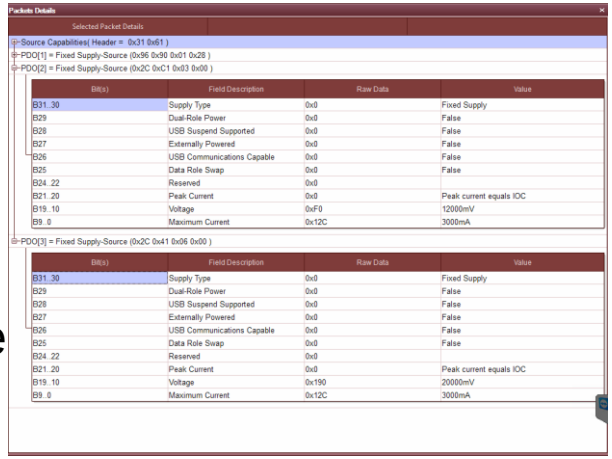
Power Delivery protocol solution

N8840A USB Type-C compliance test program and solution



Single shot of N8840A software as protocol decode

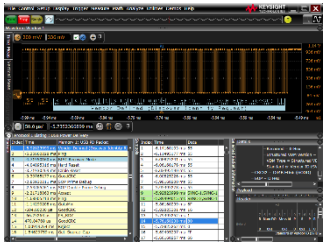
USB PD CC and Vbus line signal

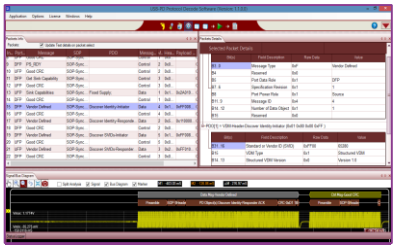


PD software decoding example

Power Delivery protocol solution

Quick Comparison





	N8837A USB-PD Protocol trigger and decode	N8840A USB-PD Electrical and protocol compliance
Trigger	Hardware based trigger on S-Series	No
Search	Yes	No
Decoded data processing time	Fast	Slow (save to storage and read again)
Segmented memory	Yes support	No
Compliance test	No(Debugging only)	Yes

Agenda

- Power Delivery
- PD protocol solution
  - N8837A Keysight USB-PD protocol decoding/triggering solution
  - N8840A Keysight USB-PD electrical & protocol compliance
- N8840A PD Compliance solution
  - eMark Cable
  - Power delivery Provider/Consumer and Dual Role Power

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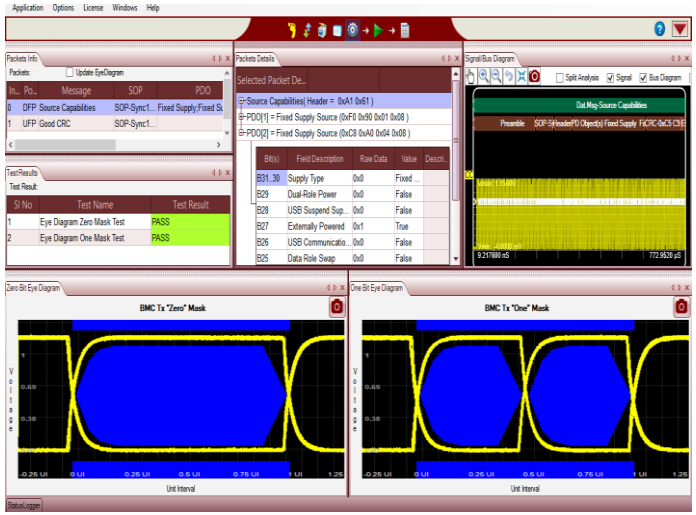
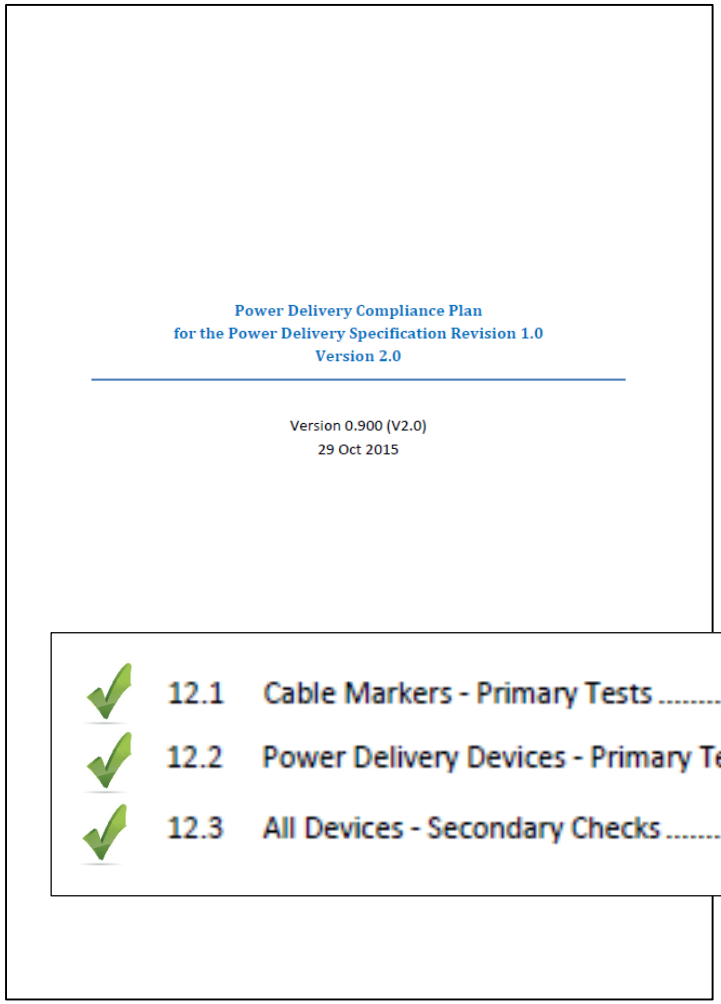
PD compliance test solution

N8840A USB Type-C PD compliance test software

- Runs on Windows based oscilloscopes
- Perform BMC-PHY Compliance tests
- Decodes USB-PD protocol
- Automates Compliance tests when used with Type-C test controller
- Developed by GRL(Granite River Lab)

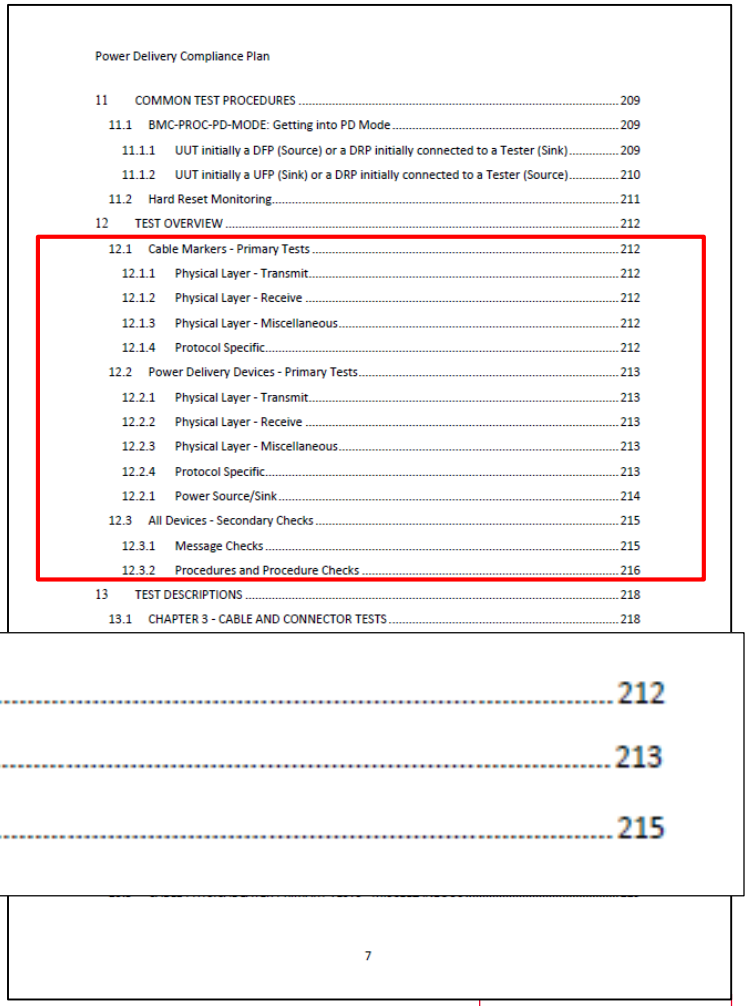


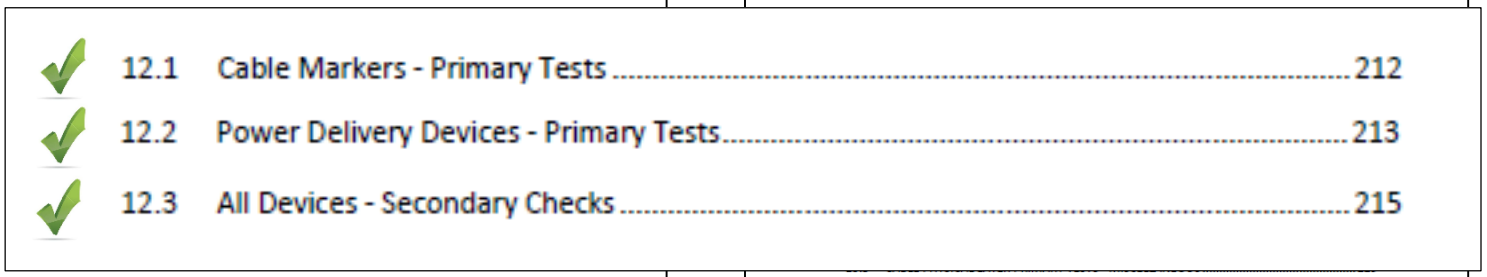
USB-PD Test type



Power Delivery Compliance Plan
for the Power Delivery Specification Revision 1.0
Version 2.0

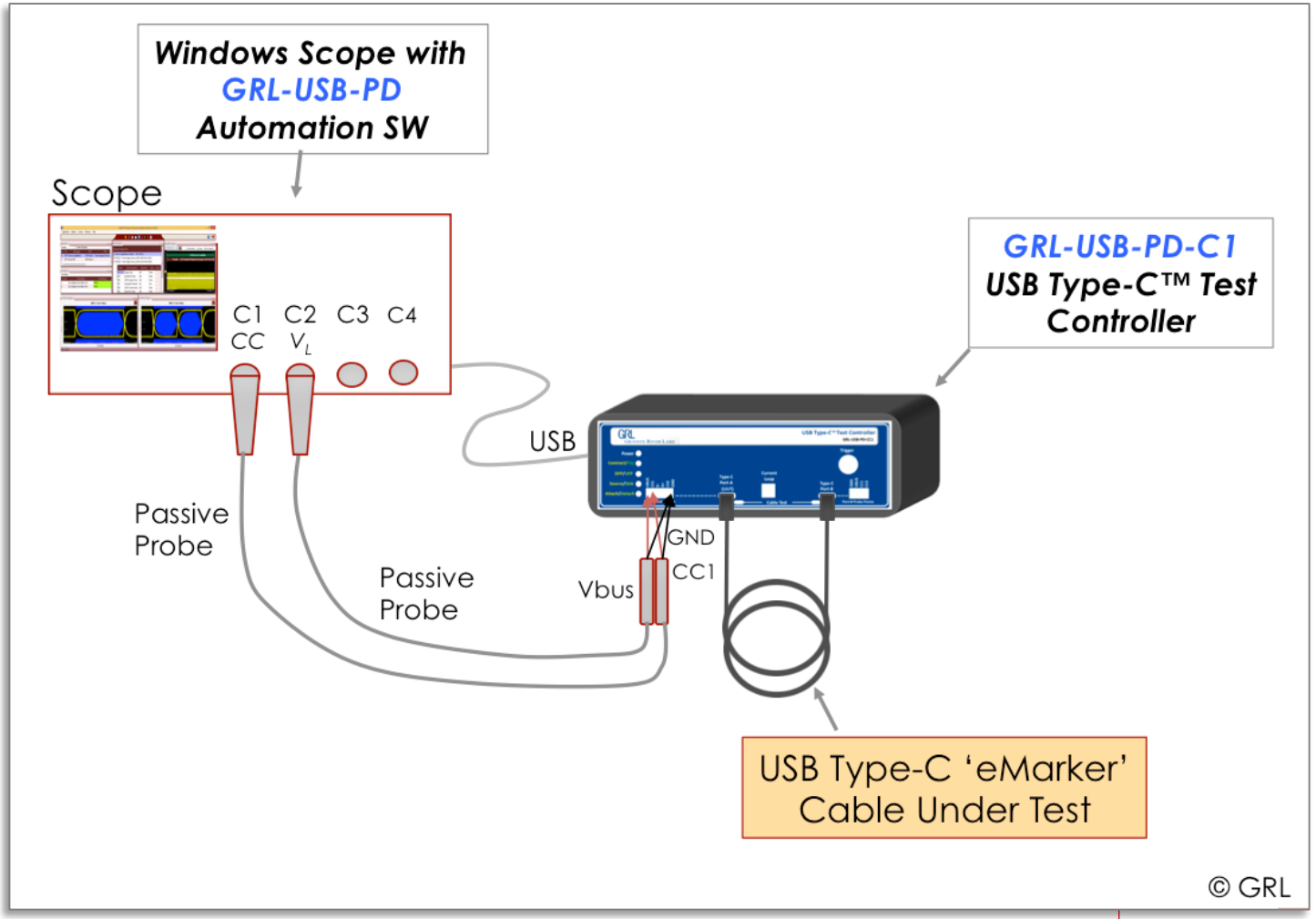
Version 0.900 (V2.0)
29 Oct 2015





USB-PD ‘eMarker’ cable

Test setup



USB-PD ‘eMarker’ cable

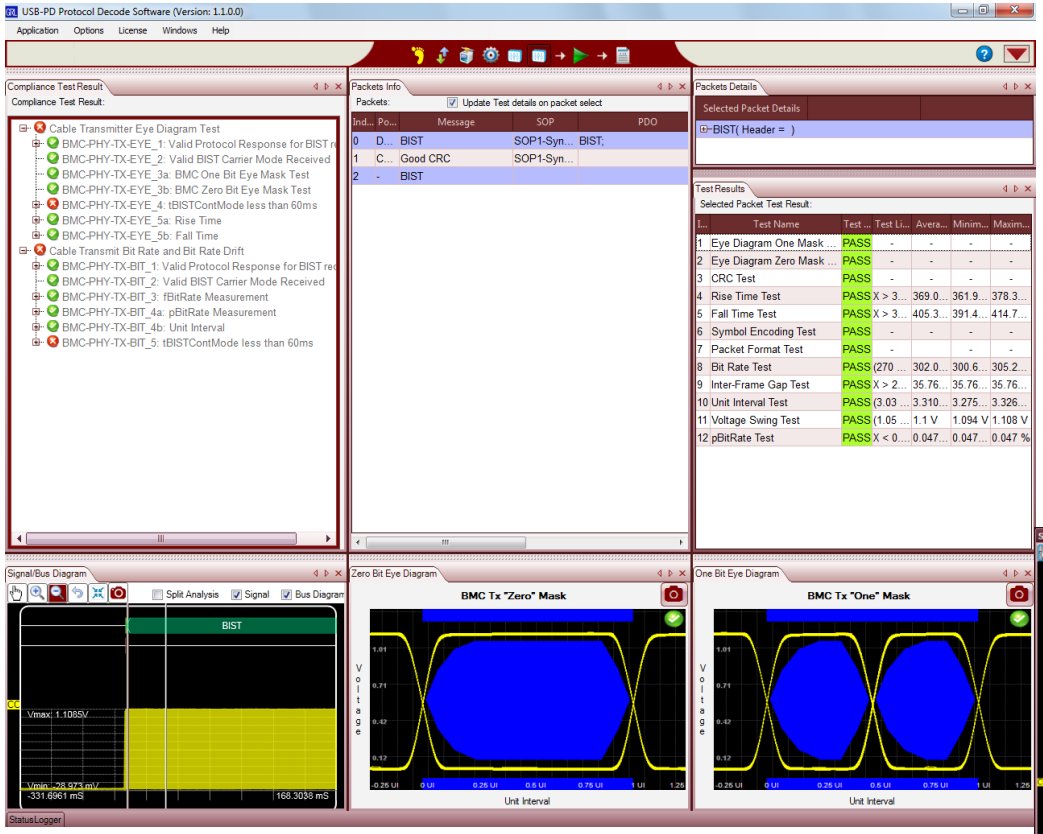
Tests

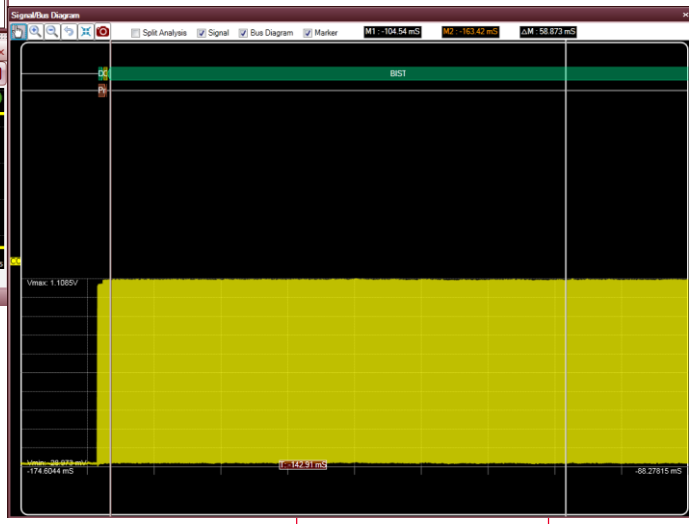
Test Group	Test Description	Test Name
	Primary Tests	
1	**Primary Cable Marker Tests**	
1.1	**CABLE PHYSICAL LAYER TESTS - TRANSMIT**	
TD 1.1.1	Cable Transmitter Eye Diagram Test (SOP Prime)	CAB-PHY-TX-EYE
TD 1.1.2	Cable Transmitter Eye Diagram Test (SOP Double Prime)	CAB-DP-PHY-TX-EYE
TD 1.1.3	Cable Transmit Bit Rate and Bit Rate Drift (SOP Prime)	CAB-PHY-TX-BIT
TD 1.1.4	Cable Transmit Bit Rate and Bit Rate Drift (SOP Double Prime)	CAB-DP-PHY-TX-BIT
1.2	**CABLE PHYSICAL LAYER TESTS - RECEIVE**	
TD 1.2.1	Cable Bus Idle Detection Test (SOP Prime)	CAB-PHY-RX-BUSIDL
TD 1.2.2	Cable Bus Idle Detection Test (SOP Double Prime)	CAB-DP-PHY-RX-BUSIDL
TD 1.2.3	Cable Receive Interference Rejection Test (SOP Prime)	CAB-PHY-RX-INT-REJ
TD 1.2.4	Cable Receive Interference Rejection Test (SOP Double Prime)	CAB-DP-PHY-RX-INT-REJ
1.3	**CABLE PHYSICAL LAYER TESTS - MISCELLANEOUS**	
TD 1.3.1	Cable Termination Impedance Test (SOP Prime)	CAB-PHY-TERM
TD 1.3.2	Cable Termination Impedance Test (SOP Double Prime)	CAB-DP-PHY-TERM
TD 1.3.3	Cable PHY Level Message Test (SOP Prime)	CAB-PHY-MSG
TD 1.3.4	Cable PHY Level Message Test (SOP Double Prime)	CAB-DP-PHY-MSG
1.4	**CABLE PROTOCOL SPECIFIC TESTS**	
TD 1.4.1	Cable ID Checks	CAB-PROT-DISCOV

Source : USB-PD Test plan Rev 0.9

USB-PD ‘eMarker’ cable

Test Result

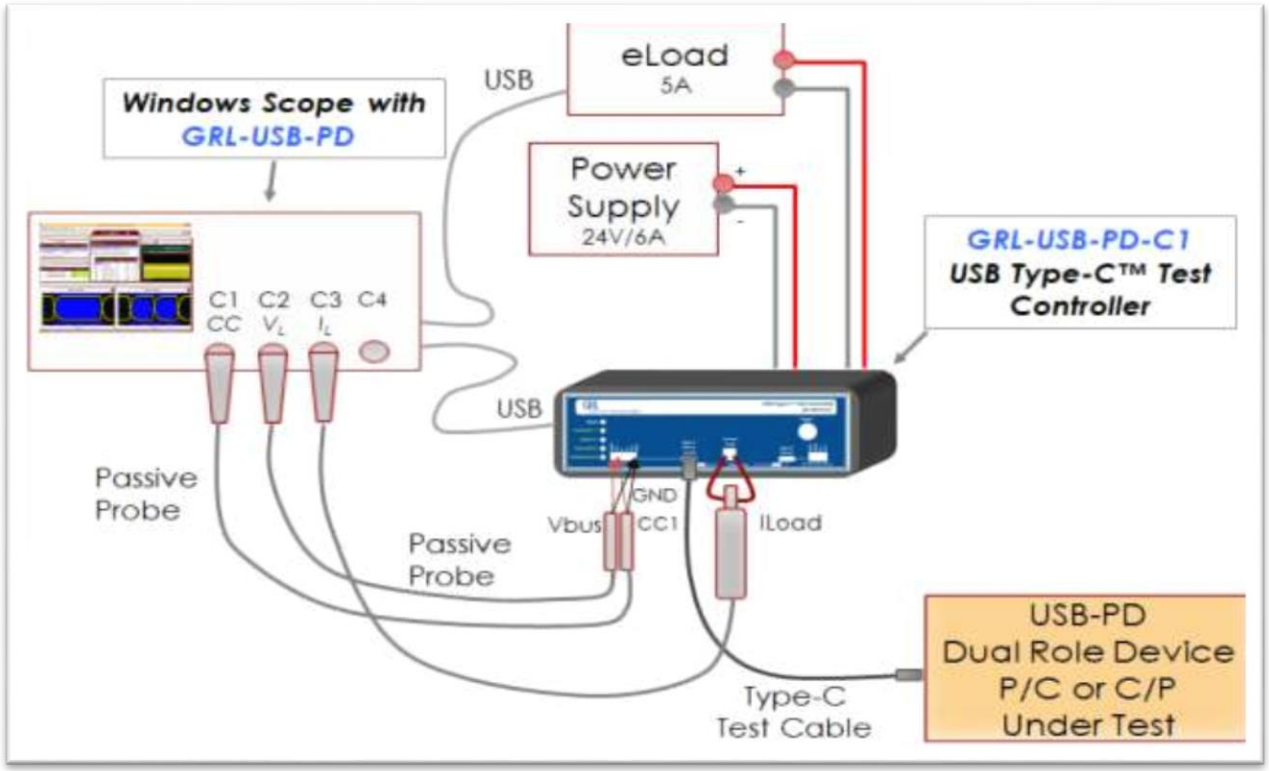




KEYSIGHT TECHNOLOGIES

USB-PD Device tests

Test setup - DRP



- Require electrical Load, current probe for load test
- Power supply will be sufficient to using SMPS power adopter but I can use for external power supply for clean power source

USB-PD Device tests

Primary tests

Test Group	Test Description	Test Name	Required Tests by Device Type			
			Provider Only	Consumer Only	Dual Role Device	
					P/C	C/P
2	**Primary Power Delivery Device Tests**					
2.1	**BMC PHYSICAL LAYER TESTS - TRANSMIT**					
TD 2.1.1	BMC Transmitter Eye Diagram Test	BMC-PHY-TX-EYE	✔	✔	✔	✔
TD 2.1.2	BMC Transmit Bit Rate and Bit Rate Drift	BMC-PHY-TX-BIT	✔	✔	✔	✔
2.2	**BMC PHYSICAL LAYER TESTS - RECEIVE**					
TD 2.2.1	BMC Bus Idle Detection Test	BMC-PHY-RX-BUSIDL	✔	✔	✔	✔
TD 2.2.2	BMC Receive Interference Rejection Test	BMC-PHY-RX-INT-REJ	✔	✔	✔	✔
2.3	**BMC PHYSICAL LAYER TESTS - MISCELLANEOUS**					
TD 2.3.1	BMC Termination Impedance Test	BMC-PHY-TERM	✔	✔	✔	✔
TD 2.3.2	BMC PHY Level Message Test	BMC-PHY-MSG	✔	✔	✔	✔
2.4	**PROTOCOL SPECIFIC - Message Checks**					
TD 2.4.1	Get_Source_Cap and Get_Sink_Cap Test	BMC-PROT-SEQ-GETCAPS	✔	✔	✔	✔
TD 2.4.2	Check Cable Capabilities (3A Marked) Test	BMC-PROT-SEQ-CHKCAB-P-PC	✔	✔	✔	✔
TD 2.4.3	Check Cable Capabilities (Unmarked) Test	BMC-PROT-SEQ-CHKCAB-NOMRK-P-PC	✔	✔	✔	✔
TD 2.4.4	Check Cable Capabilities (3A Marked) Test - After PR Swap	BMC-PROT-SEQ-CHKCAB-CP-ACC	✔	✔	✔	✔
TD 2.4.5	Check Cable Capabilities (Unmarked) Test - After PR Swap	BMC-PROT-SEQ-CHKCAB-NOMRK-CP-ACC	✔	✔	✔	✔
TD 2.4.6	Dual Role Swap Test	BMC-PROT-SEQ-DRSWAP	✔	✔	✔	✔
TD 2.4.7	VCONN Swap Test	BMC-PROT-SEQ-VCSWAP	✔	✔	✔	✔
TD 2.4.8	ID Checks	BMC-PROT-DISCOV	✔		✔	✔
TD 2.4.9	Reject Swap Test - Provider/Consumer	PROT-SEQ-SWAP-REJ			✔	
TD 2.4.10	BIST Functionality at Above 5V Test	BMC-PROT-BIST-NOT-5V-SRC	>5V DUT Only		>5V DUT Only	
TD 2.4.11	Revision Number Test	BMC-PROT-REV-NUM	✔	✔	✔	✔
2.5	**Power Source/Sink Tests**					
TD 2.5.1	Source Dynamic Load Test, Provider or Provider/Consumer	BMC-POW-SRC-LOAD-P-PC	✔		✔	
TD 2.5.2	Source Dynamic Load Test, Consumer/Provider Accepting Swap	BMC-POW-SRC-LOAD-CP-ACC				✔
TD 2.5.3	PDO Transition Test - Source, Provider or Provider/Consumer	BMC-POW-SRC-TRANS-P-PC	✔		✔	
TD 2.5.4	PDO Transition Test - Source, Consumer/Provider Accepting Swap	BMC-POW-SRC-TRANS-CP-ACC				✔
TD 2.5.5	PDO Transition, Current Draw and Suspend Test - Sink, Consumer or Consumer/Provider	BMC-POW-SNK-TRANS-C-CP		✔		✔
TD 2.5.6	PDO Transition, Current Draw, and Suspend Test, Sink, Provider/Consumer	BMC-POW-SNK-TRANS-PC			✔	

Source : USB-PD Test plan Rev 0.9

USB-PD Device tests

Secondary checks

Test Group	Test Description	Test Name	Required Tests by Device Type				
			'eMark' Cable	Provider	Consumer	Dual Role Device	
						P/C	C/P
3	**Secondary Tests for all Devices**						
3.1	**Secondary Message Checks** Performed whenever the Appropriat Message is Detected						
TID 3.1.1	PHY Level General Message Test (SOP*)	PHY-MSG-GEN					
TID 3.1.2	Message Header Checks - Except GoodCRC	PROT-MSG-HDR	✔	✔	✔	✔	✔
TID 3.1.3	Message Header Checks - GoodCRC	PROT-MSG-HDR-GCRC	✔	✔	✔	✔	✔
TID 3.1.4	Control Message Checks	PROT-MSG-CTRL	✔	✔	✔	✔	✔
TID 3.1.5	Ping Checks	PROT-MSG-CTRL-PING		✔		✔	✔
TID 3.1.6	Source Capability Message Checks	PROT-MSG-DATA-SRC-CAP		✔	✔	✔	✔
TID 3.1.7	Sink Capability Message Checks	PROT-MSG-DATA-SNK-CAP		✔	✔	✔	✔
TID 3.1.8	Request Message Checks	PROT-MSG-DATA-REQ			✔	✔	✔
TID 3.1.9	BIST Message Checks - Sent by UUT	PROT-MSG-DATA-BIST		✔	✔	✔	✔
TID 3.1.10	Vendor Defined Message Checks	PROT-MSG-DATA-VEND	✔	✔	✔	✔	✔
TID 3.1.11	Discover ID Initiator Message Checks	PROT-MSG-DATA-VDM-ID-INIT		✔	✔	✔	✔
TID 3.1.12	Discover ID ACK Message Checks	PROT-MSG-DATA-VDM-ID-ACK	✔	✔	✔	✔	✔
TID 3.1.13	Discover SVIDs Initiator Message Checks	PROT-MSG-DATA-VDM-SVID-INIT		✔	✔	✔	✔
TID 3.1.14	Discover SVIDs ACK Message Checks	PROT-MSG-DATA-VDM-SVID-ACK	✔	✔	✔	✔	✔
TID 3.1.15	Discover Modes Initiator Message Checks	PROT-MSG-DATA-VDM-MODE-INIT		✔	✔	✔	✔
TID 3.1.16	Discover Modes ACK Message Checks	PROT-MSG-DATA-VDM-MODE-ACK	✔	✔	✔	✔	✔
TID 3.1.17	Enter Mode Message Checks	PROT-MSG-DATA-VDM-ENTER-MODE	✔	✔	✔	✔	✔
TID 3.1.18	Exit Mode Message Checks	PROT-MSG-DATA-VDM-EXIT-MODE	✔	✔	✔	✔	✔
TID 3.1.19	Attention Message Checks	PROT-MSG-DATA-VDM-ATT	✔	✔	✔	✔	✔
TID 3.1.20	Procedure and Checks for any Atomic Message Sequence	PROT-PROC-AMS_1	✔	✔	✔	✔	✔

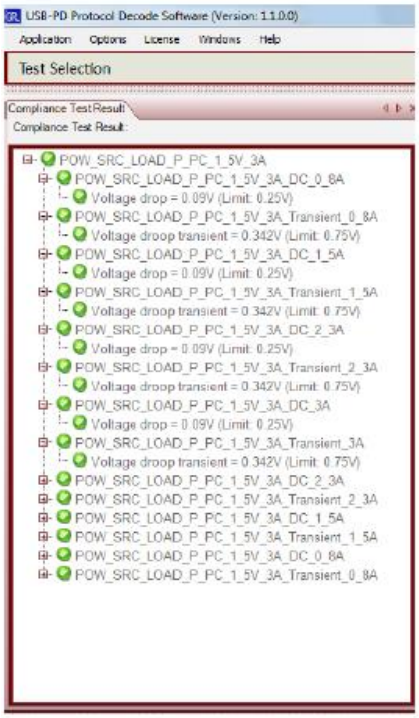
		:RC-TSTR		✔	✔	✔	✔
		:RC-UUT		✔	✔	✔	✔
		TSTR-SNK				✔	✔
		TSTR-SRC				✔	✔
		UUT-SNK				✔	✔
		UUT-SRC				✔	✔
		RCEOFFTIMER					✔
TID 3.2.8	Procedures to test PSSourceOnTimer when not Swapped	PROT-PROC-PSSOURCEONTIMER				✔	✔
TID 3.2.9	Procedures to test PSSourceOnTimer when Swapped	PROT-PROC-PSSOURCEONTIMER-SWPD				✔	✔
TID 3.2.10	Procedures to send Ping from Tester	PROT-PROC-PING					
TID 3.2.11	Procedure and Checks for Tester Originated Request	PROT-PROC-REQ-TSTR		✔		✔	✔
TID 3.2.12	Procedure and Checks for UUT Originated Request	PROT-PROC-REQ-UUT		✔		✔	✔
TID 3.2.13	Procedure and Checks for Tester Originated Source Capabilities	PROT-PROC-SRCCAPS-TSTR		✔	✔	✔	✔
TID 3.2.14	Procedure and Checks for UUT Originated Source Capabilities	PROT-PROC-SRCCAPS-UUT		✔		✔	✔
TID 3.2.15	Procedure and Checks for Tester Originated Get_Source_Cap	PROT-PROC-GETSRCCAPS-TSTR		✔	✔	✔	✔
TID 3.2.16	Procedure and Checks for UUT Originated Get_Source_Cap	PROT-PROC-GETSRCCAPS-UUT		✔	✔	✔	✔
TID 3.2.17	Procedure and Checks for Tester Originated Get_Sink_Cap	PROT-PROC-GETSNKCAPS-TSTR		✔	✔	✔	✔
TID 3.2.18	Procedure and Checks for UUT Originated Get_Sink_Cap	PROT-PROC-GETSNKCAPS-UUT		✔	✔	✔	✔
TID 3.2.19	Procedure and Checks for Tester Originated GotoMin	PROT-PROC-GOTOMIN-TSTR		✔	✔	✔	✔
TID 3.2.20	Procedure and Checks for UUT Originated GotoMin	PROT-PROC-GOTOMIN-UUT		✔	✔	✔	✔
TID 3.2.21	Procedure and Checks for Tester Originated Soft Reset	PROT-PROC-SR-TSTR		✔	✔	✔	✔
TID 3.2.22	Procedure and Checks for UUT Originated Soft Reset	PROT-PROC-SR-UUT		✔	✔	✔	✔
TID 3.2.23	Procedure and Checks for Tester Originated Hard Reset	PROT-PROC-HR-TSTR		✔	✔	✔	✔
TID 3.2.24	Procedure and Checks for UUT Originated Hard Reset	PROT-PROC-HR-UUT		✔	✔	✔	✔
TID 3.2.25	Procedure and Checks for Tester Originated BIST	PROT-PROC-BIST-TSTR		✔	✔	✔	✔

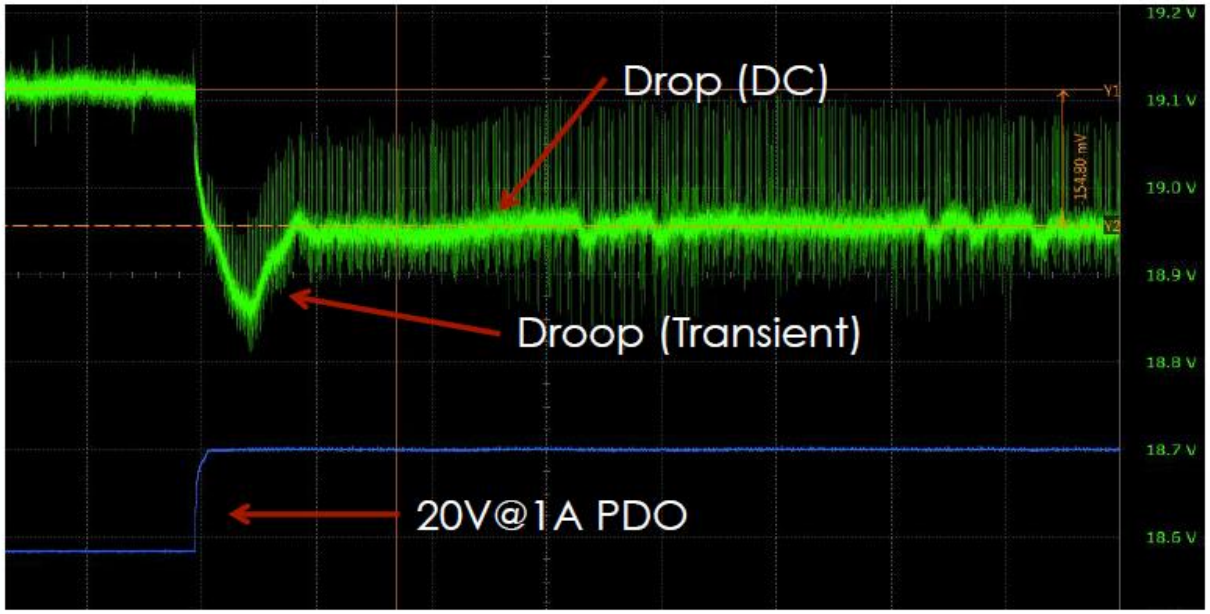
KEYSIGHT TECHNOLOGIES

Source : USB-PD Test plan Rev 0.9

USB-PD Device tests

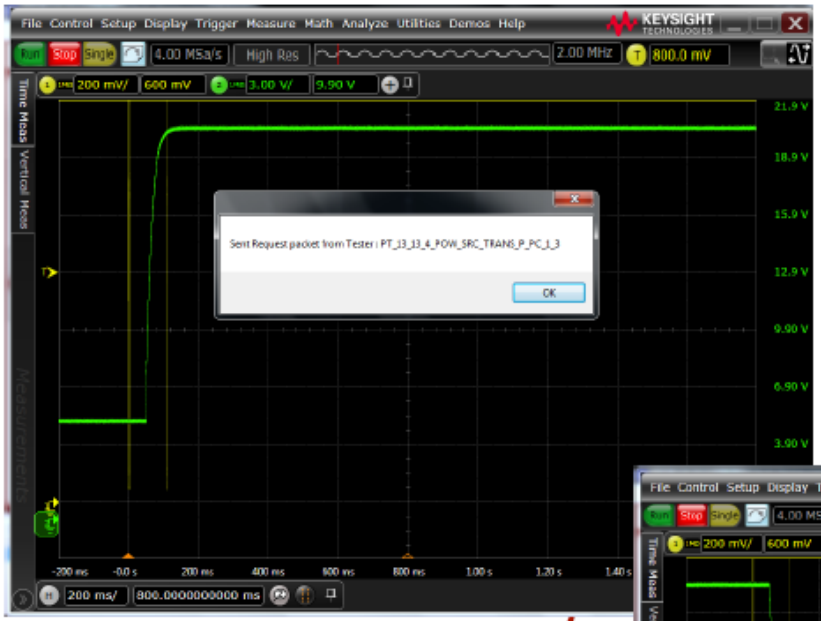
Power Load test result

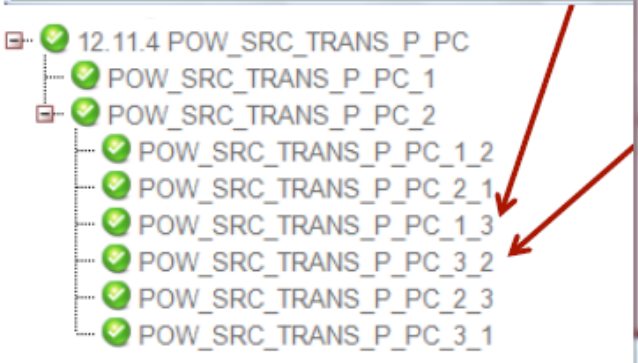




USB-PD Device tests

Power Transition test result



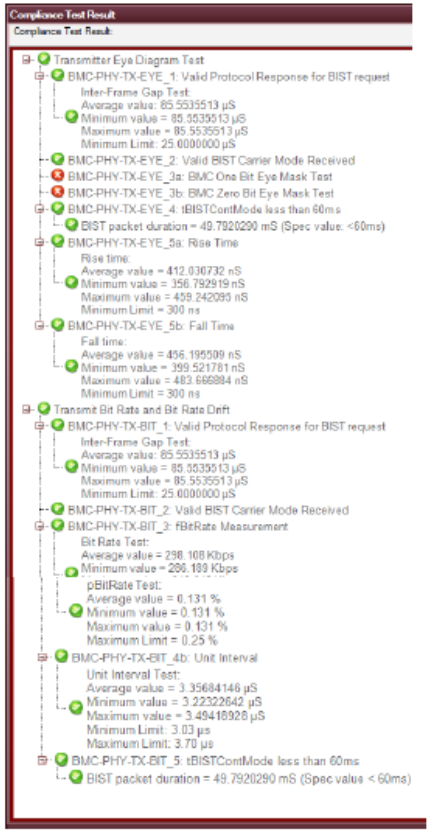


Number of PDOs in Capabilities Message						
1	2	3	4	5	6	7
1 to 1*	1 to 2	1 to 2	1 to 2	1 to 2	1 to 2	1 to 2
	2 to 1	2 to 1	2 to 1	2 to 1	2 to 1	2 to 1
		1 to 3	1 to 3	1 to 3	1 to 3	1 to 3
		3 to 2	3 to 2	3 to 2	3 to 2	3 to 2
		2 to 3	2 to 3	2 to 3	2 to 3	2 to 3
		3 to 1	3 to 1	3 to 1	3 to 1	3 to 1
			1 to 4	1 to 4	1 to 4	1 to 4
			4 to 3	4 to 3	4 to 3	4 to 3
			3 to 4	3 to 4	3 to 4	3 to 4
			4 to 2	4 to 2	4 to 2	4 to 2
			2 to 4	2 to 4	2 to 4	2 to 4
			4 to 1	4 to 1	4 to 1	4 to 1
				1 to 5	1 to 5	1 to 5
				5 to 4	5 to 4	5 to 4
				4 to 5	4 to 5	4 to 5
				5 to 3	5 to 3	5 to 3
				3 to 5	3 to 5	3 to 5
				5 to 2	5 to 2	5 to 2
				2 to 5	2 to 5	2 to 5
				5 to 1	5 to 1	5 to 1
					1 to 6	1 to 6
					6 to 5	6 to 5
					5 to 6	5 to 6
					6 to 4	6 to 4
					4 to 6	4 to 6
					6 to 3	6 to 3
					3 to 6	3 to 6
					6 to 2	6 to 2
					2 to 6	2 to 6
					6 to 1	6 to 1
						1 to 7
						7 to 6
						6 to 7
						7 to 5
						5 to 7
						7 to 4
						4 to 7
						7 to 3
						3 to 7
						7 to 2
						2 to 7
						7 to 1

USB-PD Device tests

Compliance result

BMC PHY

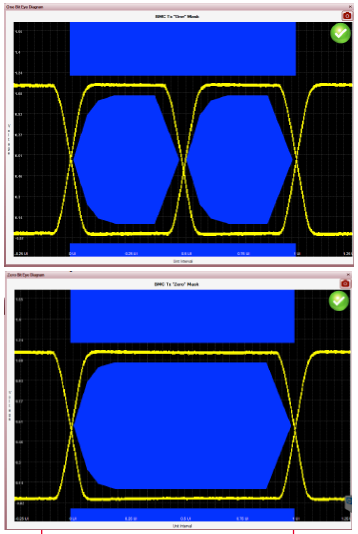


Power Loads and Transitions

- 12.11.1 POW_SRC_LOAD_P_PC
  - POW_SRC_LOAD_P_PC_1
    - DUT failed to send PING message when contracted to greater than 5V
  - POW_SRC_LOAD_P_PC_2
  - POW_SRC_LOAD_P_PC_PDO1_5V_3A
    - POW_SRC_LOAD_P_PC_3
    - POW_SRC_LOAD_P_PC_4
    - POW_SRC_LOAD_P_PC_5
    - POW_SRC_LOAD_P_PC_6
      - Load Current set to 0.75: Voltage drop = 0.032V (Limit: 0.25V)
      - Load Current set to 1.5: Voltage drop = 0.031V (Limit: 0.25V)
      - Load Current set to 2.25: Voltage drop = 0.265V (Limit: 0.25V)
      - Load Current set to 3: Voltage drop = 0.41V (Limit: 0.25V)
      - Load Current set to 2.25: Voltage drop = 0.283V (Limit: 0.25V)
      - Load Current set to 1.5: Voltage drop = 0.025V (Limit: 0.25V)
      - Load Current set to 0.75: Voltage drop = 0.044V (Limit: 0.25V)
  - POW_SRC_LOAD_P_PC_PDO2_12V_3A
    - POW_SRC_LOAD_P_PC_3
    - POW_SRC_LOAD_P_PC_4
    - POW_SRC_LOAD_P_PC_5
    - POW_SRC_LOAD_P_PC_6
      - Load Current set to 0.75: Voltage drop = 0.165V (Limit: 0.6V)
      - Load Current set to 1.5: Voltage drop = 0.075V (Limit: 0.6V)
      - Load Current set to 2.25: Voltage drop = 0.277V (Limit: 0.6V)
      - Load Current set to 3: Voltage drop = 0.422V (Limit: 1V)
      - Load Current set to 2.25: Voltage drop = 0.227V (Limit: 1V)
      - Load Current set to 1.5: Voltage drop = 0.007V (Limit: 1V)
      - Load Current set to 0.75: Voltage drop = 0.172V (Limit: 1V)
- 12.11.4 POW_SRC_TRANS_P_PC
  - POW_SRC_TRANS_P_PC_1
  - POW_SRC_TRANS_P_PC_2
    - POW_SRC_TRANS_P_PC_1_2
    - POW_SRC_TRANS_P_PC_2_1
    - POW_SRC_TRANS_P_PC_1_3
    - POW_SRC_TRANS_P_PC_3_2
    - POW_SRC_TRANS_P_PC_2_3
    - POW_SRC_TRANS_P_PC_3_1

Power Role Swap

- POW_SWAP_PC_SRC_REQ
  - PROC_PD_MODE
  - PROT_PROC_SWAP_UUT_SRC
    - UUT could not initiate Power Role Swap
- POW_SWAP_PC_SNK_SRC
  - PROC-PD-MODE
  - PROT-PROC-SWAP-TSTR-SNK
  - PROT-PROC-SWAP-TSTR-SRC
- POW_SWAP_PC_SNK_SNK
  - PROC-PD-MODE
  - PROT-PROC-SWAP-TSTR-SNK
  - PROT-PROC-SWAP-UUT-SNK



KEYSIGHT TECHNOLOGIES

Thank you