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Clocks: Optimizing and Supporting JESD204B Interfaces

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09/23/2015

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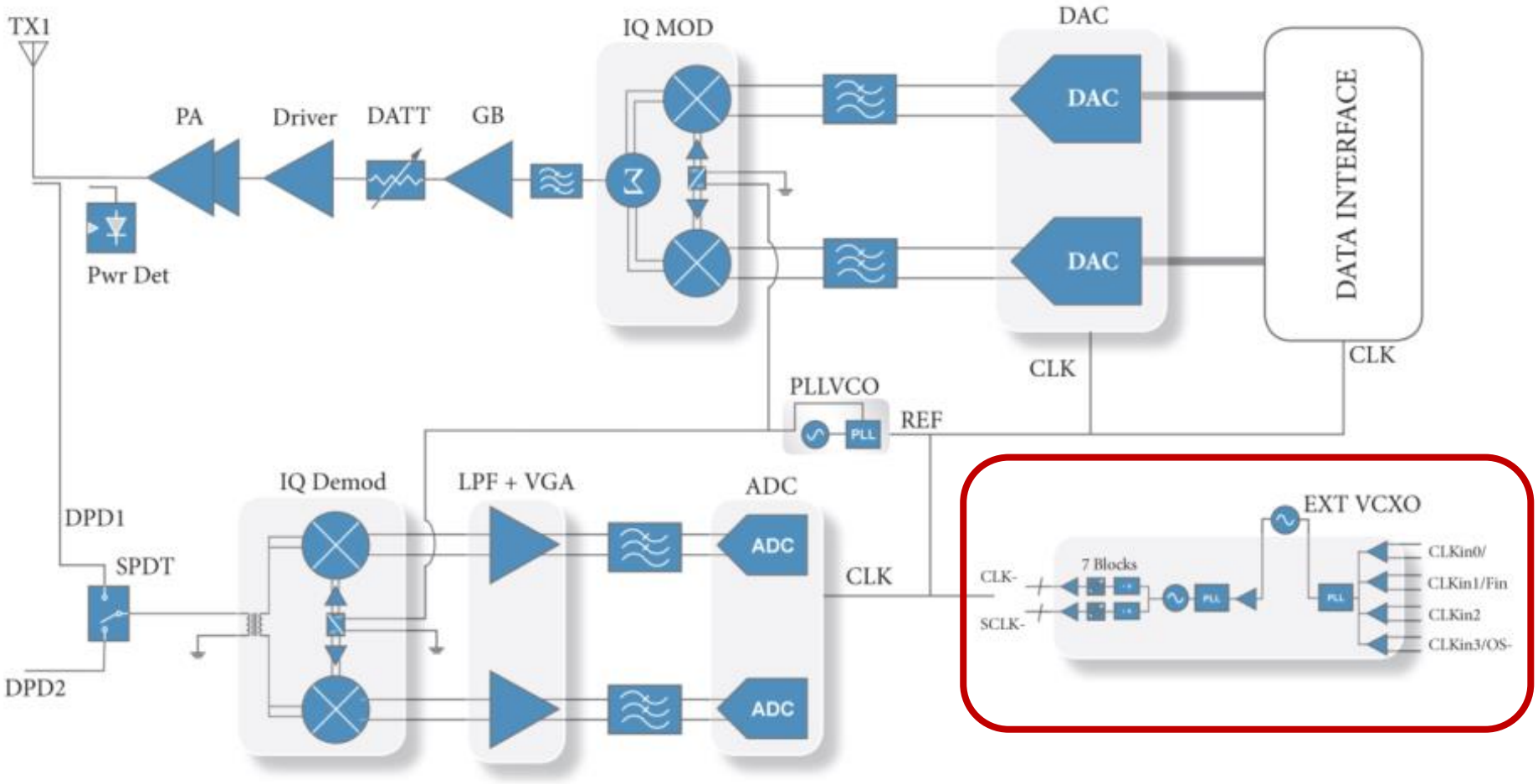
Base Station Clocking

Common Transceiver Card Design



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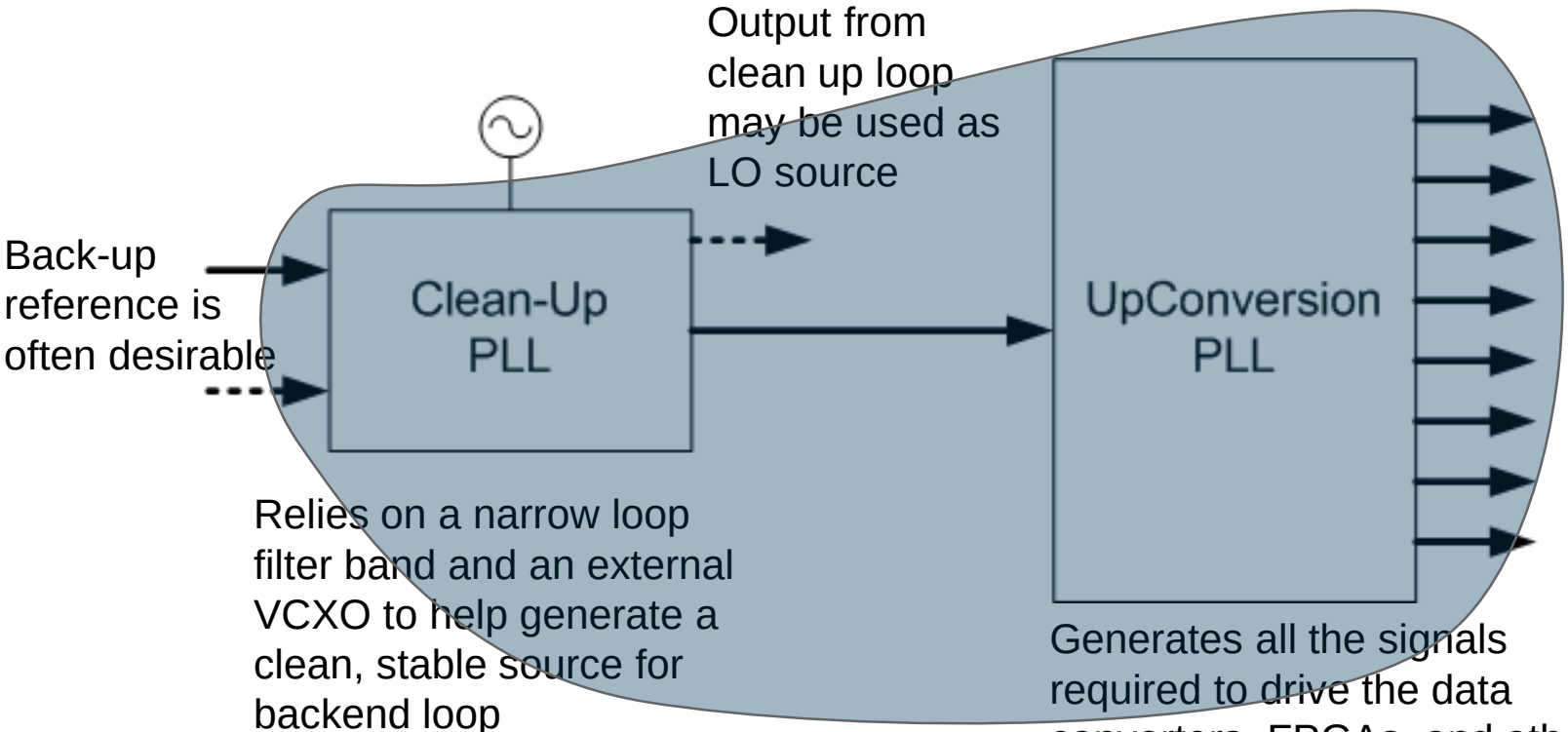
Common Transceiver Card Clock Tree



Most designs rely on a single chip with both PLLs on it

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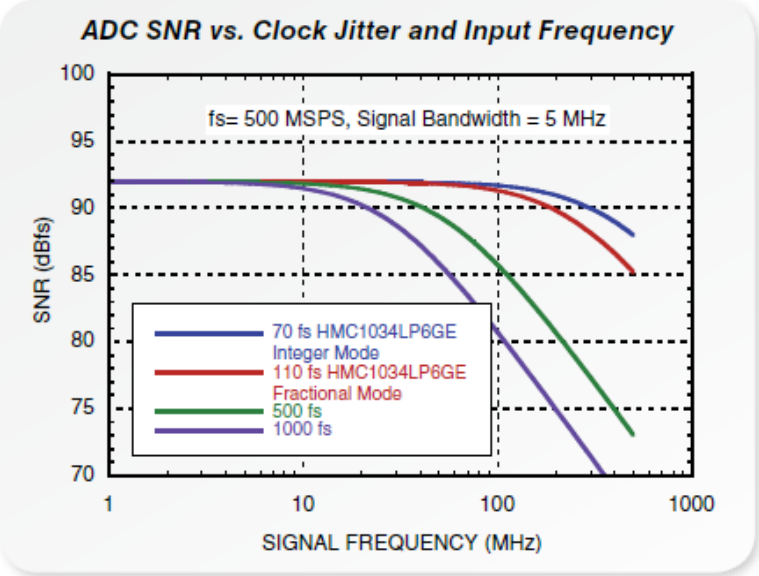
Data Converter Clocking (ADC/DAC Sample Clocks)

Extract the Best SNR Performance from your Data Converters!

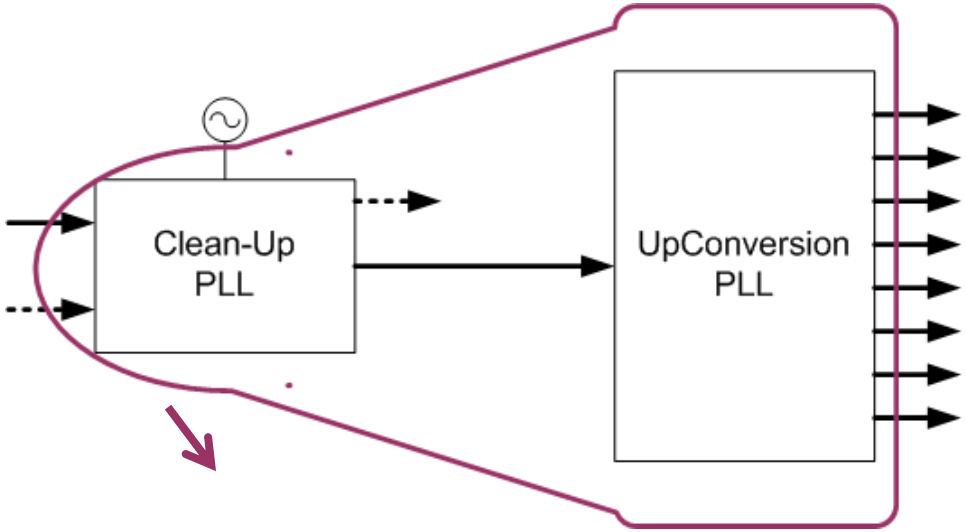
- HMC1034LP6GE achieves <100fs RMS Phase Jitter in Integer Mode
- HMC987LP5E, 1:8 LVPECL Fan-out Buffer Distributes Data Converter Sample Clocks with only 8fs RMS additive Jitter (12kHz to 20MHz)
- HMC988LP3E Clock Divider & Delay Management IC Adjusts Data Converter Sample Clock Windows in 20ps Resolution and Offers -170dBc/Hz Phase Noise Floor
- AD9525, 8-Output Clock Generator with <50fs RMS Absolute jitter



The low phase noise floor of a clock signal as well as its low integrated phase jitter helps to minimize the SNR degradation at high ADC / DAC input frequencies in multi-carrier, multi-acquisition applications. Analog Devices' Clock and Timing Ics are designed with data converter applications in mind, and work well with Analog Devices' High Speed ADC devices

Current & Emerging Generation WIFR Clock Architecture

Released



AD9528 (14 output)
JESD204B support, 1.25GHz max
Wide tuning- 0.18 CMOS

HMC7044 (14 output)
JESD204B, 3.2 GHz max
Narrow tuning- 0.18 BiCMOS

FY14 FY15

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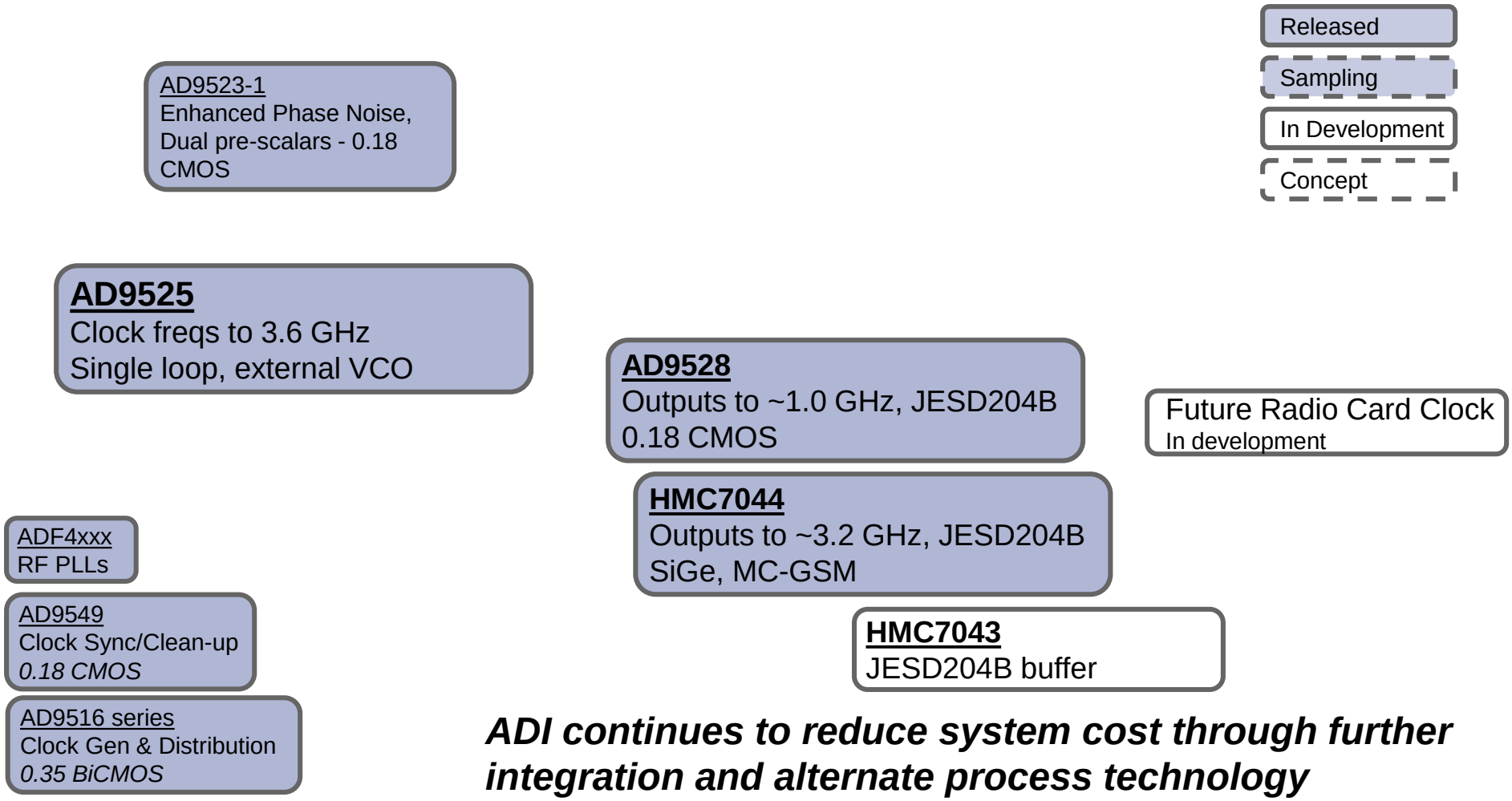
Latest Radio Card Clock Offerings



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Introducing the HMC7044

HMC7044 Introduction

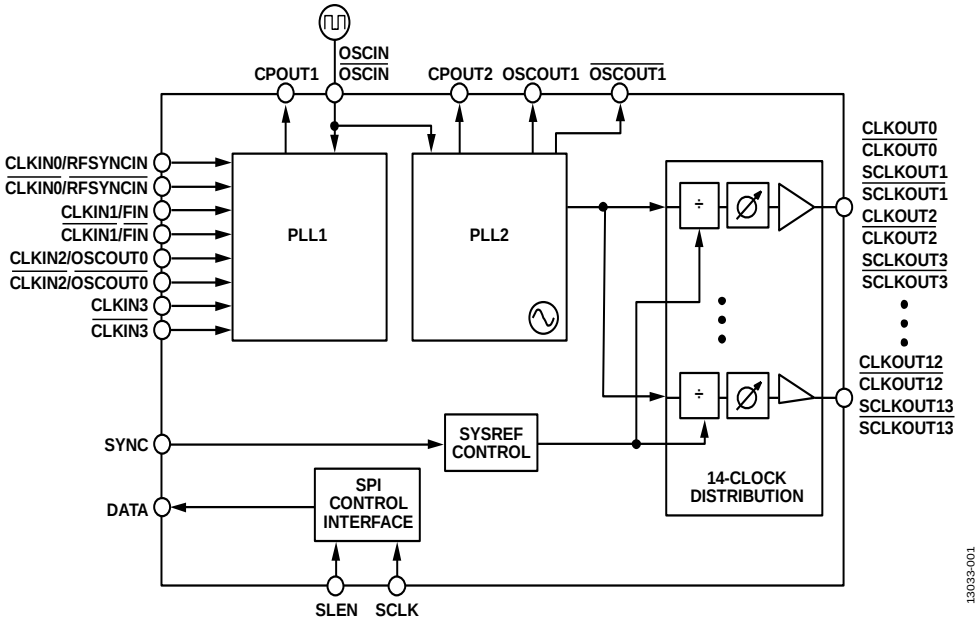
Highlights

Industry Leading Performance
- Ultra-low 45fs RMS jitter (12k-20MHz) at 2949.12 MHz
- Best-in-class Phase Noise Floor of -156.3dBc/Hz at 2.5GHz
- Excellent GSM blocker performance of -141.7dBc/Hz at 800kHz with 983.04MHz output

Supports JESD204B Synchronization
- "Sysref-Valid" Interrupt
- Deterministic Latency to RF-SYNC inputs for multiple device clock tree designs
- Multiple HMC7044 devices may be connected with pin or SPI-controlled SYNC trigger

Improve Bandwidth with Wide Frequency Coverage
- 2 integrated VCO cores for operation up to 3.2GHz
- Support for up to 6GHz of external VCO

Flexible Configuration:
- 16 Outputs: 14+2 configuration: Programmable in LVDS/LVPECL/CML or CMOS type options
- Complete flexibility of configuring each output to be either Device or SYSREF clock outputs
- Excellent channel isolation
- Separate clock groups with <-75dBc channel isolation while maintaining tight channel skew



Package	Status
10x10mm 68 pin LFCSP	Sampling Release: Sep 2015

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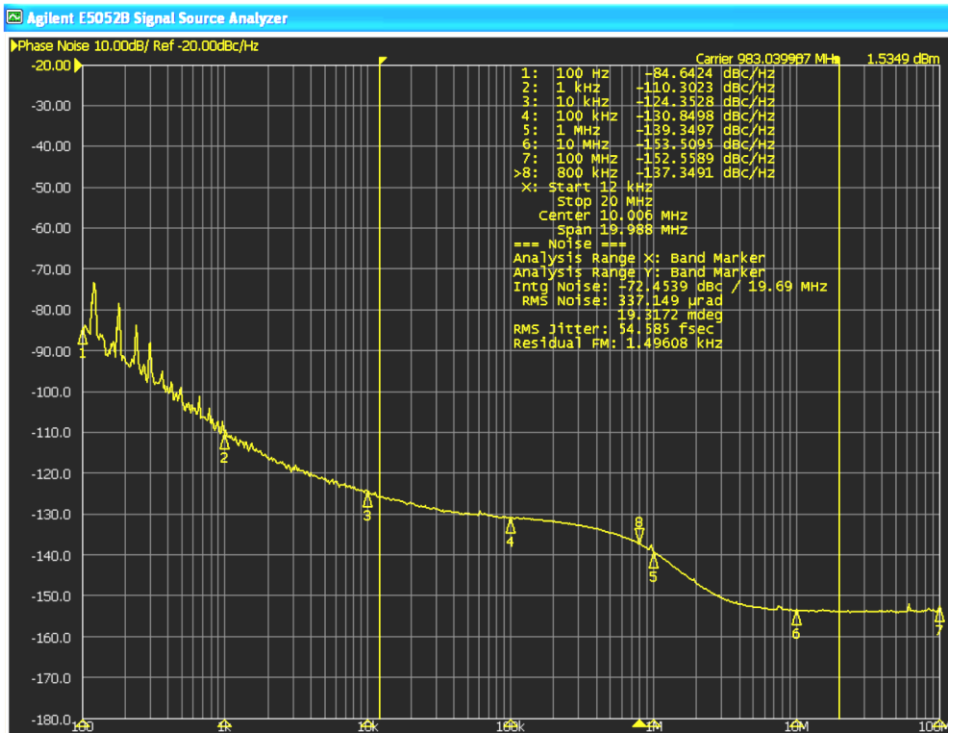
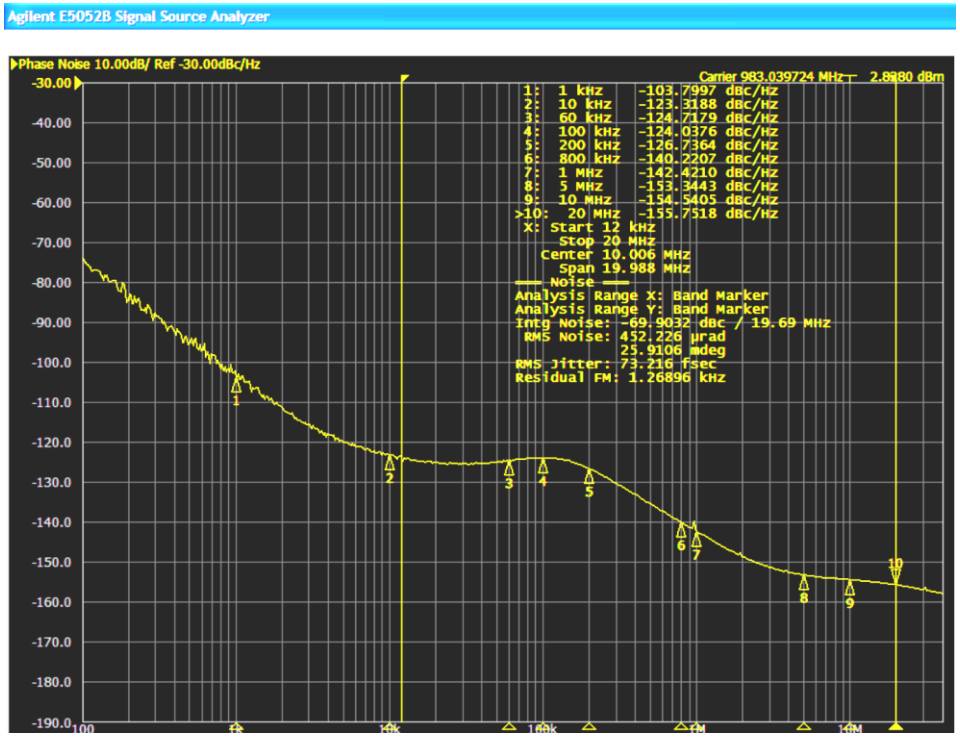
HMC7044 Performance Overview





HMC7044 may be configured for best integrated jitter operation with <55fs RMS jitter performance

800kHz offset may be improved to as low as -140.3dBc at 983.04M with bias setting change

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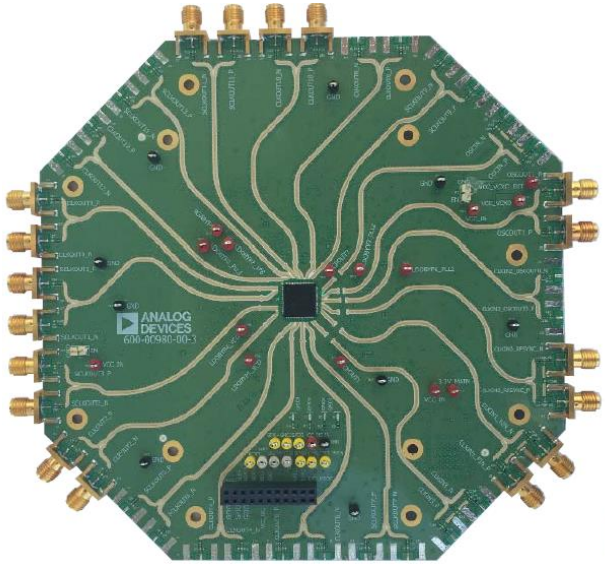
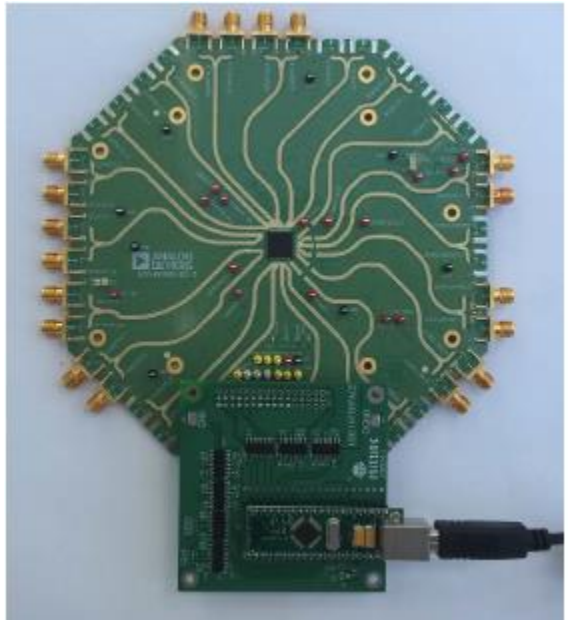
Customer Value of the HMC7044LP10BE

Features	Benefits / Customer Value
Industry leading Performance	○ Improve SNR and Dynamic Range of high speed data converters ○ Generate LO signals with excellent spurious performance ○ CPRI clock jitter attenuation
Supports JESD204B Synchronization	○ Simplify the frame alignment procedure between the FPGA and ADC/DAC components ○ Reduce system latency by monitoring “sysref_valid” interrupt to avoid additional wait time ○ Build large systems with multiple data acquisition channels which can be synchronized to a master FPGA sysref signal
16 Outputs: 14+2 configuration	○ Single device to generate all required basestation sample-, and JESD204B frame-alignment (SYSREF) clock signals
Wide Frequency Coverage	○ Support high sample rate and RF- ADC/DAC components ○ SPI-programmable frequency settings
Very linear output phase adjustment	○ Flexibility to compensate for PCB flight time mismatches among different outputs ○ Ensure proper setup and hold times are observed for data converters
SPI-programmable performance vs. power adjustment	○ Allows for multiple use cases with either low power or high performance operation depending on system needs
High Accuracy Frequency Holdover	○ Improves Quality of Service (reduces instances of down time) ○ Effective clock management in case of reference clock failures ○ Maintain frequency accuracy to ensure continuous operation or shut-down procedure when CPRI link fails
Flexible and Priority-based Reference Switchover	○ Improves Quality of Service (reduces instances of lost calls and down time) ○ Effective clock management in case of reference, system clock failures
Complete flexibility of configuring each output to be either Device or SYSREF clock outputs	○ Improve spurious performance while still generating multiple frequencies on the same device

Evaluation Board Available

The EK1HMC7044LP10B evaluation kit is a compact, easy to use platform for evaluating all the features of the HMC7044. A 122.88 MHz VCXO is mounted on the evaluation board to provide a complete solution. All inputs and outputs are configured as differential on the evaluation board.





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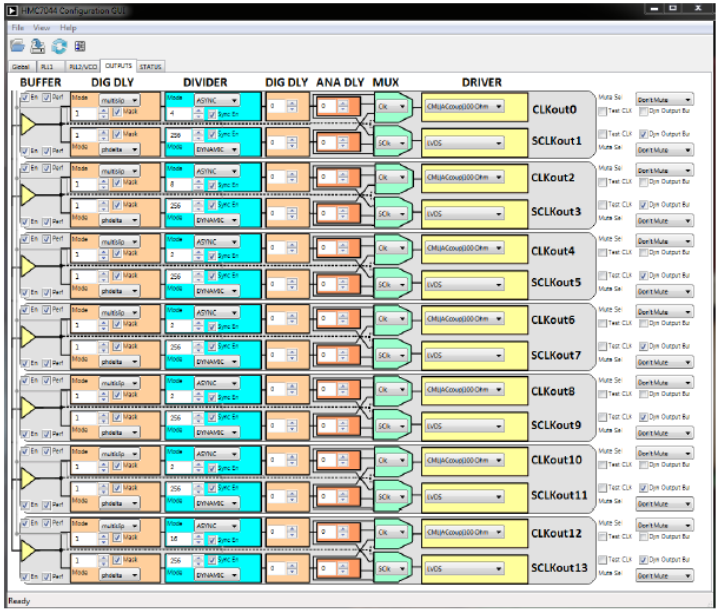
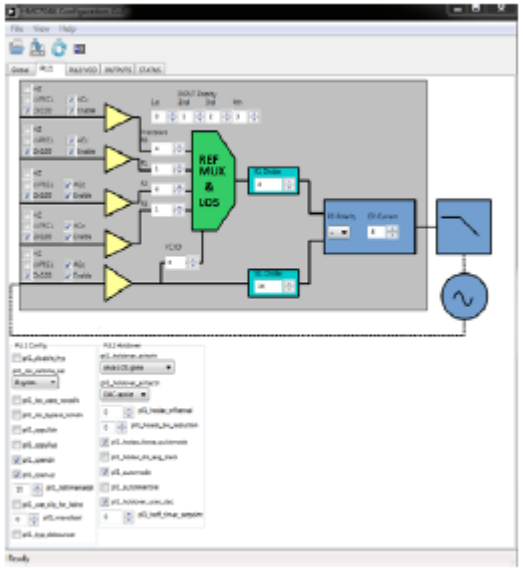
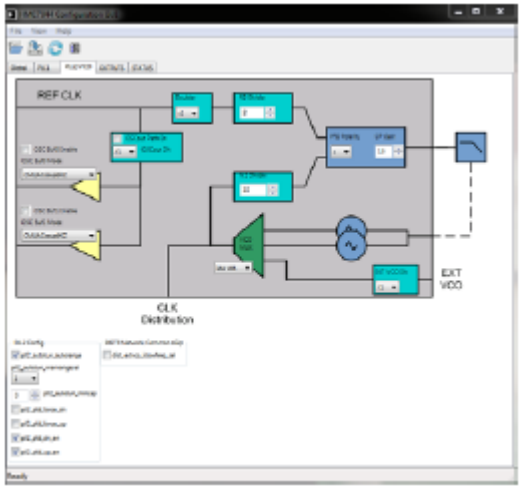
Evaluation Board Available

The evaluation kit of the HMC7044 comes with an easy-to-use, GUI based configuration software. Providing pull-down menus and check-box based input fields for easy configuration, the software allows the designer to save a setup file and generate the required register contents.







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HMC7044 Information

- Product Webpage:

http://www.analog.com/HMC7044

- Evaluation board and units are available

- Easy-to-use configuration software

- IBIS Models are available on request

- Incorporated with ADISimFrequencyPlanner tool:
  https://ez.analog.com/message/185966#185966

- Contacts: RFMG-timing@analog.com

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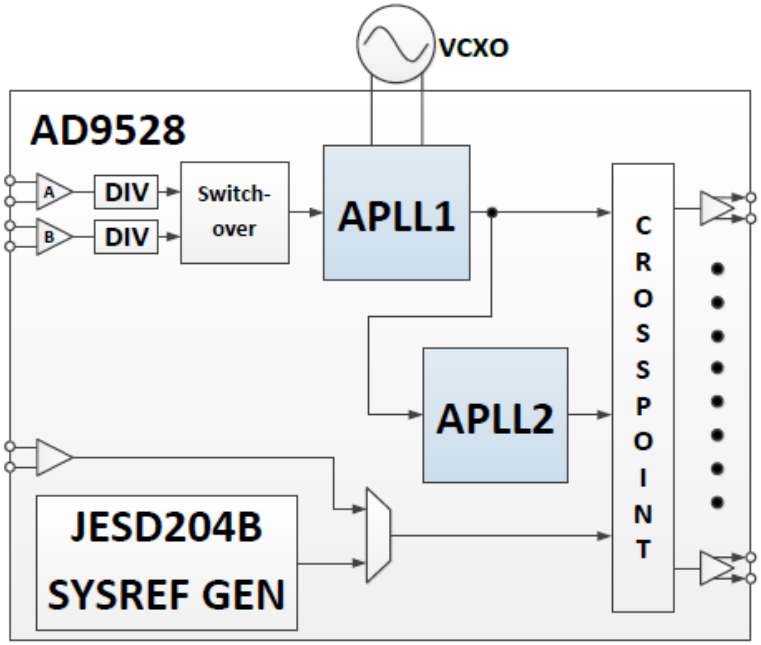
AD9528 for BTS Clocking

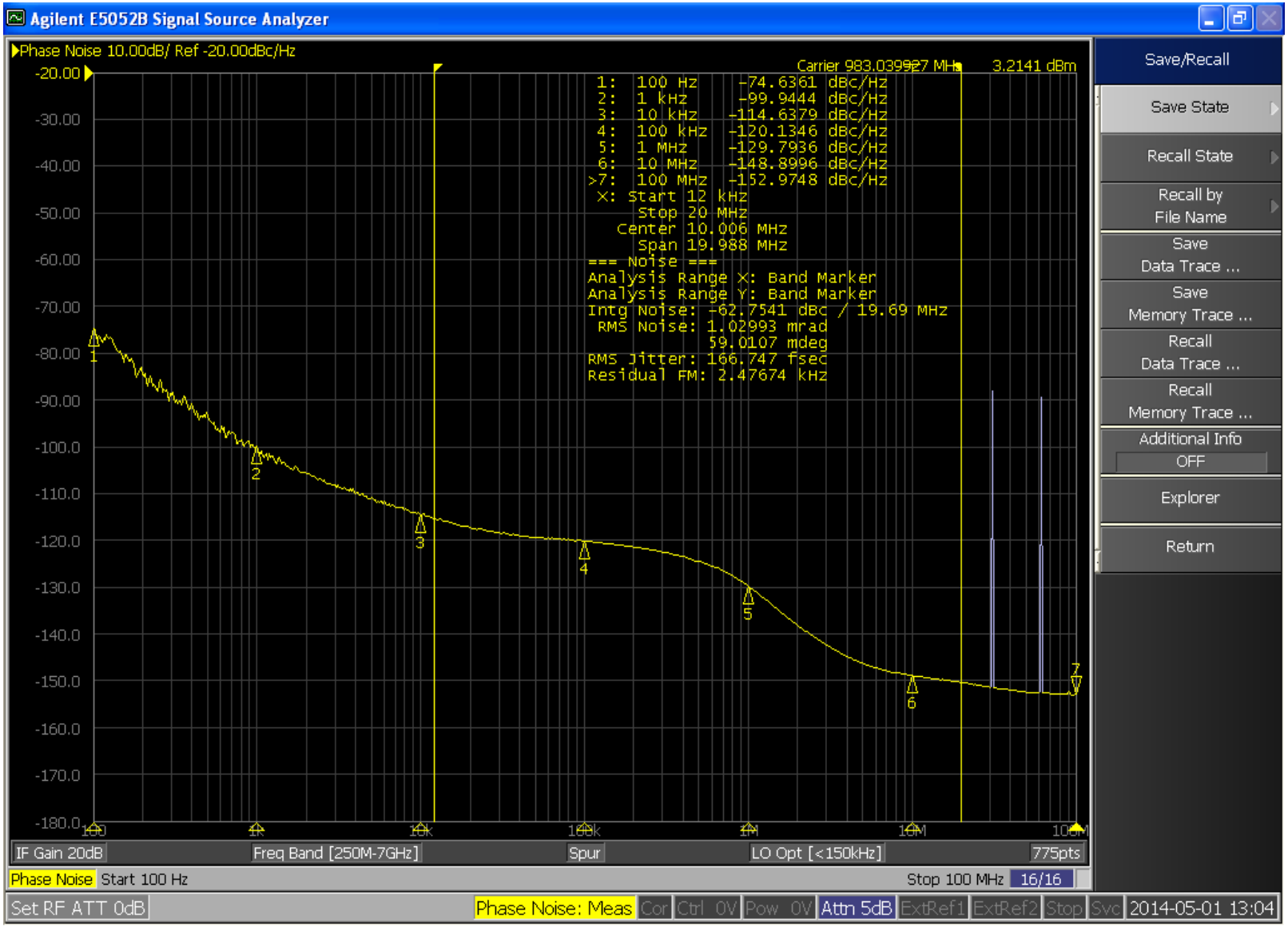
AD9528: JESD204B Compatible Clock Generator

- PRIMARY DIFFERENTIATION POINTS
- Lower power
  - Consumes ~ 2/3rds in similar configurations
- Lower output frequency
  - Max output frequency 1.25 GHz vs. 3.25 GHz
- Worse jitter/PN performance
  - AD9528 supports LTE, but not GSM performance needs
- Single 3.3V power supply
- Internal LDOs allow operation directly from switcher



Operating Freq	Status	Package	Output Logic
2 x 1.25 GHz 12 x 1.0 GHz	Released RFND	72 LFCSP 10x10	LVDS, HSTL

AD9528 Phase Noise (983.04MHz)



Customer Value of the AD9528BCPZ

Features	Benefits / Customer Value
Efficiency of Power solution	○ Eases design effort ○ Reduces cost of running ○ Can simplify cooling schemes
Supports JESD204B Synchronization	○ Simplify the frame alignment procedure between the FPGA and ADC/DAC components ○ Reduce system latency by monitoring “sysref_valid” interrupt to avoid additional wait time ○ Build large systems with multiple data acquisition channels which can be synchronized to a master FPGA sysref signal
14 Outputs: Up to seven Device/SYSREF pairs	○ Single device to generate all required basestation sample-, and JESD204B frame-alignment (SYSREF) clock signals ○ Perfectly aligned with ADI’s AD93xx transceiver solutions
Very linear output phase adjustment	○ Flexibility to compensate for PCB flight time mismatches among different outputs ○ Ensure proper setup and hold times are observed for data converters
High Accuracy Frequency Holdover	○ Improves Quality of Service (reduces instances of down time) ○ Effective clock management in case of reference clock failures ○ Maintain frequency accuracy to ensure continuous operation or shut-down procedure when CPRI link fails
Flexible and Priority-based Reference Switchover	○ Improves Quality of Service (reduces instances of lost calls and down time) ○ Effective clock management in case of reference, system clock failures
Complete flexibility of configuring each output to be either Device or SYSREF clock outputs	○ Improve spurious performance while still generating multiple frequencies on the same device

AD9528 Information

- Product Webpage:

http://www.analog.com/AD9528

- Evaluation board and units are available
- Easy-to-use configuration software
- IBIS Models are available on request
- Incorporated with ADISimCLK tool: http://www.analog.com/en/design-center/advanced-selection-and-design-tools/interactive-design-tools/adisimclk.html
- Engineer Zone support Community: https://ez.analog.com/community/clock_and_timing

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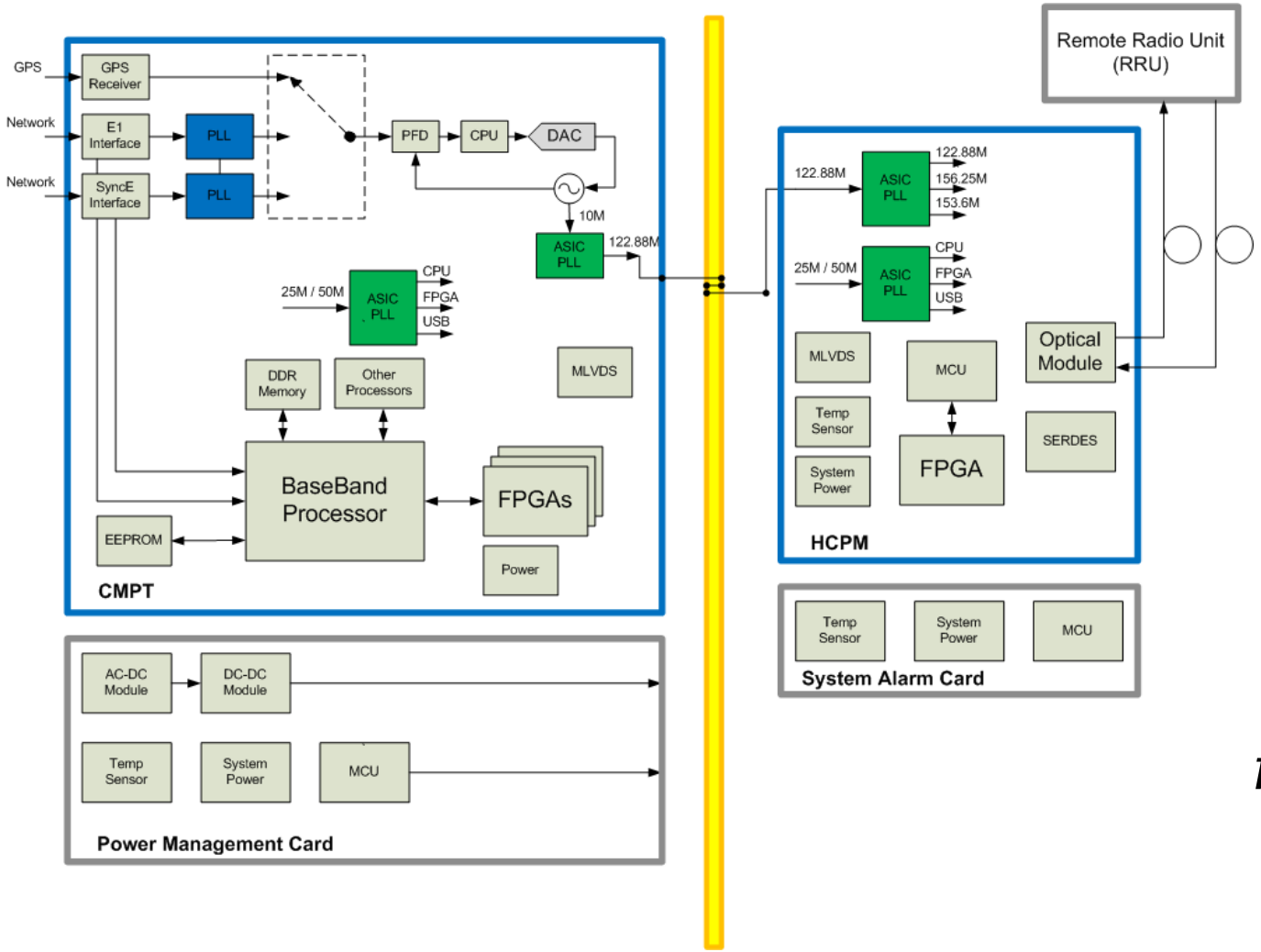
Baseband Unit Clocking

Clocking Needs for the BBU

The Traditional BBU has multiple clocking requirements



for all of them

Clocking the Base Band Unit

- Recovers network clock - phase & time stamp for management of Self Organized Networks (SON) or Heterogeneous networks (HetNet)
  - IEEE1588 protocol provides freq (marginal) and phase (difficult):
    - FDD-LTE requires < 2.5uS accuracy (CoMP could require < 0.5uS)
    - TDD-LTE also need 2.5uS
  - GPS (1PPS) or SyncE (T1/E1) provides freq. reference for radio card or RRH
  - Recommended 1PPS jitter cleanup benefit from digital loops

    AD9548 450Mhz outputs, hitless switching and holdover

    Next generation in development

- Ethernet, CPU, PCI clock sources can be integrated
  - Reduce cost & failure rate of XOs by deriving all clocks from single XO

    AD9572 Two PLLs, Fibre Channel clocks

    AD9574 Seven outputs from single 19.44 or 25MHz XO

    AD9531 Three PLLs, 24 outputs

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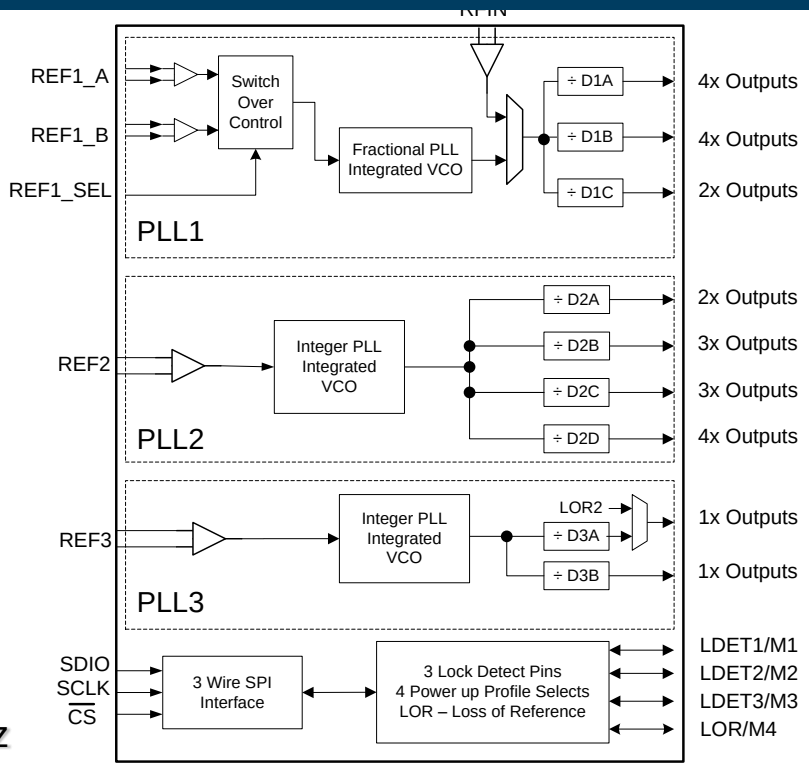
AD9531 BBU Clock Solution

- KEY BENEFITS & FEATURES
- Three fully integrated PLL/VCO cores
- Loss of reference and lock detection for each PLL
- Automatic synchronization of all outputs on power-up
- Manual output synchronization capability
- PLL1 optimized for CPRI clock generation
  - 0.21 ps rms jitter (12 kHz to 20 MHz) integer n mode
  - 0.46 ps rms jitter (12 kHz to 20 MHz) frac-n mode
  - Frequency range: 9.5 to 260 MHz CMOS
  - Frequency range: 310 kHz to 400 MHz HSTL
- PLL2 input: Diff./single-ended/crystal optimized for Ethernet clock
  - Jitter 0.34 ps rms
- PLL3 input: Differential/crystal CPU clock 9.5 to 100 MHz
  - 1.80 ps rms jitter
  - Outputs:
    - HSTL/LVDS: 22.5 MHz to 400 MHz
    - CMOS: 22.5 MHz to 150 MHz



Package	Output Logic	Status
12x12mm 88 LFCSP	HSTL, LVDS, CMOS	Released

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Wrap-up

- ADI offers a broad portfolio of signal chain products for the entire RF and data path of wireless systems
- Complementing the high performance data converter offerings, are best-in-class clocking products from ADI
- HMC7044 is introduced to offer a high frequency, high performance extension to the already most comprehensive portfolio of clocks for demanding applications
- AD9528 offers a power-efficient architecture with compelling features
- Future products from ADI will continue to be ***ahead of what's possible*** today!

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Thank You For Watching!

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