Enpirion PowerSoC

- DC-DC converter key parameter

Agenda

- **Efficiency**
  - **- Power dissipation(Pd)**
  - **- Thermal resistance(θ_{JA})**
- **Output voltage deviation**
  - **- Output ripple**
  - **- Load Transient**
- **Compensation**
  - **- Bulk capacitor**
  - **- OCP**
- **Enpirion products**

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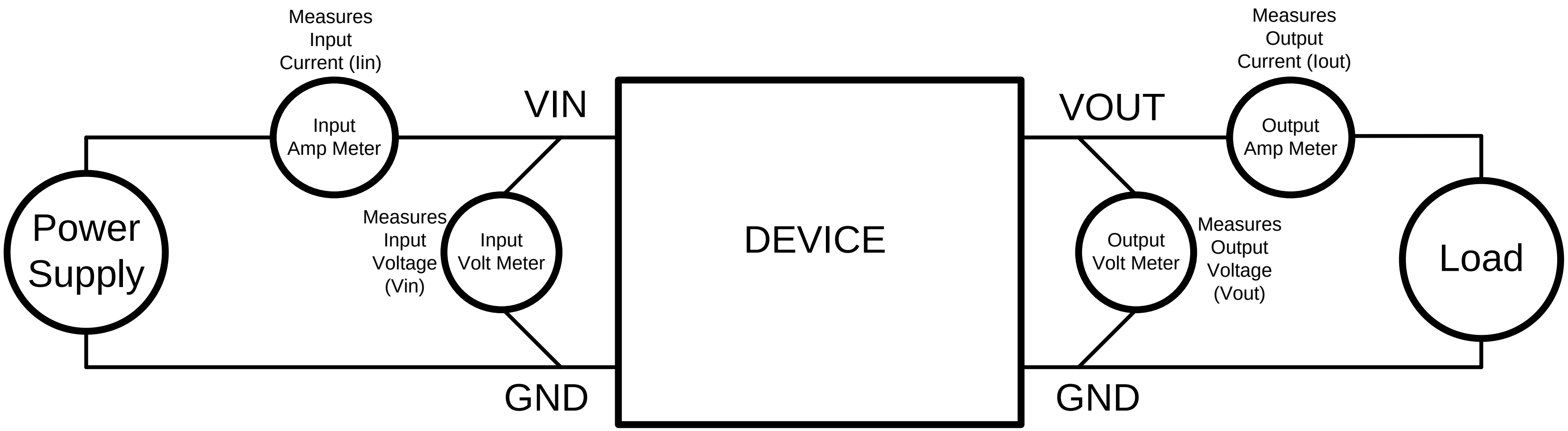
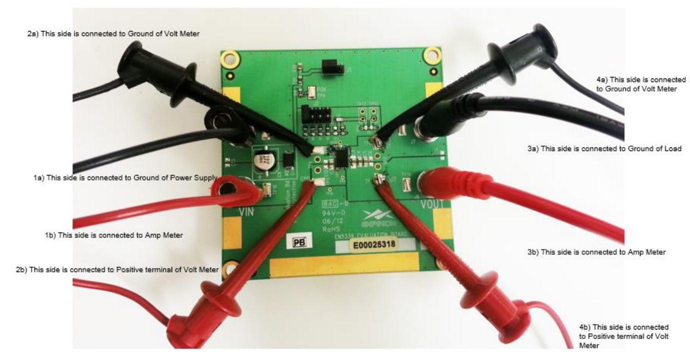
Efficiency

- Power dissipation
- Thermal resistance

Efficiency - Measuring Efficiency Diagram



1) Measure Input Current with series Amp Meter
2) Measure Input Voltage with Volt Meter
3) Measure Output Current with series Amp Meter
4) Measure Output Voltage with Volt Meter
5) Efficiency = (Vout x Iout) / (Vin x Iin) * 100



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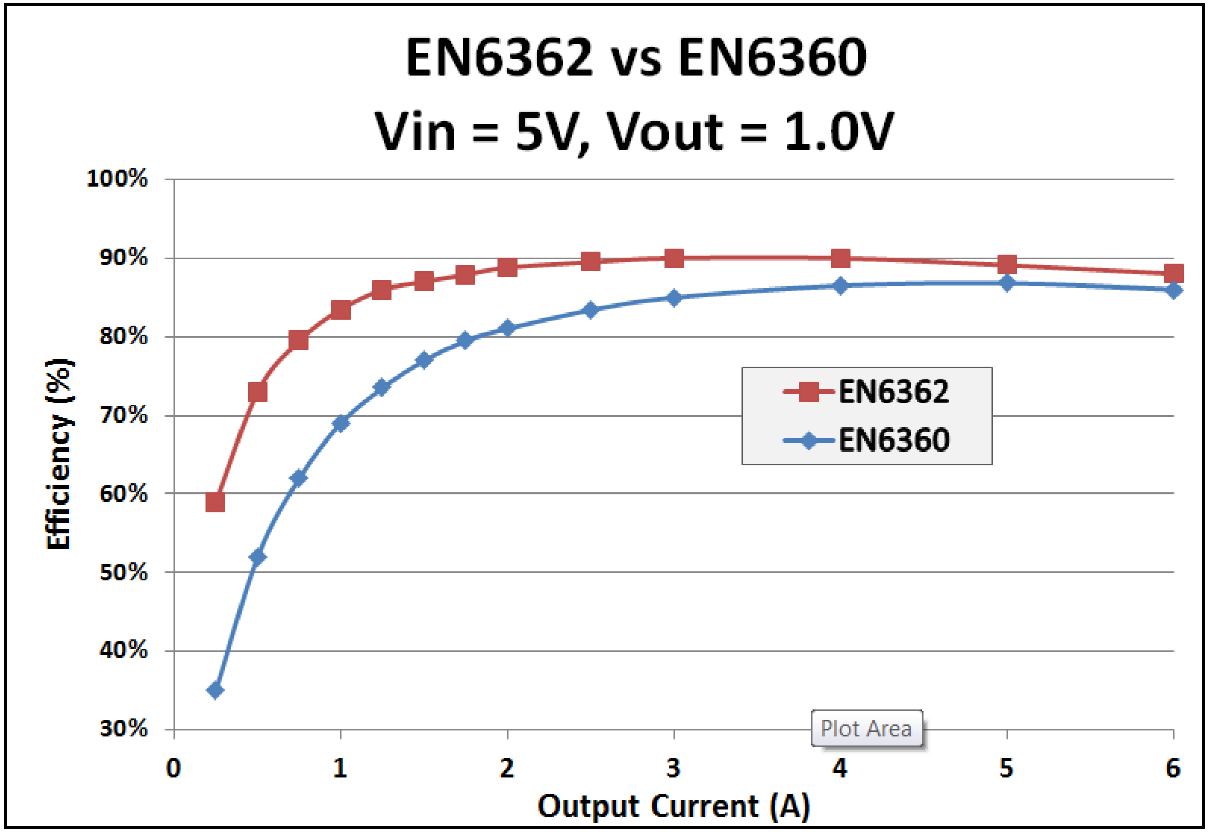
Efficency



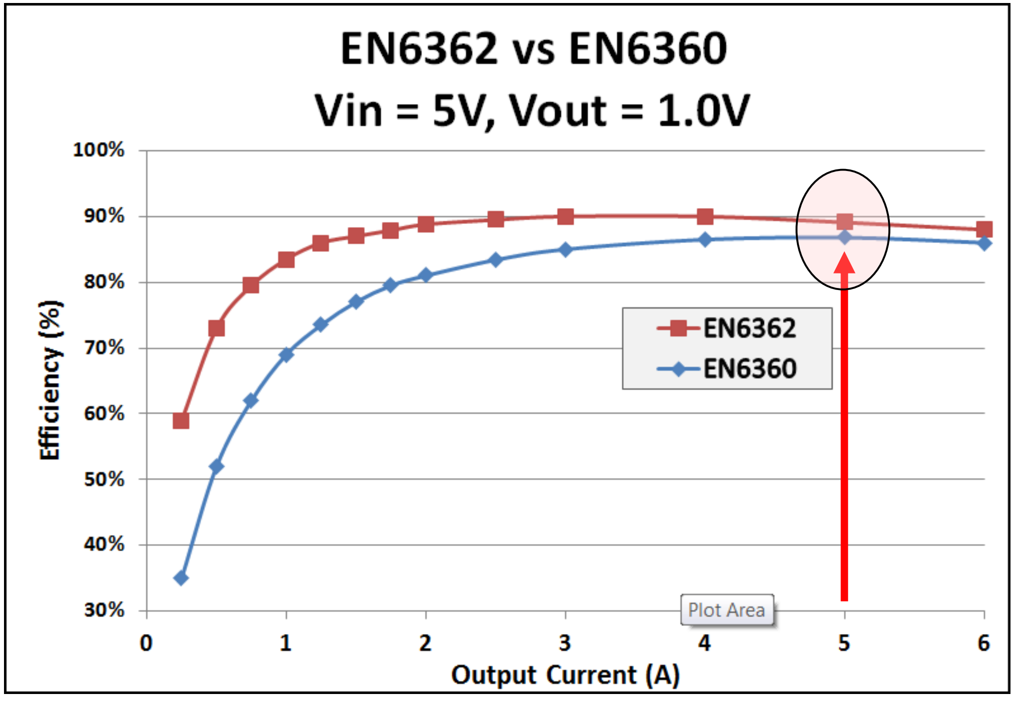
- **EN6362 Efficiency Exceeding EN6360**
  - By 2.0% @ 6.0A
  - By 10% @ 1.5A
  - By 21% @ 0.5A

Efficiency – Estimation Pd

Example: EN6362QI

V_{IN} = 5V
V_{OUT} = 1.0V
I_{OUT} = 5A
First calculate the output power.
P_{OUT} = 1V x 5A = 5W

efficiency (η) shown.
For V_{IN} =5V, V_{OUT} = 1.0V at 5A, η ≈ 90%
η = P_{OUT} / P_{IN} = 90% => 0.9
P_{IN} = P_{OUT} / η
P_{IN} ≈ 5W / 0.9 ≈ 5.56W



Pd = Pin – Pout = 5.56W - 5W = 0.56W(손실 발생)

Efficency – Thermal Resistance θ_{JA}

Example: EN6362QI

1. **Pd** = Pin – Pout = 5.56W - 5W = **0.56W**
2. theta JA value (θ_{JA})
   - EN6362QI(6A) has a 16 °C/W without airflow
   - This parameter estimate how much the temperature will rise in the device

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	3.0	6.5	V
Output Voltage Range	V_{OUT}	0.60	$V_{IN} – V_{DO}$ [2]	V
Operating Junction Temperature	T_J	-40	+125	°C

Thermal Characteristics

PARAMETER	SYMBOL	TYP	UNITS
Thermal Resistance: Junction to Ambient (0 LFM) [3]	θ_{JA}	16	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	1	°C/W
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	25	°C

Efficency – Estimation T_J & T_{AMAX}

Example:EN6362QI

1. Pd = Pin – Pout = 5.56W - 5W = 0.56W(열손실 발생)
2. theta JA value (θ_{JA}) : 16 °C/W
3. Determine the change in temperature (ΔT) based on P_D and θ_{JA}.

   $\Delta T = P_D \times \theta_{JA}$

   $\Delta T \approx 0.56W \times 16°C/W = 8.96°C$

4. The junction temperature **(T_J) = T_A + ΔT**

   $T_J \approx 25°C + 8.96°C \approx 34°C$

5. The maximum operating junction temperature (T_{JMAX}) of the device is 125°C, so the device can operate at a higher ambient temperature.

The maximum ambient temperature (T_{AMAX}) allowed can be calculated.

$T_{AMAX} = T_{JMAX} – P_D \times \theta_{JA}$

$\approx 125°C – 8.96°C \approx 116°C$

The maximum ambient temperature the device can reach is 116°C given the input and output conditions.

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Output voltage Deviation

- Output ripple
- Load transient

Output ripple

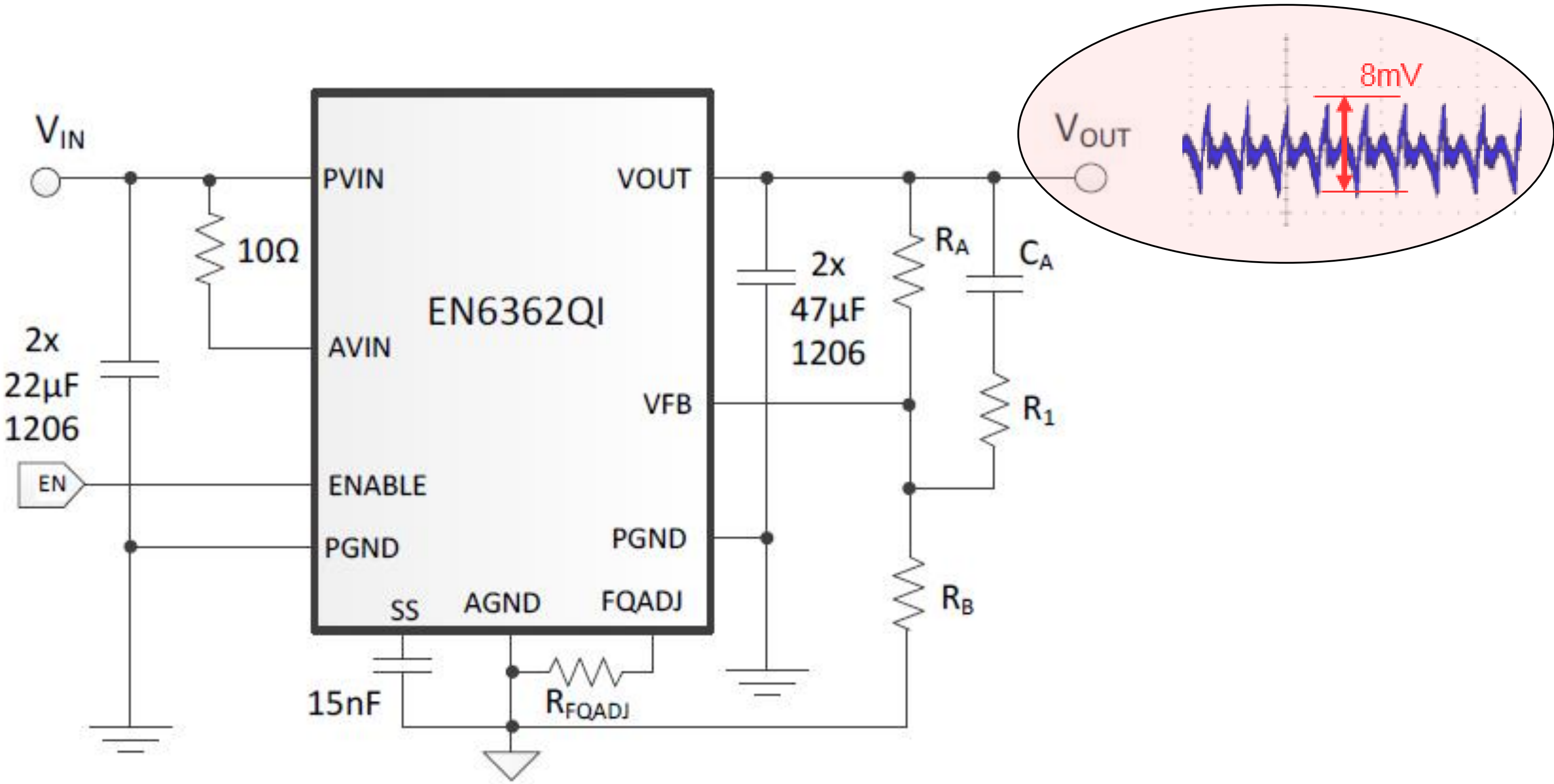


Figure 1: Simplified Applications Circuit

Output ripple

- **Example : EN6362QI(6A)**
  - DC-DC PWM noise
  - Output ripple ≈ 8mV~

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Switching Frequency	F_{SW}	R_{FADJ} = 6.98kΩ, V_{IN} = 5V	0.9	1.2	1.5	MHz

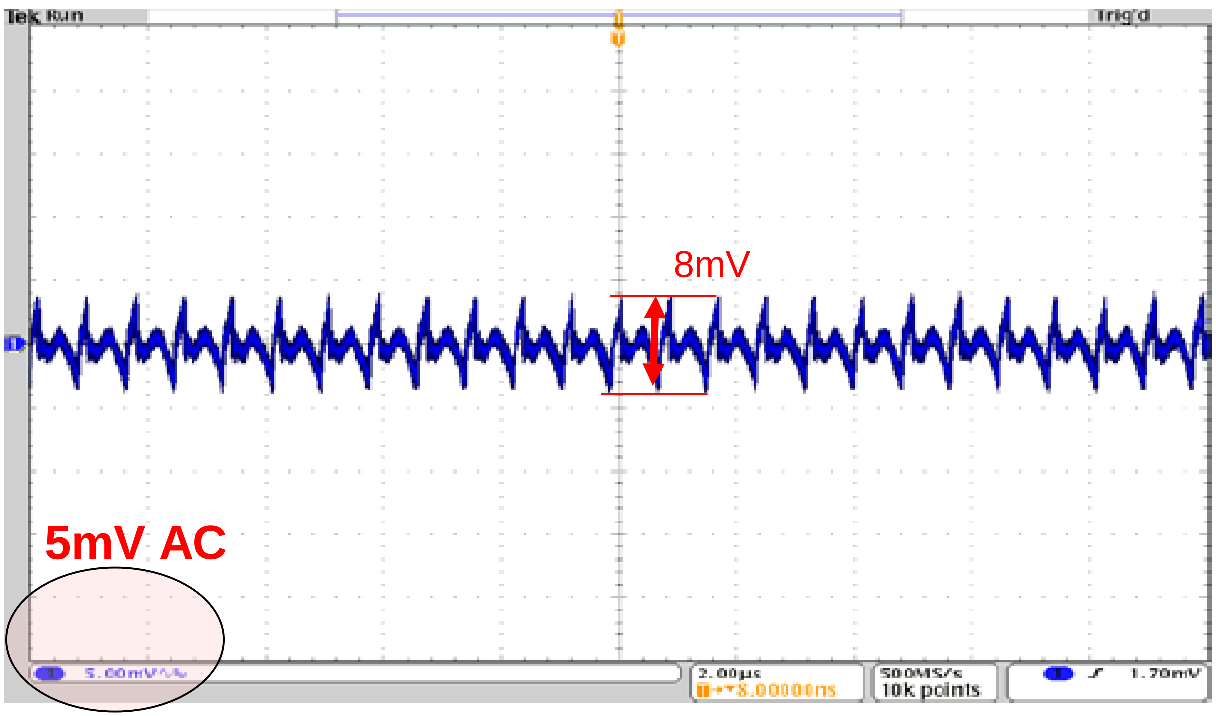


Figure 12: Output ripple V_{IN} = 5V, V_{OUT} = 1V

Output ripple – Capacitor

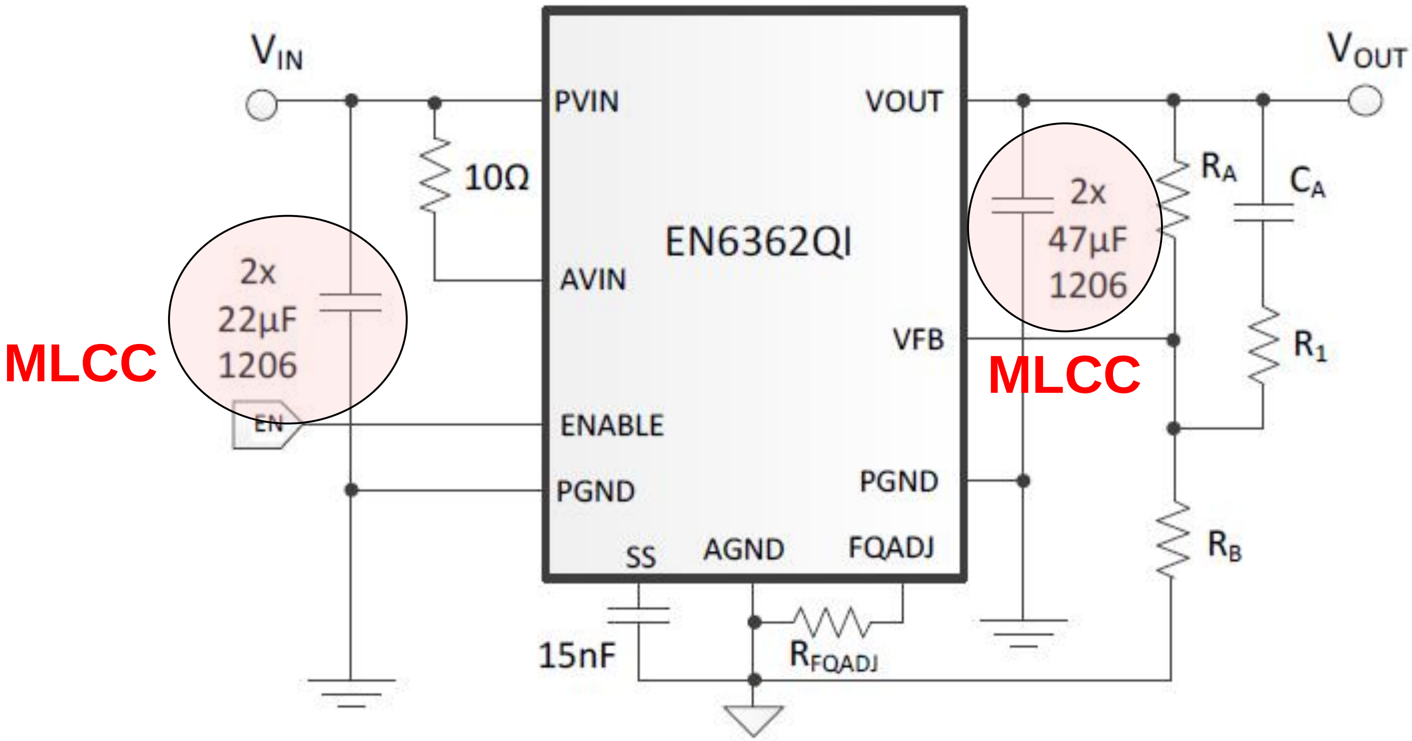
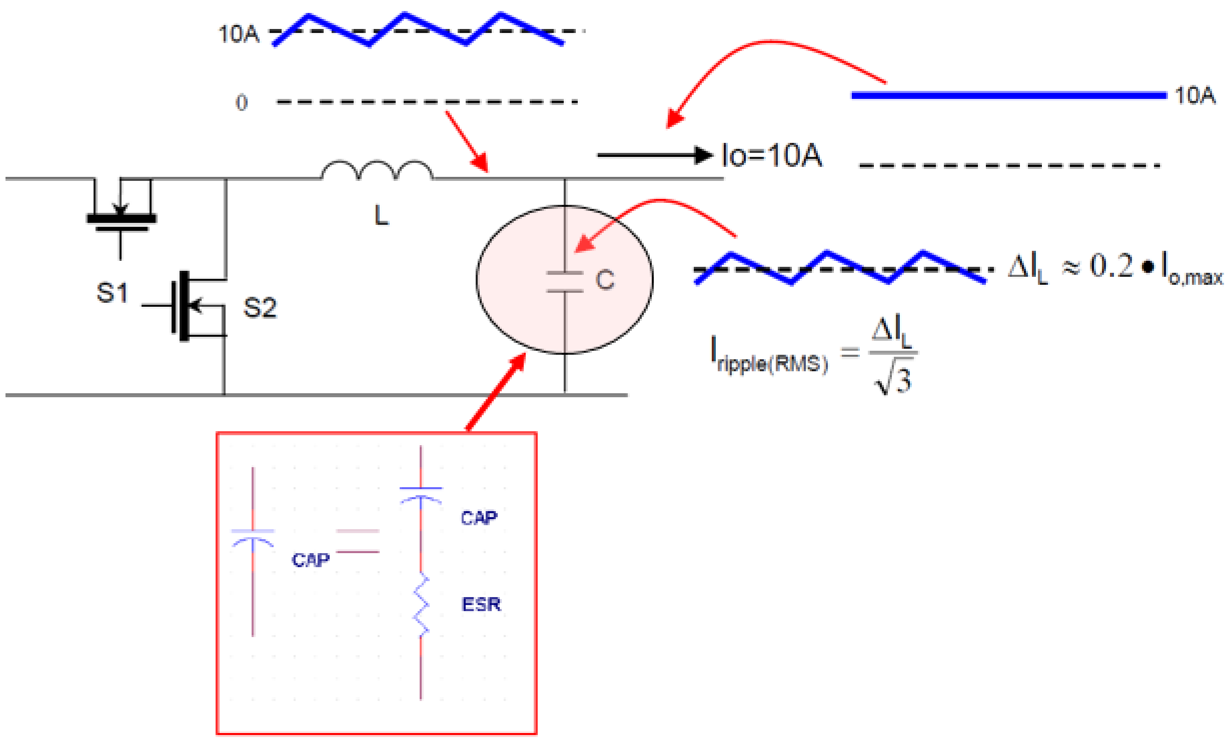


Figure 1: Simplified Applications Circuit

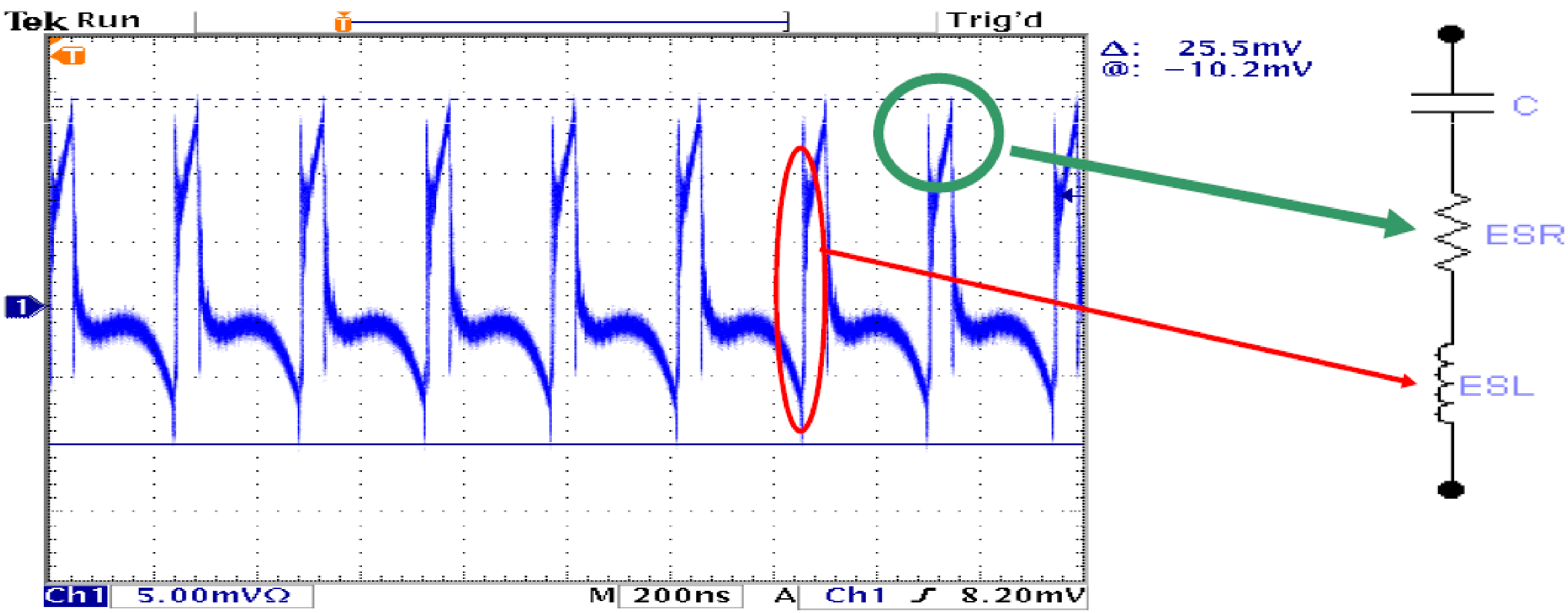
Output ripple – Output capacitor(Cout)

- **Output capacitor can reduce ripple noise**



Output ripple – Capacitor ESR & ESL

- It depends on the inductor and the output impedance of the output capacitor @ the switching frequency.
- ESL is one of the biggest contributor to the ripple **(Poor layout will increase this value.)**



Output ripple – Capacitor Reducing ESR

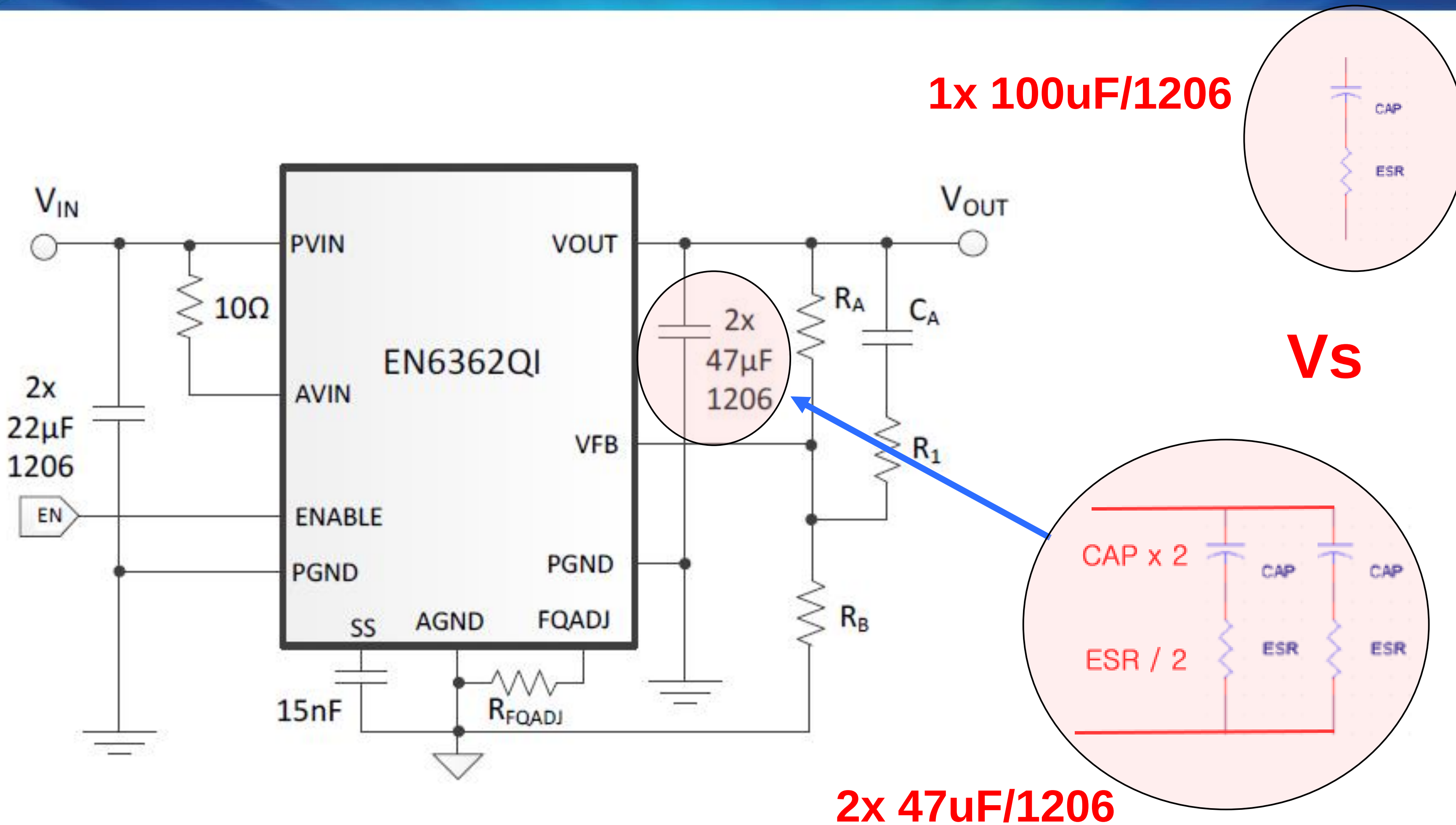
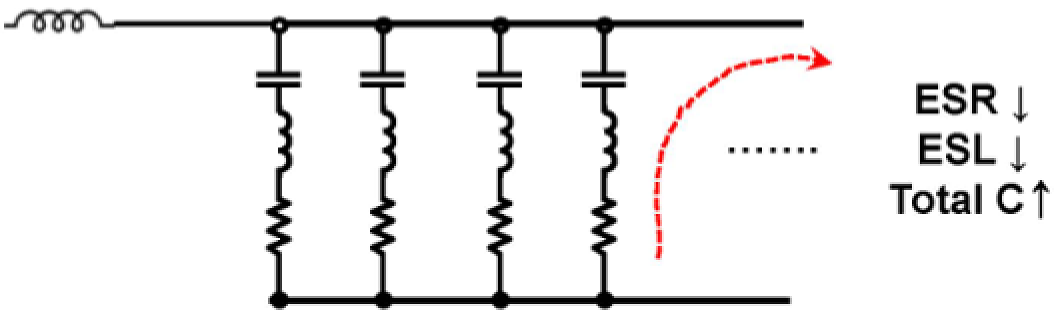


Figure 1: Simplified Applications Circuit

Output ripple – Output capacitor

- **Output capacitor can reduce ripple noise**



Capacitor ESR/ESL → Voltage Ripple

To lower the equivalent ESR/ESL

– Use low ESR/ESL capacitor → Cost

– R_{total} = ESR/n, n = number of capacitors

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Output ripple – Capacitor Size

- **Example : EN6362QI(6A)**

Table 1: Recommended Input Capacitors

Description	MFG	P/N
22µF, 10V, 20% X5R, 1206 (2 capacitors needed)	Murata	GRM31CR61A226ME19L
	Taiyo Yuden	LMK316BJ226ML-T

Table 2: Recommended Output Capacitors

Description	MFG	P/N
47µF, 10V, 20% X5R, 1206 (2 capacitors needed)	Taiyo Yuden	LMK316BJ476ML-T
47µF, 6.3V, 20% X5R, 1206 (2 capacitors needed)	Murata	GRM31CR60J476ME19L
	Taiyo Yuden	JMK316BJ476ML-T
10µF, 6.3V, 10% X7R, 0805 (Optional 1 capacitor in parallel with 2x47uF)	Murata	GRM21BR70J106KE76L
	Taiyo Yuden	JMK212B7106KG-T

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Output ripple – Capacitor size

- **Capacitance drop**

Nominal Cap Value	Case Size	Thickness	Voltage Rating	Measured Value at 0V DC Bias freg>100kHz	% Capacitance Drop (Typical)	
					3V DC Bias	5V DCBias
10uF	0603	0.8mm	6.3V	5.2uF	45%	67%
	0805	1.25mm	10V	7uF	20%	40%
	1206	1.6mm	10V	10uF	5%	12%
	1210	2mm	25V	10uF	2%	5%
22uF	0805	1.25mm	6.3V	12uF	33%	55%
	1206	1.6mm	6.3V	19uF	15%	33%
	1210	2.5mm	16V	19uF	1%	8%
47uF	1206	1.6mm	6.3V	35uF	33%	60%
	1210	2.5mm	6.3V	43uF	12%	28%
	1812	2.5mm	6.3V	47uF	10%	20%

Table 1: Comparison of various ceramic cap values and case sizes

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Deviation – Load Transient

- **Example : EN6362QI(6A)**
  - Pk-Pk : 80mV
  - Rispond time : 16uS @ 0A to 6A loading

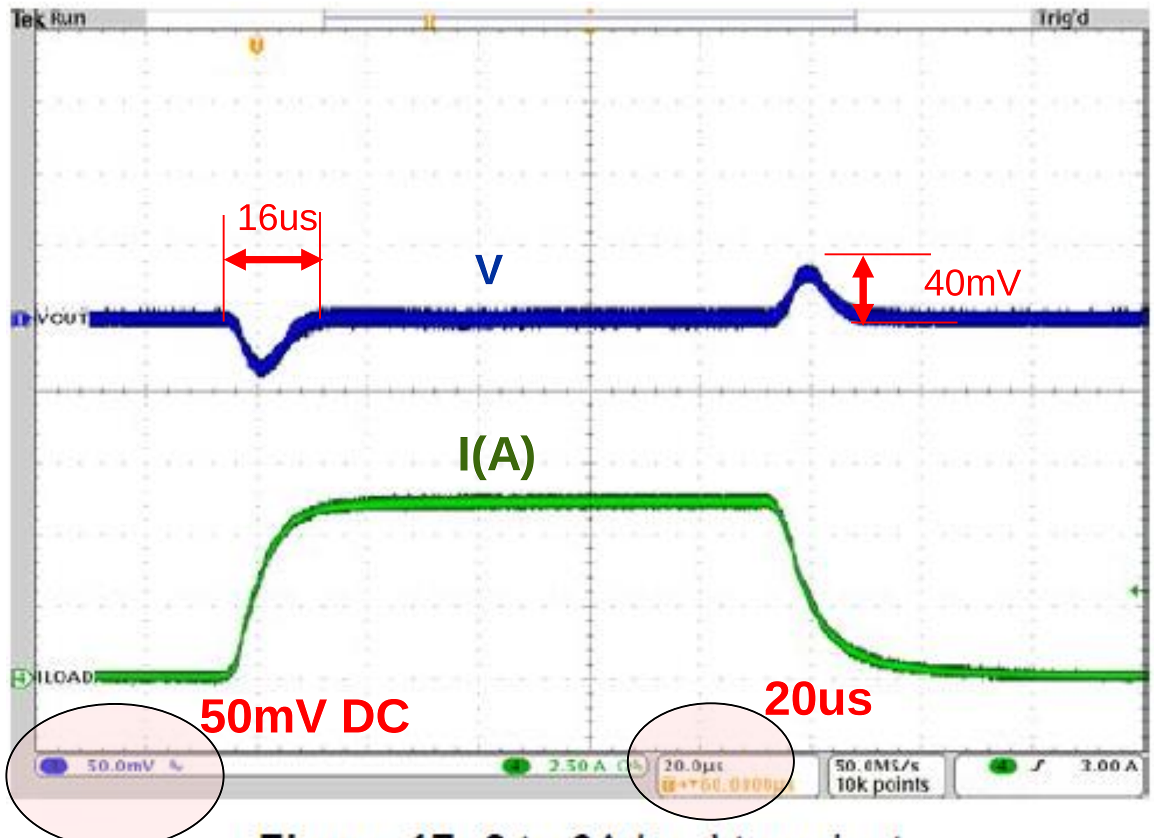
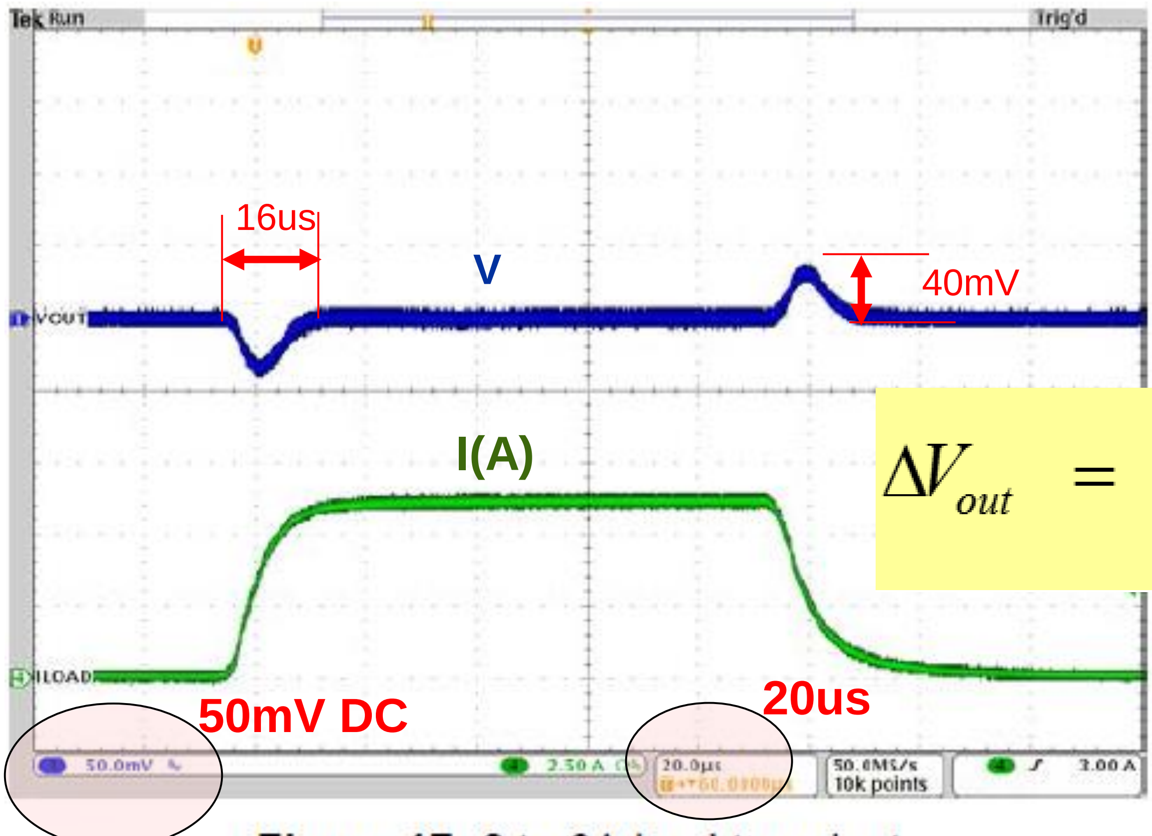


Figure 17: 0 to 6A load transient

Deviation – Load Transient

- **Example : EN6362QI(6A)**
  - Pk-Pk : 80mV
  - Rispond time : 16uS @ 0A to 6A loading



$$\Delta V_{out} = \frac{\Delta I_{load}}{8.BW.C_{out}}$$

Figure 17: 0 to 6A load transient

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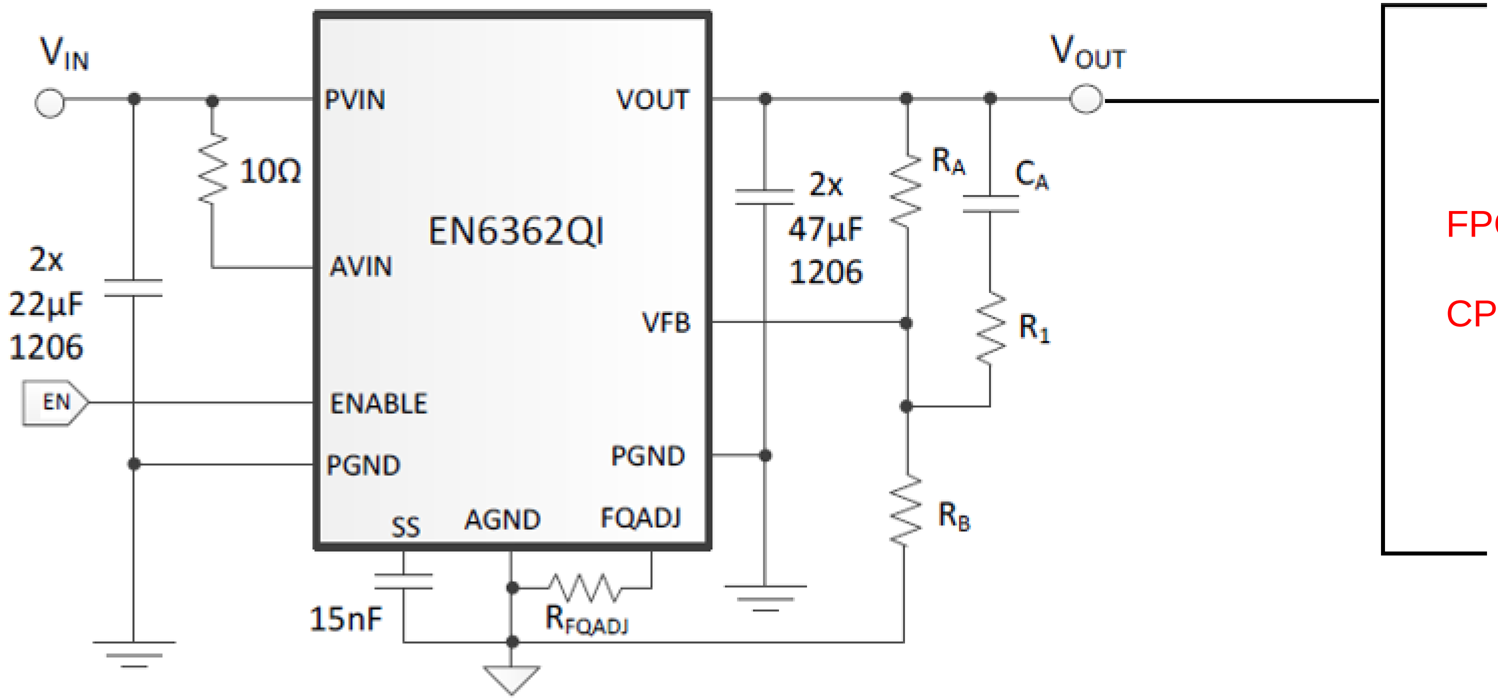
Compensation circuit

- Bulk Capacitor
- Measuring Bode Plot
- OCP(Over current protection)

Bulk Capacitor



Bulk Capacitor

- **Why we need Bulk capacitor?**
  - Reduce Ripple !
  - Supplying current during Load Transient !
  - Reduce switching noise !
  - Manufacturer's requirement.

Whatever the reason, you might need adjusting the BW and Soft Start time – Why?

1) The Power inductor + Output Capacitor = Double poles at low frequency

= Phase lag by 180 Deg

= **Unstable system**

2) The OCP might trip if the bulk capacitor current exceeds the OCP level:

$$I_{CBulk} = C_{Bulk} \frac{dV}{dt}$$

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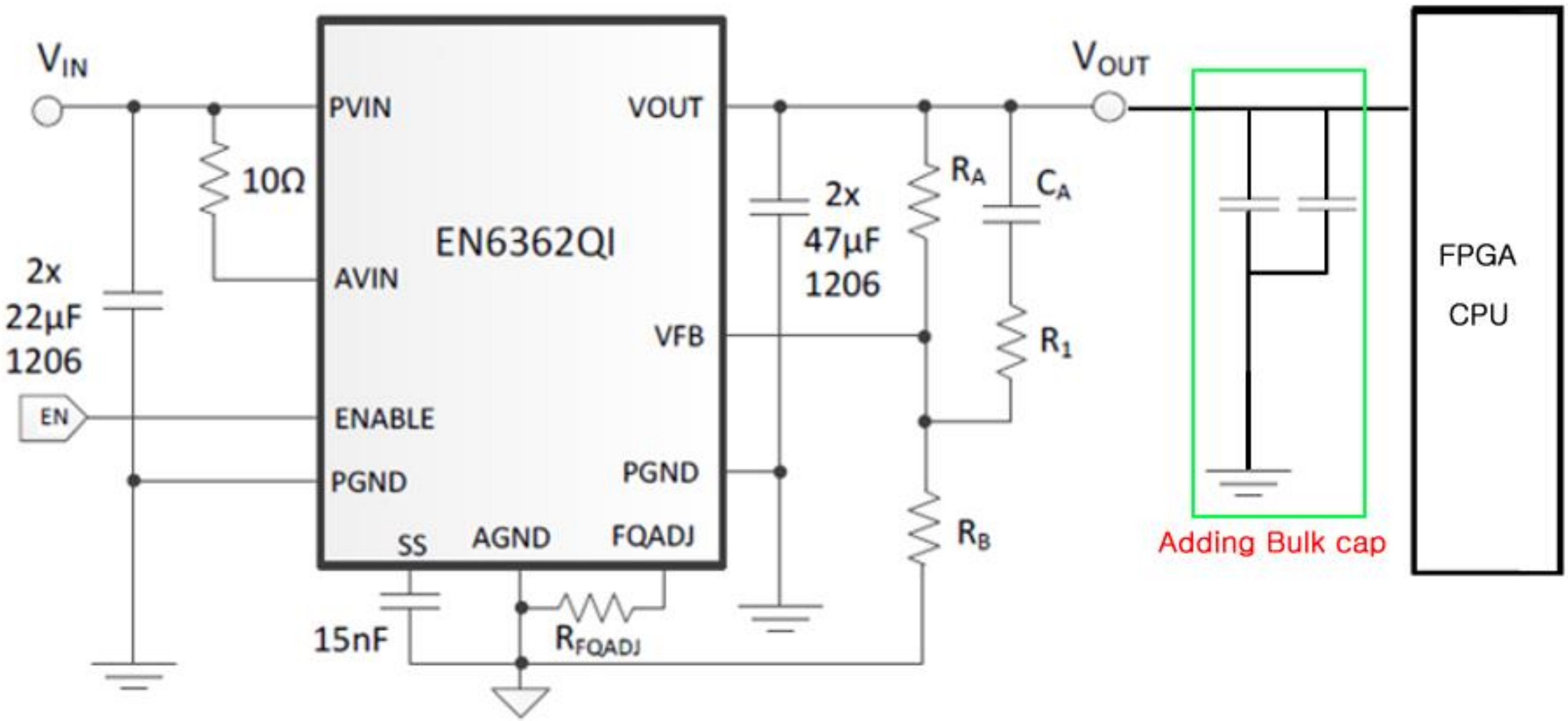
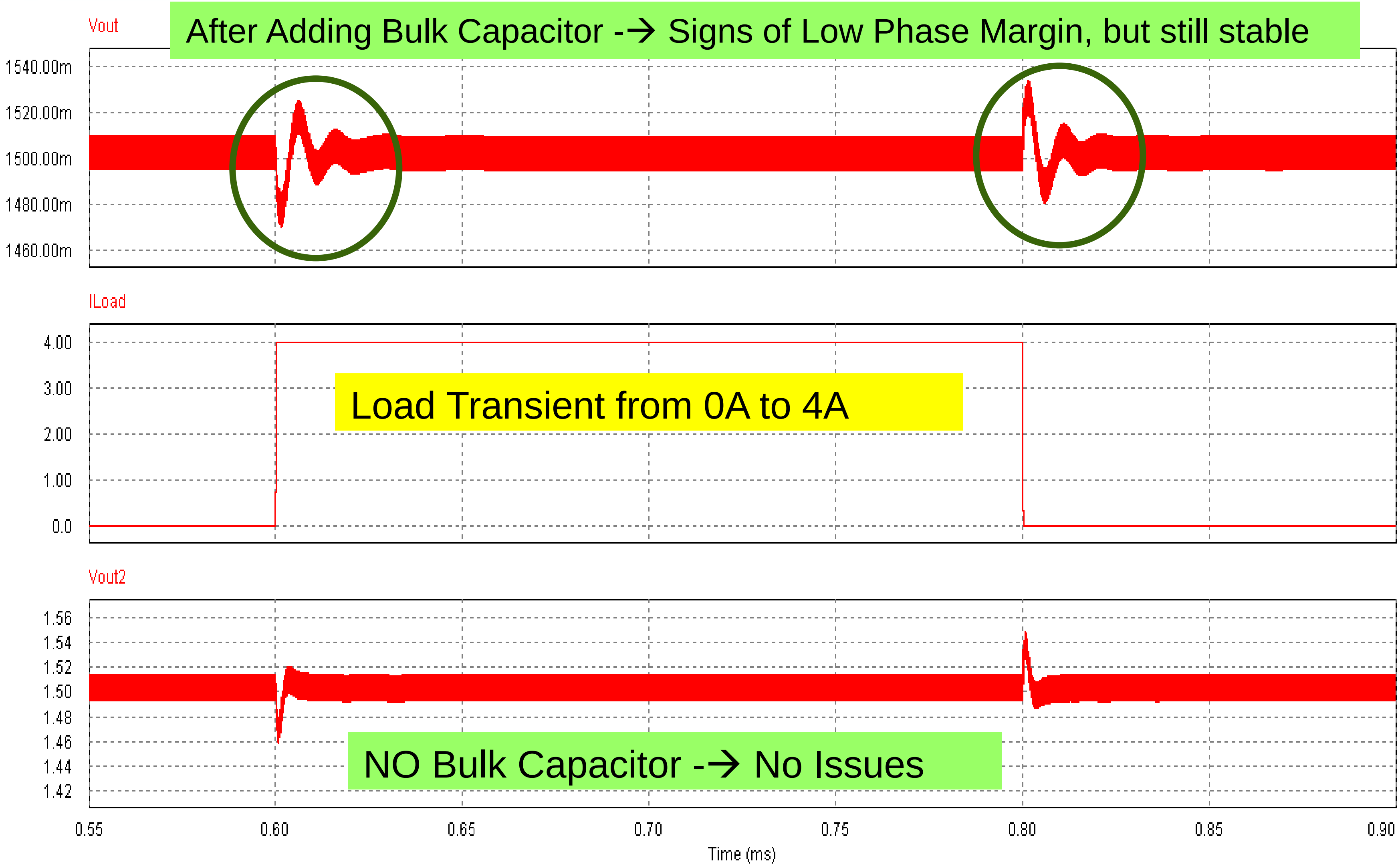
Bulk Capacitor



Bulk Capacitor Vs. Stability: Output waveforms during Load Transient



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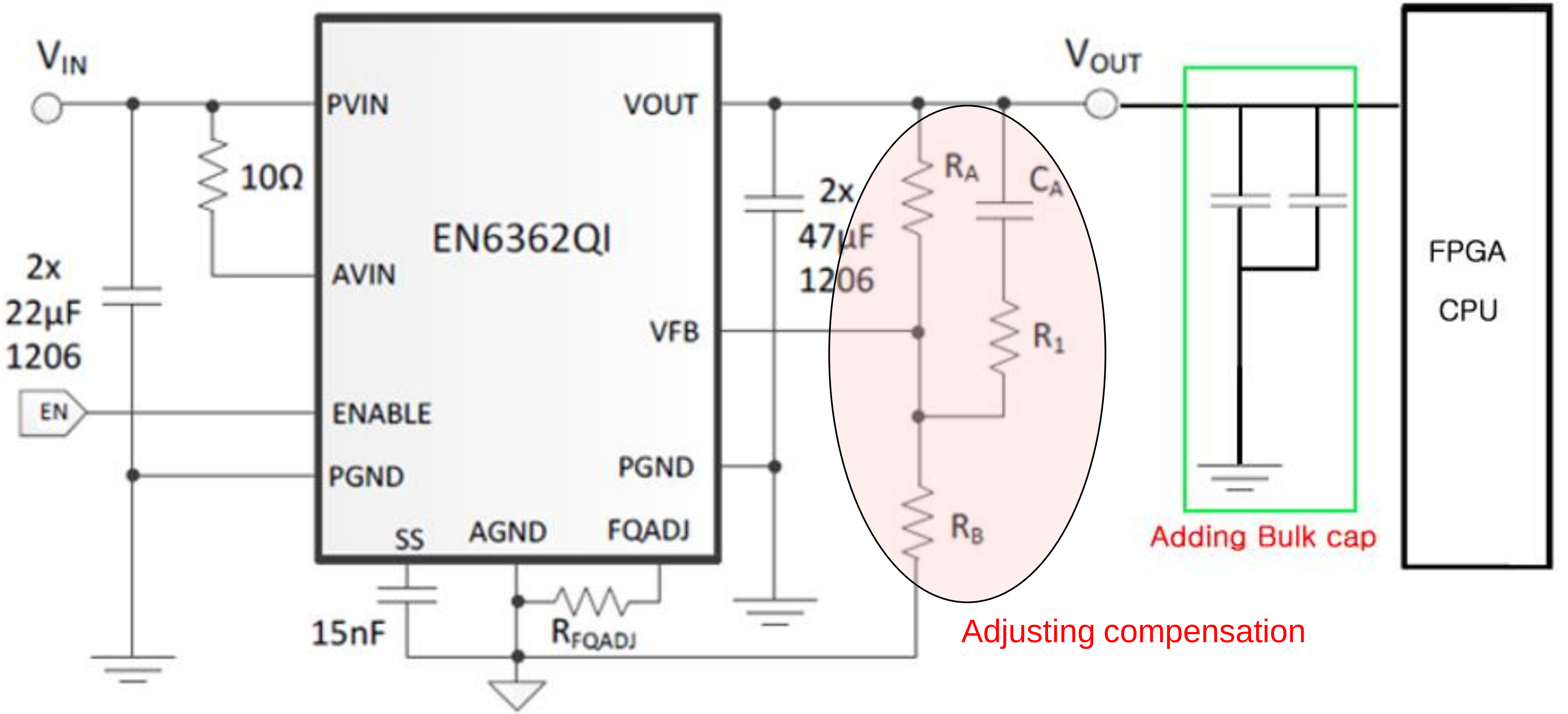
Compensation circuit



Basic Relationships between deviation and Cout

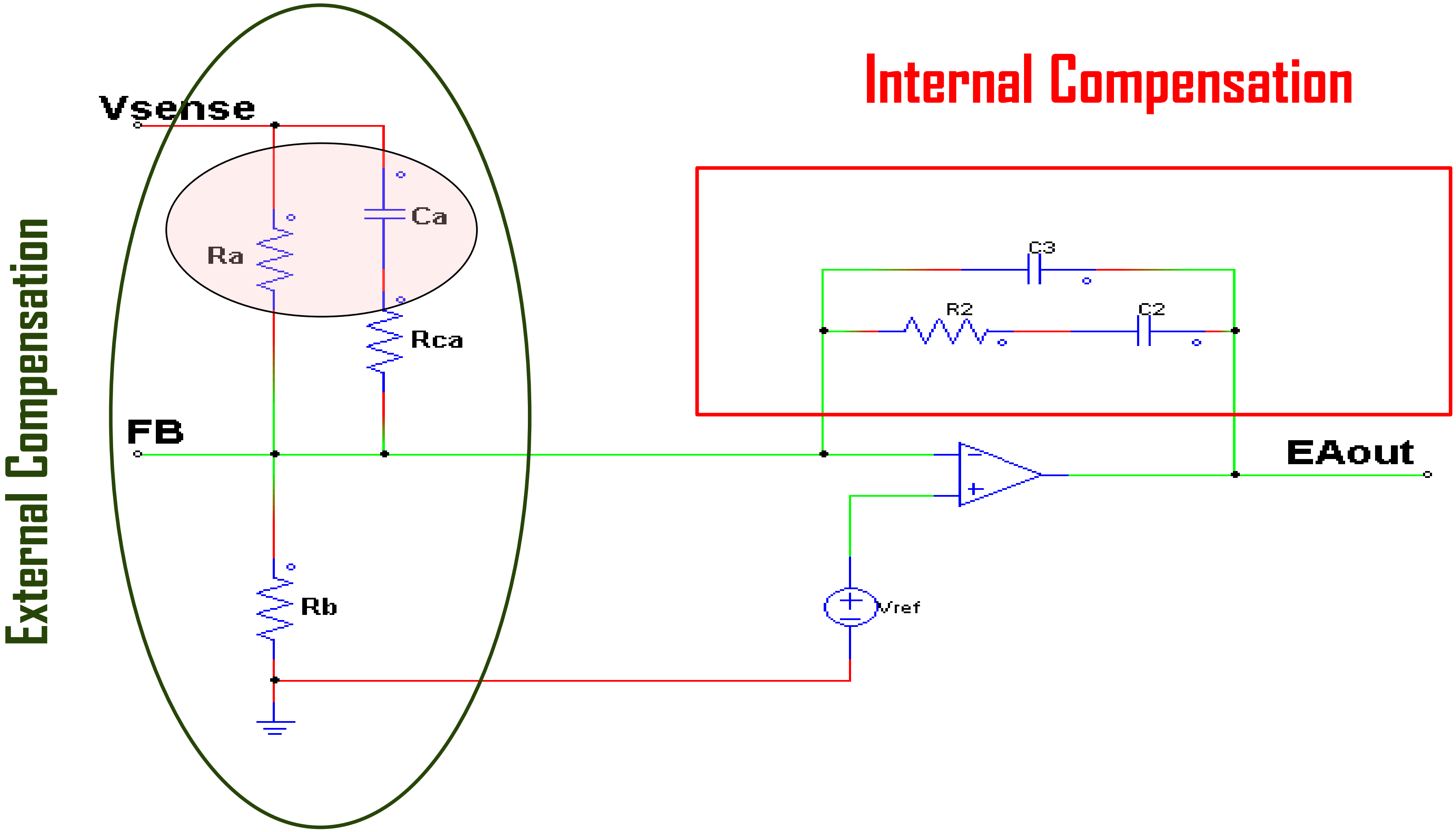
- **Loop Band Width (BW) as a function of Output capacitor (Cout) and power Inductor**

$$BW \quad \alpha \quad \frac{1}{\sqrt{L_{out} . C_{out}}} \qquad \text{Eq.1}$$

- Output voltage deviation (ΔVout) as a function of load step (ΔI_{load}), BW, and Cout

$$\Delta V_{out} \quad \alpha \quad \frac{\Delta I_{load}}{8 . BW . C_{out}} \qquad \text{Eq.2}$$

Compensation circuit



Compensation Vs, Bulk Capacitor

- **Handling Bulk Capacitor:**
  - **Adjusting the compensation components:**
    - Increase Ca in 20% step. Check load transient performance, and Vdrain or Vout waveform. Look for oscillation or sign of oscillation.
    - <u>OR</u>: Increase Ra in 20% step. Check load transient performance, and Vdrain or Vout waveform. Look for oscillation or sign of oscillation..
    - Measuring Bode Plot using Frequency analyzer is the best way to check the system Stability.

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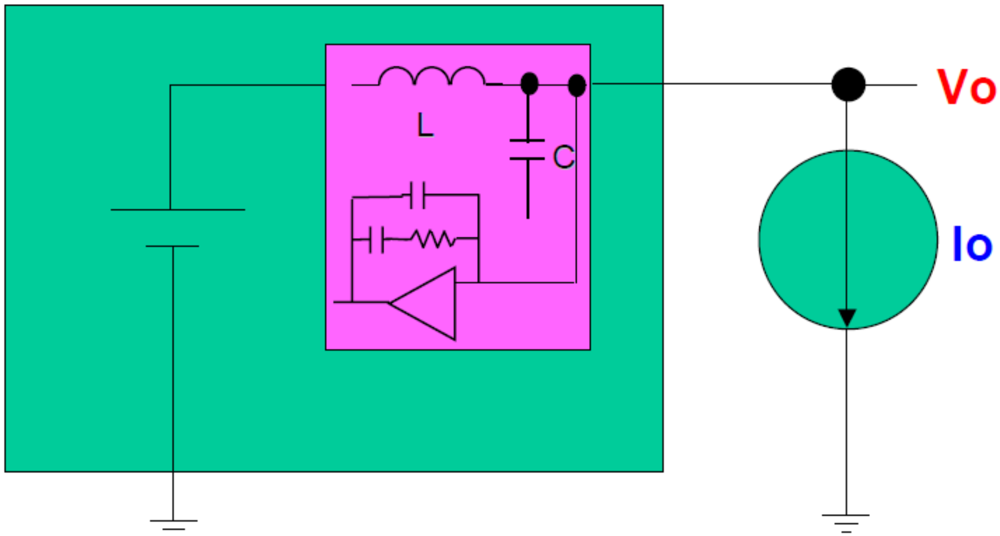
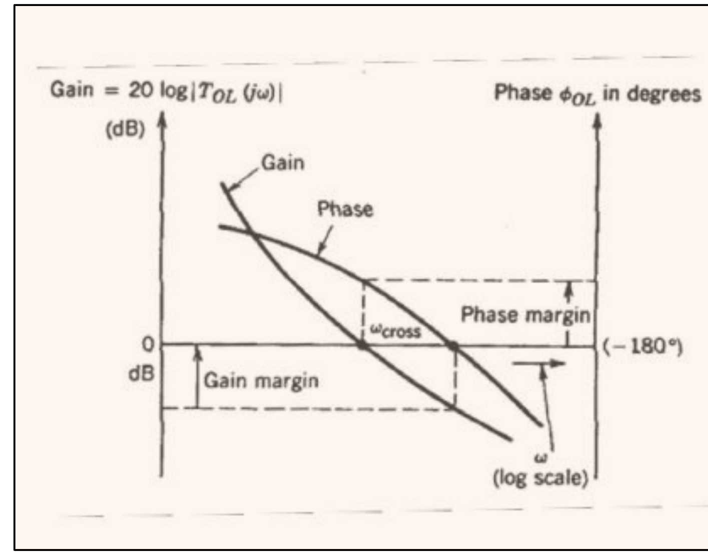
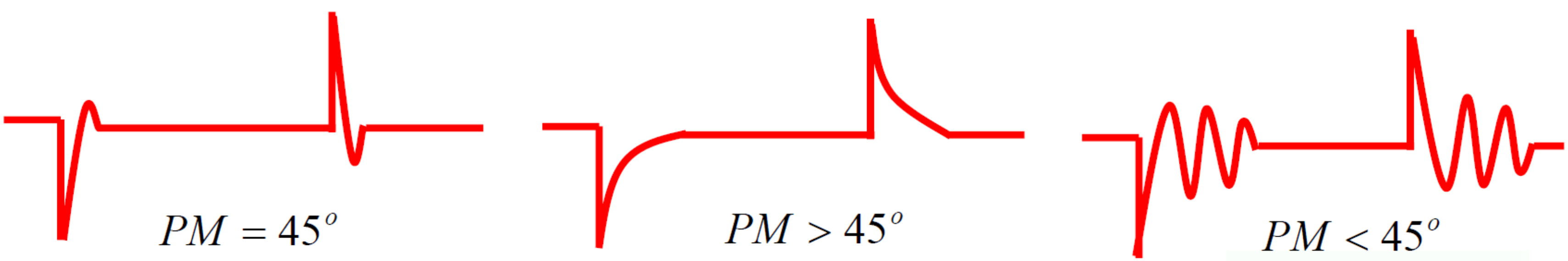
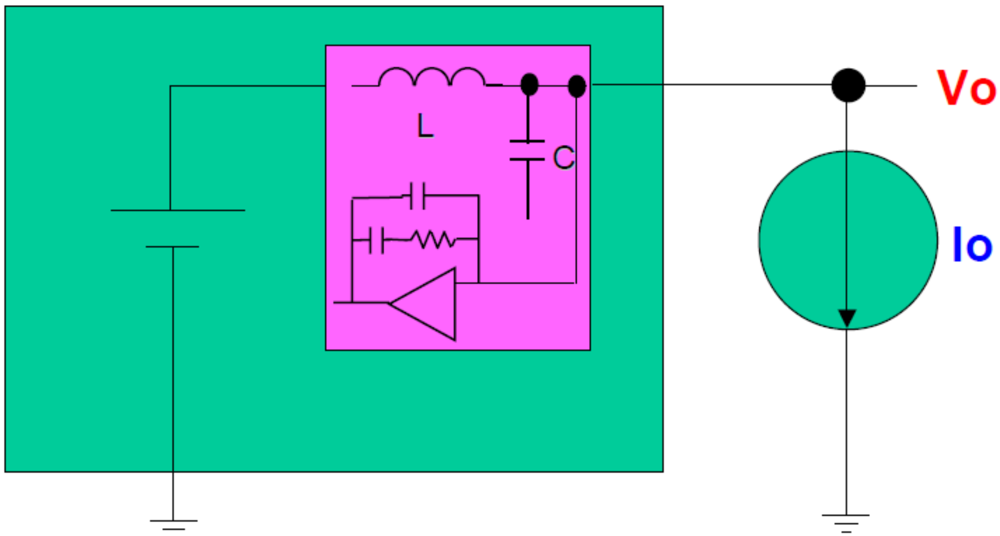
Measuring Bode Plot

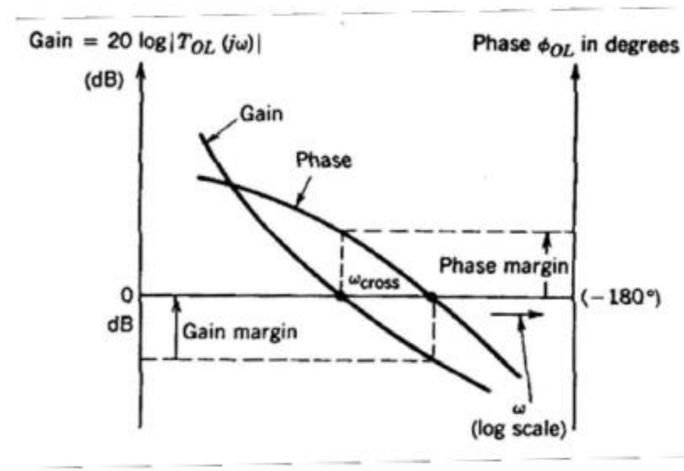


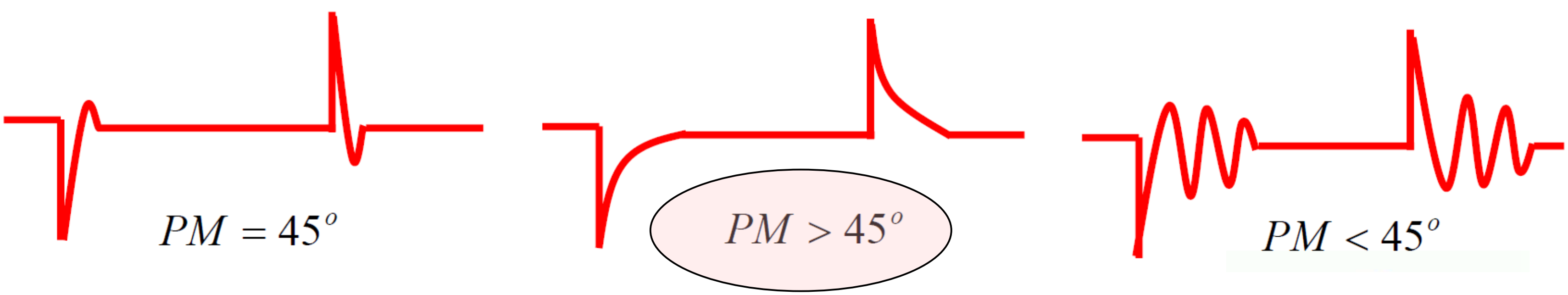




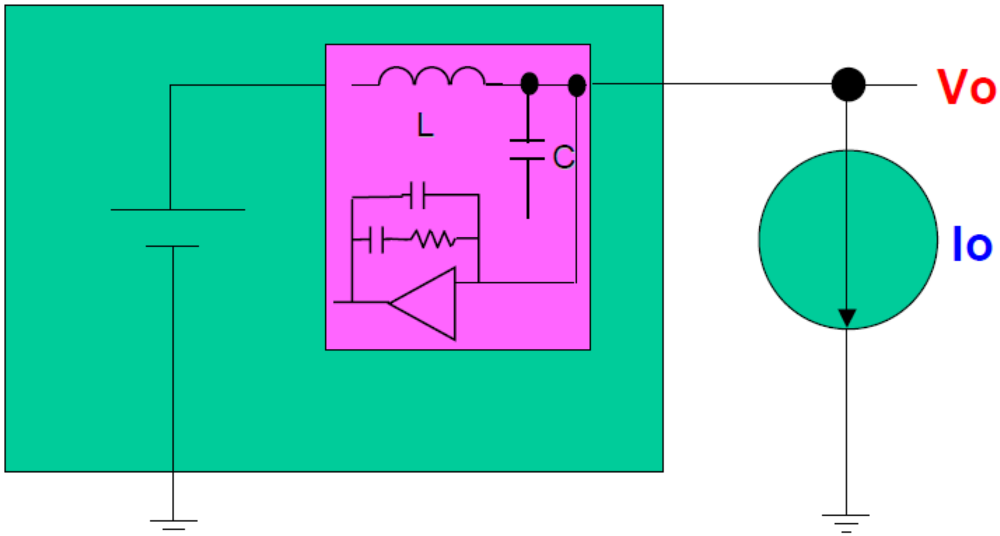
Measuring Bode Plot

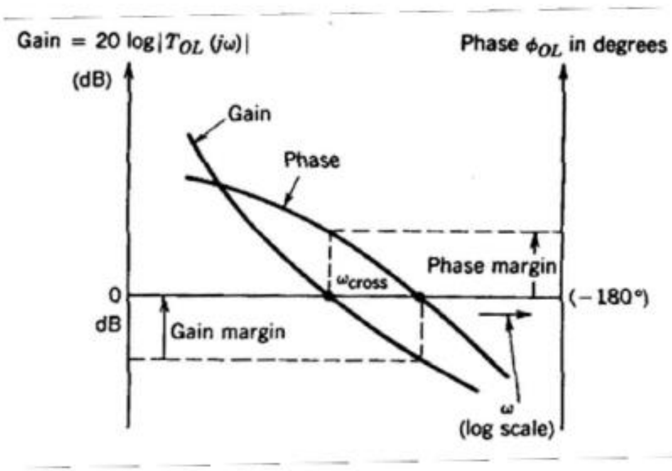


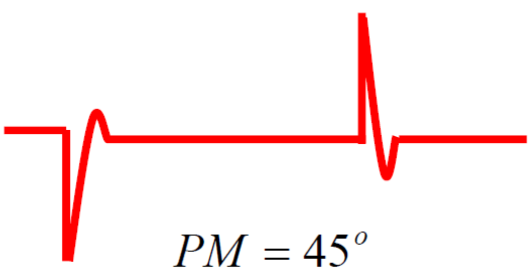




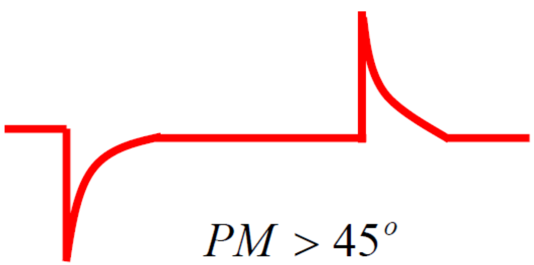
Measuring Bode Plot



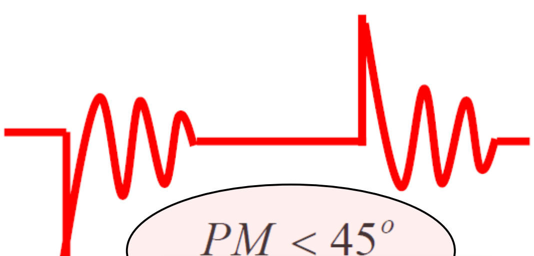




$PM = 45^o$

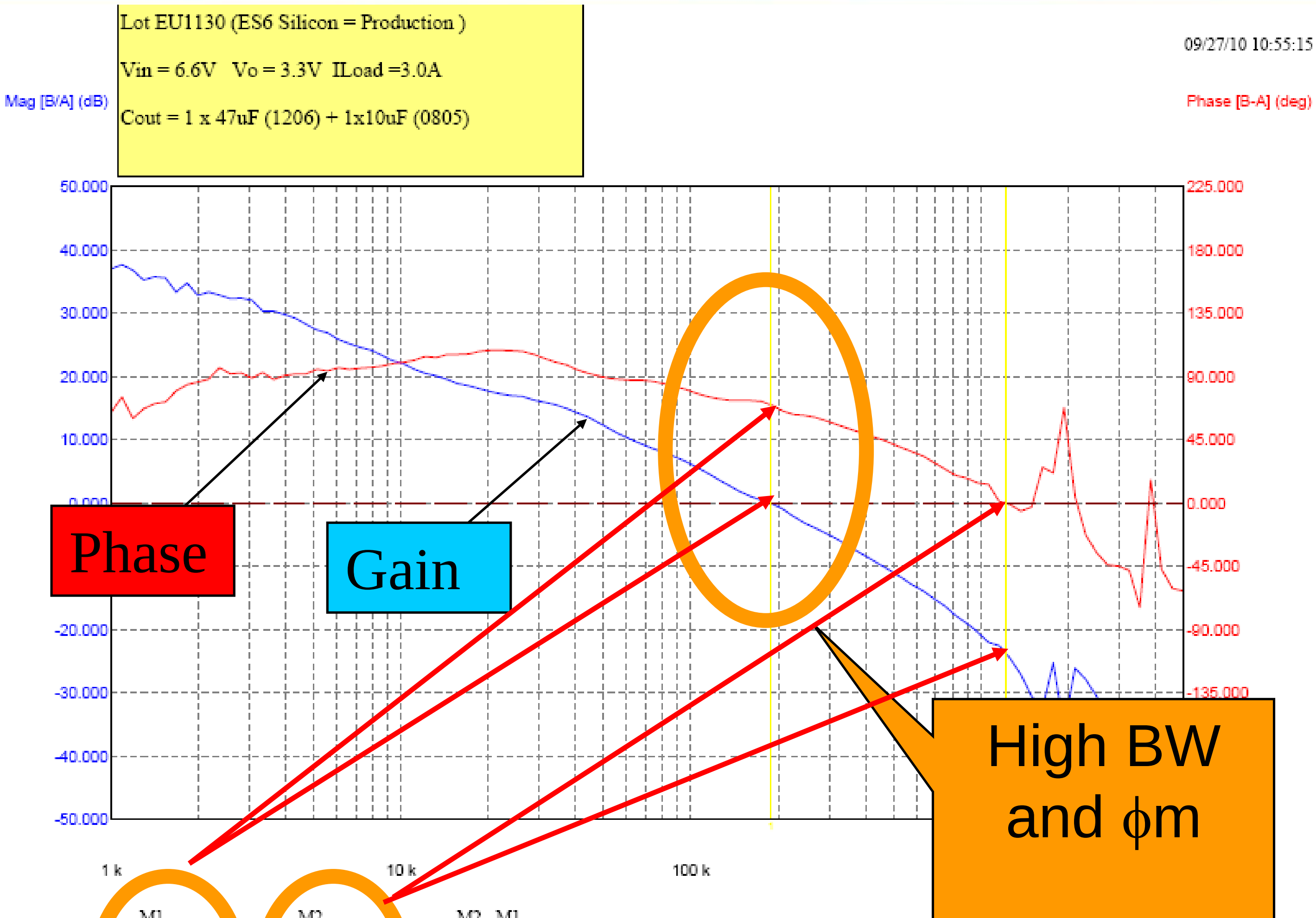


$PM > 45^o$



$PM < 45^o$

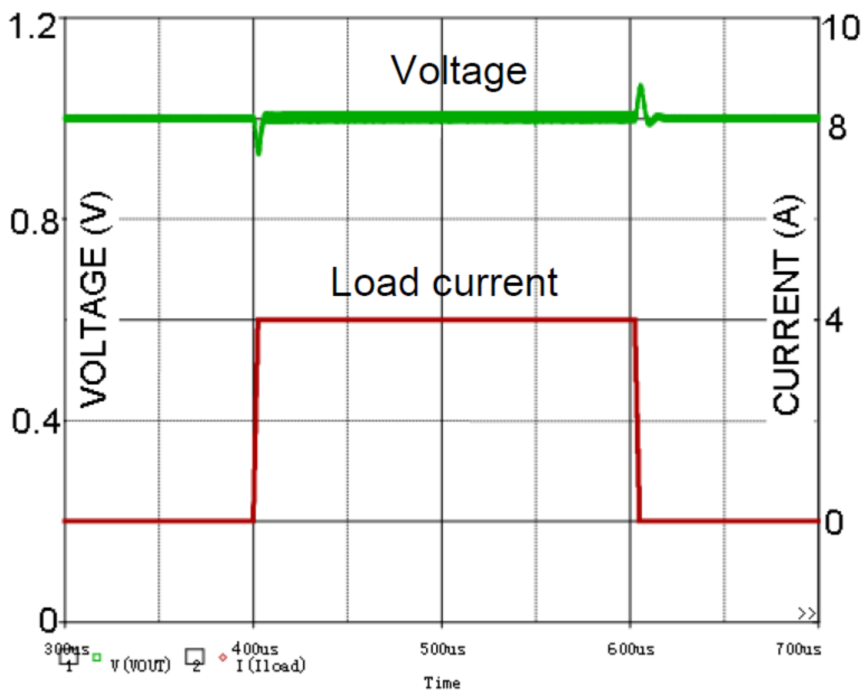
EN6337 Bode Plot

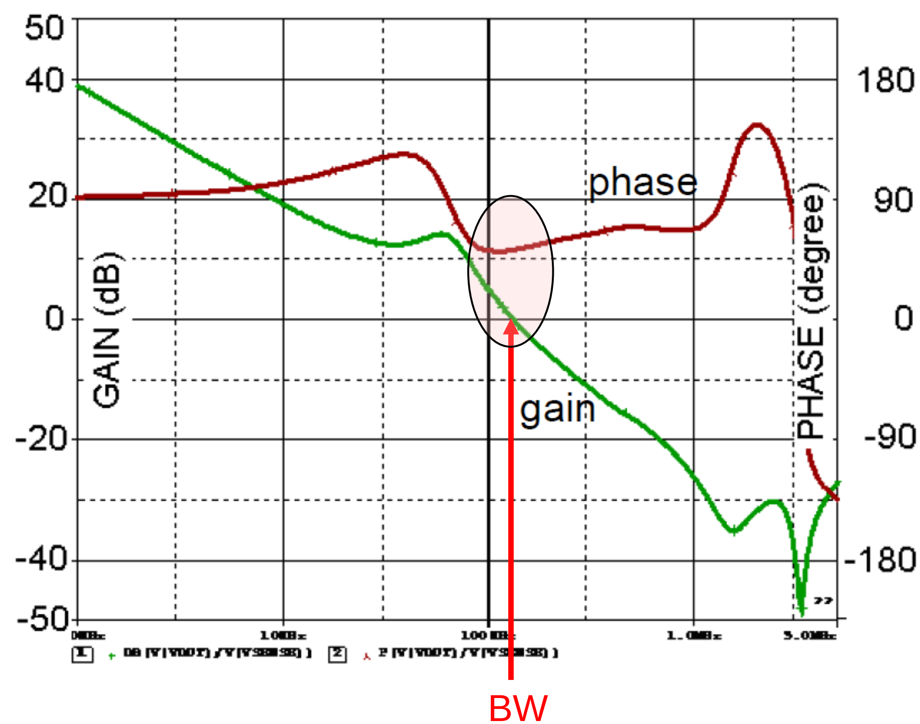


	M1	M2	M2 - M1
Frequency	189.25 kHz	1.23 MHz	1.04 MHz
Magnitude	-0.041 dB	-23.835 dB	-23.795 dB
Phase	69.783 deg	-0.194 deg	-69.976 deg
Ref (Mag)	0.000 dB	0.000 dB	0.000 dB
Ref (Phase)	0.000 deg	0.000 deg	0.000 deg
Delta (Mag)	-0.041 dB	-23.835 dB	
Delta (Phase)	69.783 deg	-0.194 deg	

Vout Stability & Bode Plot

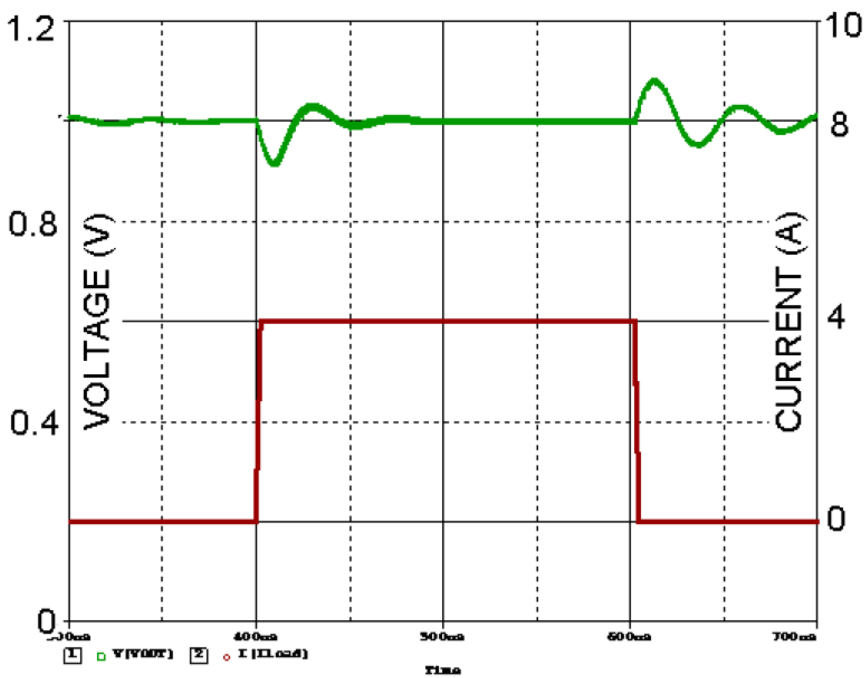
- **Without extra bulk capacitors**

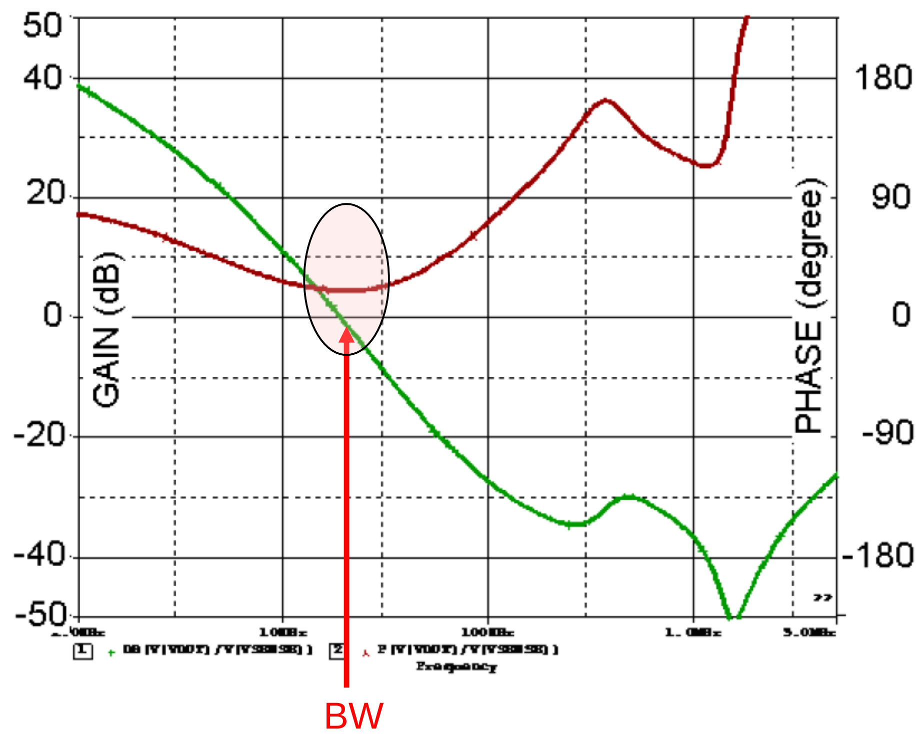




Vout stability & Bode Plot

- **With extra bulk capacitors**





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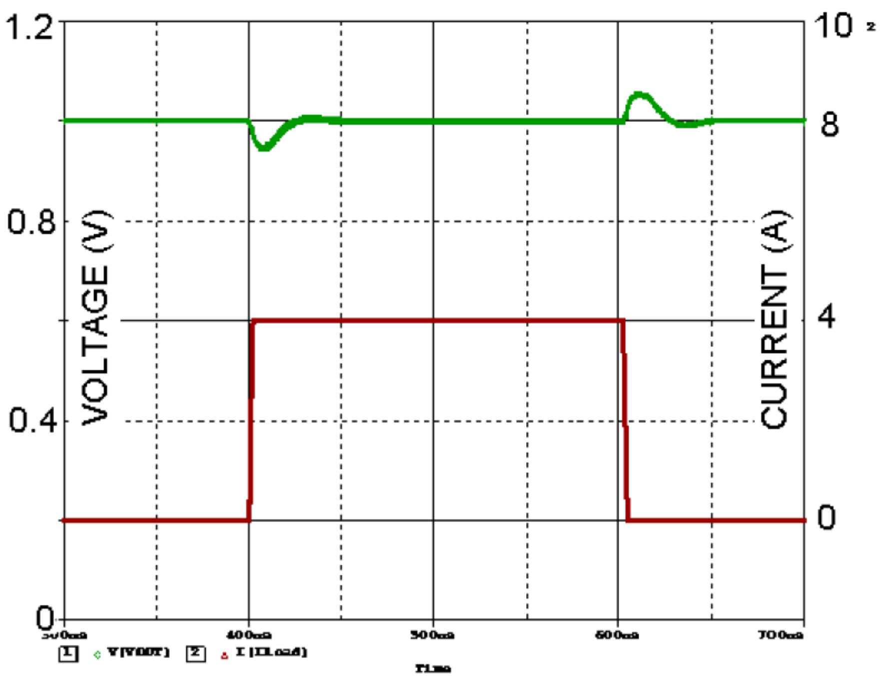
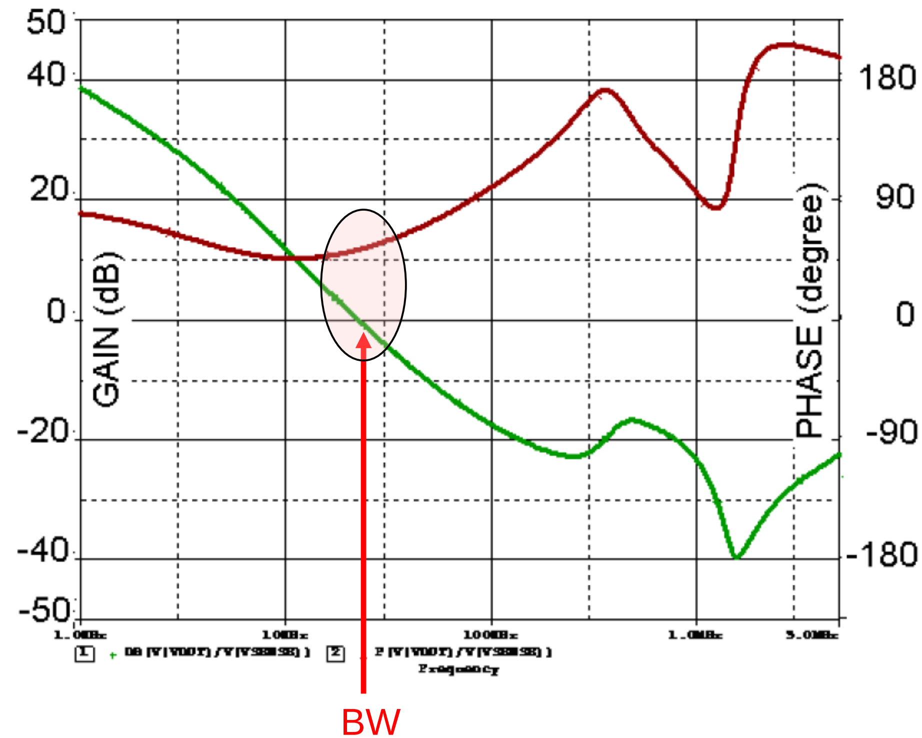
Vout stability & Bode Plot

- **With extra bulk capacitors and adjusting the loop**





Bulk Capacitor Vs OCP(Over current Protection)

- **Example : EN6362QI(6A)**
  - OCP level : 8A(Min)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VFB Pin Voltage	V_{FB}	T_A =-40°C to 85°C, 3V ≤ V_{IN} ≤ 6.5V, I_{LOAD} = 0A to 6A	0.591	0.600	0.609	V
		T_A =-40°C to 105°C, 3V ≤ V_{IN} ≤ 6.5V, I_{LOAD} = 0A to 6A	0.588	0.600	0.612	V
VFB Pin Input Leakage Current	I_{VFB}	VFB Pin Input Leakage Current	-10		+10	nA
Shut-Down Supply Current	I_{SD}	Power Supply Current with ENABLE=0		0.7		mA
Under Voltage Lock-out (V_{IN} Rising)	V_{UVLOR}	Voltage Above Which UVLO is Not Asserted		2.3		V
Under Voltage Lock-out (V_{IN} Falling)	V_{UVLOF}	Voltage Below Which UVLO is Asserted		2.0		V
Drop Out Voltage	V_{DO}	V_{IN} = 3V, V_{OUT} set 3.3V, I_{LOAD} = 6A, 100% duty cycle		210	450	mV
Drop Out Resistance	R_{DO}	Input to Output Resistance		35	75	mΩ
Over Current Trip Level	I_{OCP}	Sourcing Current	8	14	17	A
Switching Frequency	F_{SW}	R_{FADJ} = 6.98kΩ, V_{IN} = 5V	0.9	1.2	1.5	MHz

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Bulk Capacitor Vs OCP

- **OCP and Soft Start:**

Example: Iocp = 6A, Cbulk = 1mF, SS_Cap has been chosen for 1msec soft start time, Vout = 3.3V:

$$I_{CBulk} = C_{Bulk}\frac{dV}{dt} = 1mF\frac{3.3}{1m} = 3.3A$$

If ILoad > 2.7A, The OCP circuit will trip and the part will never start.

Bulk Capacitor Vs OCP

- **Handling Bulk Capacitor:**
  - **Adjusting Soft Start Capacitor:**
    - SS Cap need to be adjust to avoid the OCP trip using the equation provided earlier.

Example of Parameters taken into consideration:

1. **Silicon:**
   1. Resistors
   2. MIM capacitors
   3. Process variation (FF, SS, SF, FS, over temp)
2. **Inductor:**
   1. Inductance variation over all parameters ±20%
   2. The effect of DC resistor and its variation
   3. Continuous monitoring L Vs. I
3. **Output Capacitors:**
   1. Variation over Frequency, and bias voltage
   2. Variation over temperature (X5R, X7R)
   3. Adding more capacitors
4. **Board Layout:**
   1. Adding extra ESL, or ESR
   2. Parasitic added to XFB node (mainly capacitive coupling)
   3. Parasitic at EAout or between EAout and XFB
5. **External components variation:**
   1. Ra, Rb up to ±10%
   2. Ca up to ±30%
6. **Input capacitors**
   1. Variation over Frequency, and bias voltage
   2. Variation over temperature (X5R, X7R)
   3. Adding more capacitors

Breadth:
6 categories with total >22 parameters

Sweeps: performed across all parameter ensuring acceptable variation (<25%)

Validation/team:
PCB with the recommended Layout

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Enpirion PowerSoC

- Roadmap Presentation

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PWM Controller
Inductor
Compensation Circuit

- <=15V DC-DC switching regulators
- 300mA to 15A
- standard product & ASSP
- www.enpirion.com

Target Markets

Enterprise

Telecom

Embedded/ Industrial

Storage/SSD

Test & Measurement

Optical Networking

Hardware/Power Designer Challenges

- Increasing # of power rails
- More function in smaller form factors
- Noise sensitivity & lower power budgets
- Time-to-market Pressures; fewer resources
- While improving <u>Cost & Reliability</u>!

PowerSoC Benefits

- ✓ High efficiency, smallest size
- ✓ Excellent noise/transient performance
- ✓ Simple, low risk power design
- ✓ Highest reliability, fewest components

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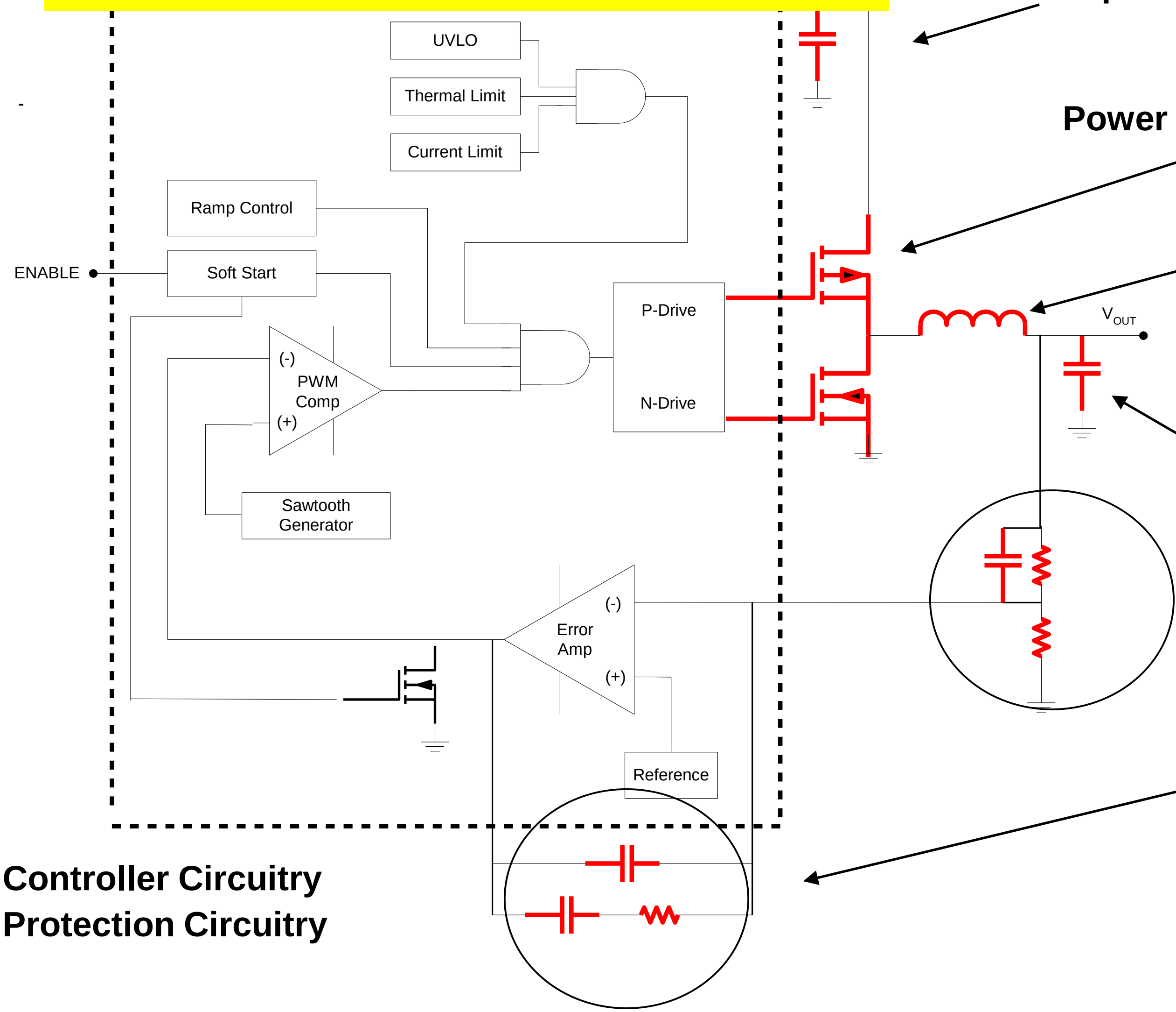
Key Components of a Switch-Mode DC-DC Converter

How do you Make it Smaller?



Input Filter Capacitor(s)

Power MOSFETS (Switches)

Power Inductor

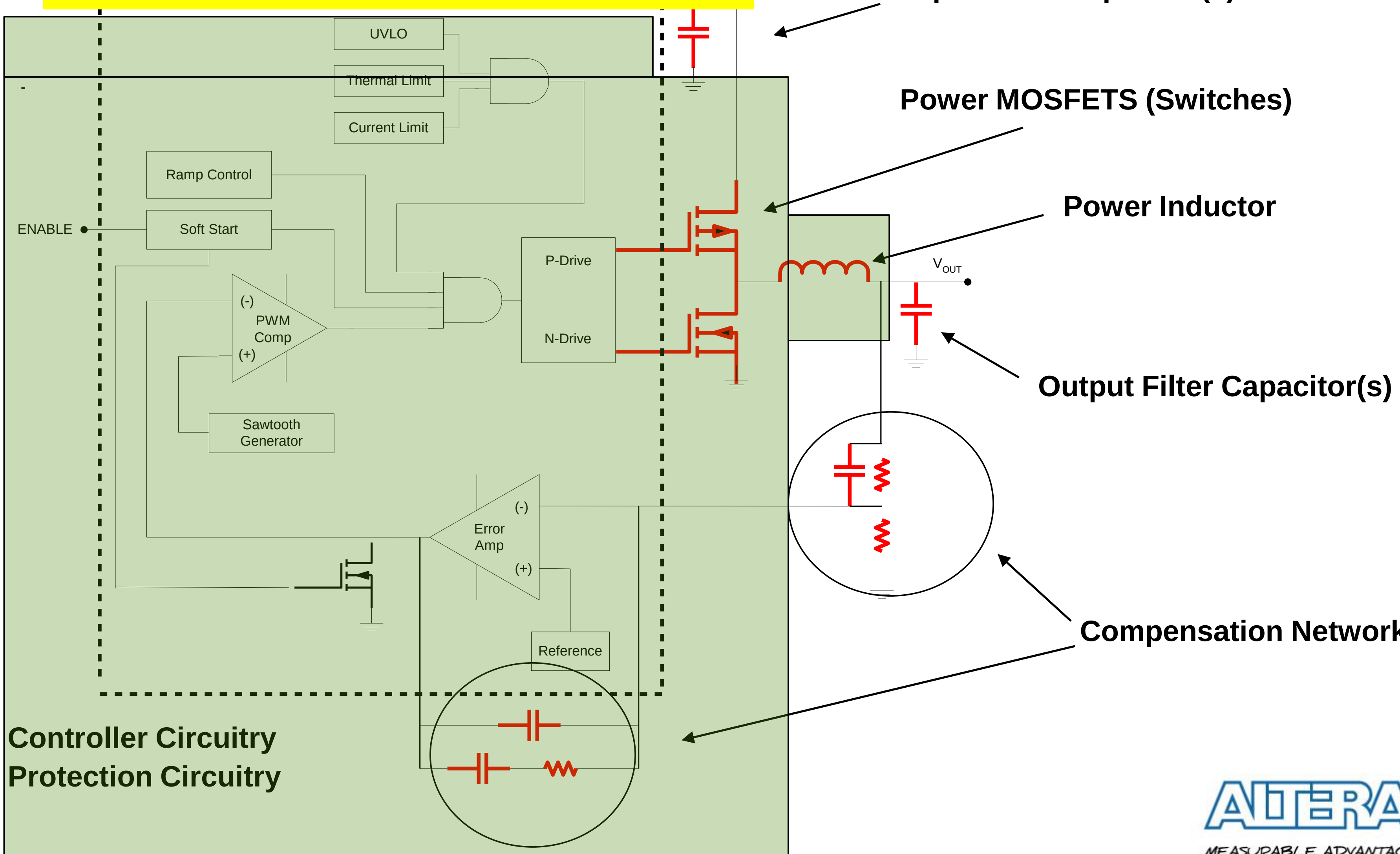
Output Filter Capacitor(s)

Compensation Network

Controller Circuitry
Protection Circuitry

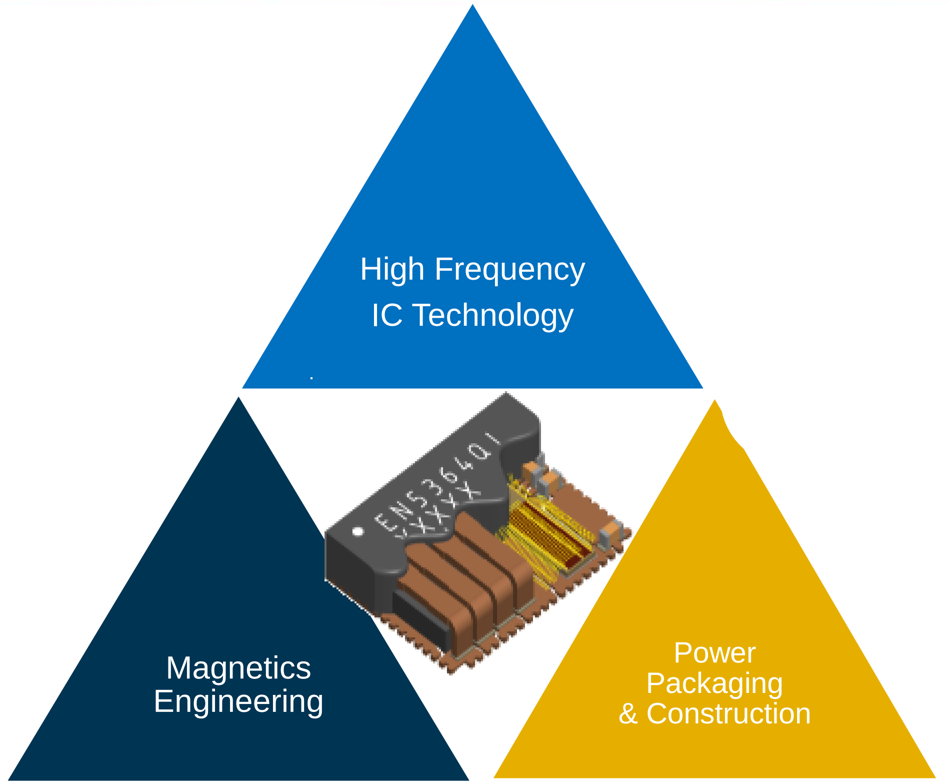
Key Components of a Switch-Mode DC-DC Converter

How do you Make it Smaller?



Key Enablers of High Density PowerSoC

3 Focused Technology Developments



DC-DC System Engineering

- Inductor Selection
- Capacitor Selection
- Power Stage Analysis
- Controller & Compensation Design
- Stability
- Time Domain Simulation
- Validation
- Production Testing

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Enpirion Power Solutions Roadmaps and Feature Sets Intersect with FPGA Power Rail Needs

Enpirion Power Products Must Have…	
CORE Supply Group	• Tight static accuracy • Dynamic load with large load steps • High efficiency and excellent thermal performance • Digital communications and control for SmartVID and system power management • Parallel capability to scale across wide range of high power/current needs
TXVR Supply Group	• Tight static and AC accuracy • Low ripple and low noise • Precise switching frequency control • Compatibility with isolation devices (beads, LDOs) • High efficiency and excellent thermal performance
IO/AUX Supply Group	• Smallest, lowest cost solution size, including integration and multiple outputs • Low profile / backside placement • Ease of use/design • Low quiescent current

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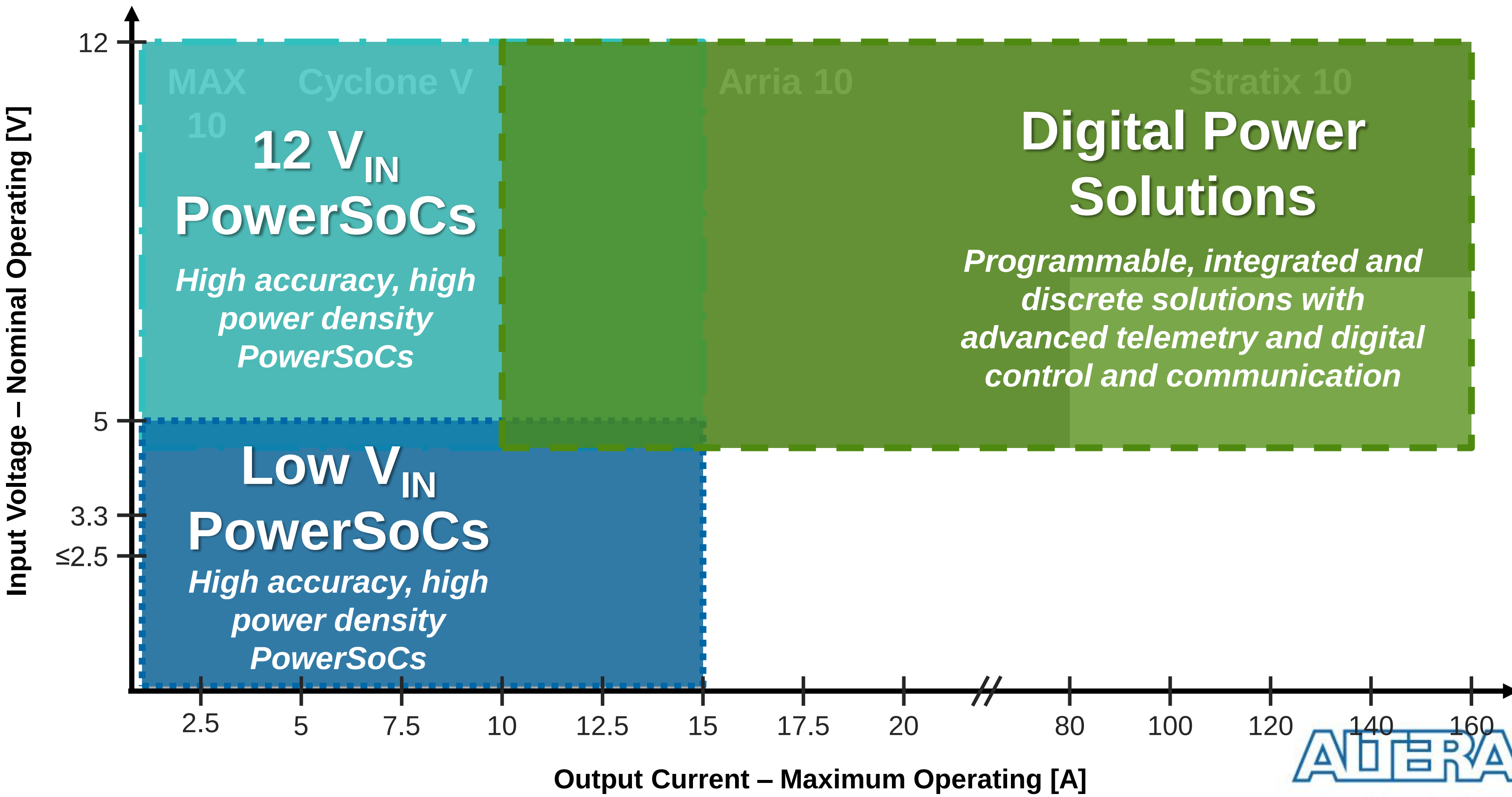
Investing in Making FPGA and SoC Systems Better – Three Strategic Focus Areas

Enpirion Power Solutions will cover the needs of FPGAs and SoCs – from low power MAX designs to full featured, high power Stratix designs



5V Road Map Time Line:

Single Output | Multi-Output | In Definition (not approved)

EN63xx

- EN6310: 1A
- EN6337: 3A
- EN6347: 4A
- EN6360: 8A
- EN63A0: 12A
- Efficiency-Optimized
- Parallel high current product options
- AEC-Q100 product options

EP53xx/EN53xx

- EP5348: 0.4A
- EP5358x: 0.6A
- EP53A8x: 1A
- EN5319: 1.5A
- EN5329: 2A
- EN5339: 3A
- EN5367: 6A
- Optimized for small Solution size
- Parallel high current product options
- AEC-Q100 product options

EN6362QI
6A, 8x8mm

EZ6301QI
1.5A switcher
2 x 300mA LDO
4x7mm

EN6311QI
1A, 4x5mm

EN63F0QI
15A

EN63A1QI
10A

EN6340QI
4A

EN6330QI
3A

EN6320QI
2A

EP6360QI
0.6A

Today | 2015 | 2016

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12V PowerSoC Road Map Time Line:

In Design | In Discovery | In Definition

EN24xx for HSSI will have tight accuracy (+/- 1%), and remote sense

EN25xx for Core will have 1% accuracy, differential remote sense, and will support a limited set of PMBus instructions to provide telemetry (VOUT, IOUT, DIE_TEMP) and some control functions (on/off, Margin+/-, trim+/-, VOUT_SET)

ERxx Regulators

- ER3105 0.5A
- ER3110 1.0A
- ER2125 2.0A
- ER3125 2.5A

IBA Products

- EC2630QI 4.5A IBC
- EC7100 Single ϕ Controller + Drvr
- ED8101 Single ϕ PWM Controller
- ED8106 Single ϕ PWM Controller
-

EN25K0QI
20A for Core

EN25F0QI
15A for Core

EN24A0QI
10A for HSSI

EN2440QI
4A for HSSI

EN2810QI
1.0A for IO

Today | 2015 | 2016

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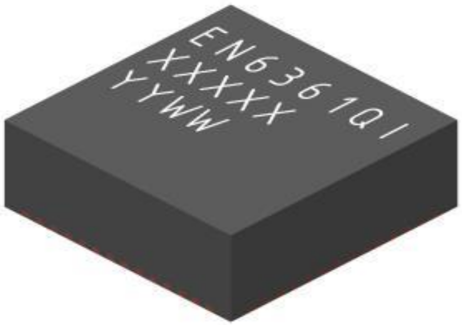
EN6362 , 5Vin/6A Power SOC

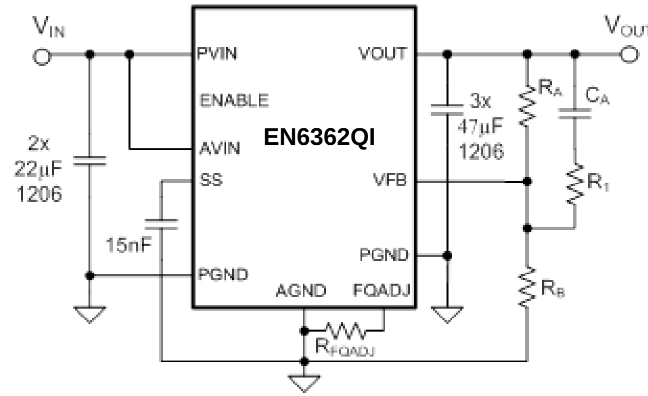


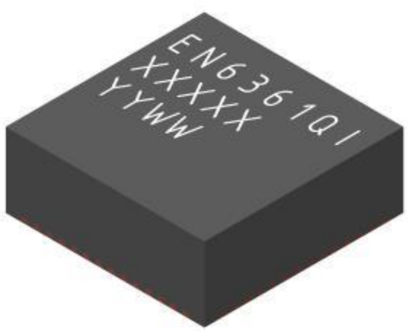
8 mm x 8 mm x 3 mm

EN6362QI 6A High Efficiency PowerSoC

Specifications:

- Synchronous Buck Converter
- Input Voltage Range: 2.5V – 6.5V
- VOUT Range: 0.6V – (V_{IN} – $V_{DROPOUT}$)
- ±1% VFB accuracy over Line/Temp
- 6A Continuous Output Current
- 8mm x 8mm x 3mm QFN
- Solution Footprint: 170mm^2





8mm x 8mm x 3mm

170mm^2

Features:

- High conversion efficiency
- No load current de-rating at 85°C
- Excellent ripple and EMI performance
- Best in class transient response
- Programmable Soft Start
- Enable and POK for sequencing
- OCP, SCP, OTP, UVP
- Monotonic Startup into a Pre-biased load

Nine AEC-Q100 Qualified Enpirion PowerSoC Products for Automotive Applications

Products	I_{OUT} (A)	V_{IN} Range (V)	V_{OUT} Range (V)	Package	Approx. Total Solution Size (mm^2)	Enable	OCP	OTP	UVLO	VID	External V_{OUT} Set	Power Good (POK)	Programmable Soft-Start	Frequency Synchronization	Parallel Operation
EP53xx 5V PowerSoCs															
EP5358LUA	0.6	2.4 - 5.5	0.60 - (V_{IN} - $V_{DROPOUT}$)	uQFN16	14	■	■	■	■	■	■				
EP5358HUA	0.6	2.4 - 5.5	1.8 - 3.3	uQFN16	14	■	■	■	■	■					
EP53A8LQA	1.0	2.4 - 5.5	0.60 - (V_{IN} - $V_{DROPOUT}$)	QFN16	21	■	■	■	■	■	■				
EP53A8HQA	1.0	2.4 - 5.5	1.8 - 3.3	QFN16	21	■	■	■	■	■					
EP53xx 5V PowerSoCs															
EN6310QA	1.0	2.7 - 5.5	0.6 - 3.3	QFN30	65	■	■	■	■		■	■	■		
EN6337QA	3.0	2.5 - 6.6	0.75 - (V_{IN} - $V_{DROPOUT}$)	QFN38	75	■	■	■	■		■	■	■	■	
EN6347QA	4.0	2.5 - 6.6	0.75 - (V_{IN} - $V_{DROPOUT}$)	QFN38	75	■	■	■	■		■	■	■	■	
EN6360QA	8.0	2.5 - 6.6	0.60 - (V_{IN} - $V_{DROPOUT}$)	QFN60	190	■	■	■	■		■	■	■	■	■
EN63A0QA	12.0	2.5 - 6.6	0.60 - (V_{IN} - $V_{DROPOUT}$)	QFN76	227	■	■	■	■		■	■	■	■	■

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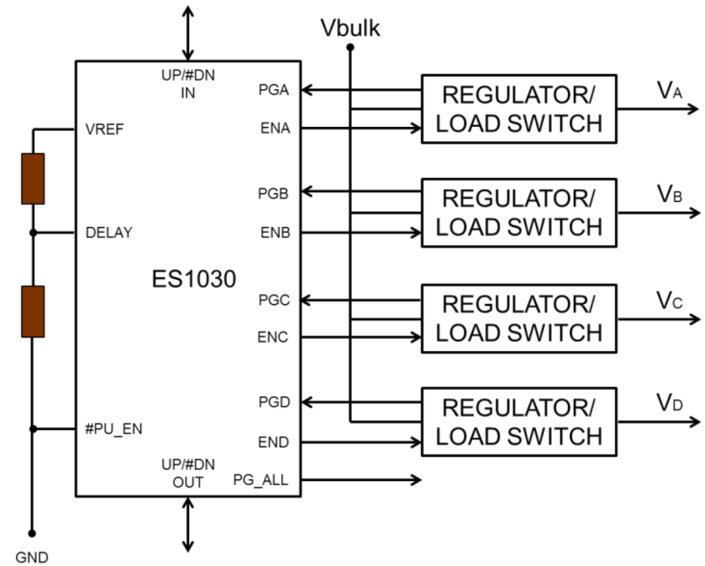
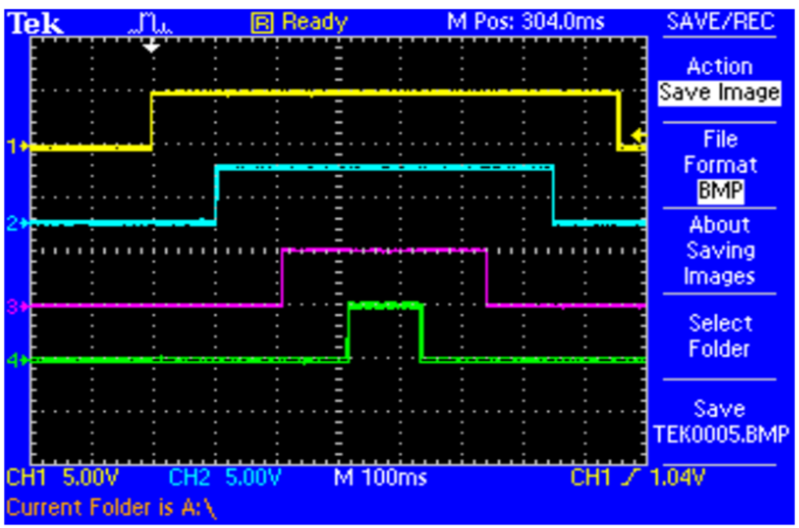
ES1030 Adjustable Quad Sequencer



Specifications

- 4-Channel
- Operates from 1.8 to 5.5V supply voltage
- Logic level outputs
- I/O options: ENABLE and Power Good
- Operating Temp Range: -40ºC to 85ºC\
- 10% delay accuracy



3mm x 2mm x 0.55mm QFN

Features

- Sequence ENABLES in ABCD up DCBA down order
  - Programmable
  - Accurate
- Adjustable delay
- Easily daisy chained to support more than four sequenced signals
- Fault reverses sequence

ES1030 General Description

Item	Specification
Device	ES1030 4ch Nested Sequencer w/ Digital Fault Handling
VIN Range	1.8V – 5.5V
Output Channels	4ch, chainable
Return Channels	4ch digital PG signals
Logic Levels	1.8V-5V nominal
Delay Range	32us-8.4ms
Delay Programming	Resistor divider from internal reference
Delay Accuracy	10% over load and temp
Ambient Temp Range	-40°C to +85°C
Package Size	ES1030: 2.0mm x 3.0mm x 0.55mm, 0.4mm pitch STQFN-20
Features:	Push-pull outputs, chaining inputs and outputs, fault aborts sequence up and triggers sequence down, aggregate PG signal

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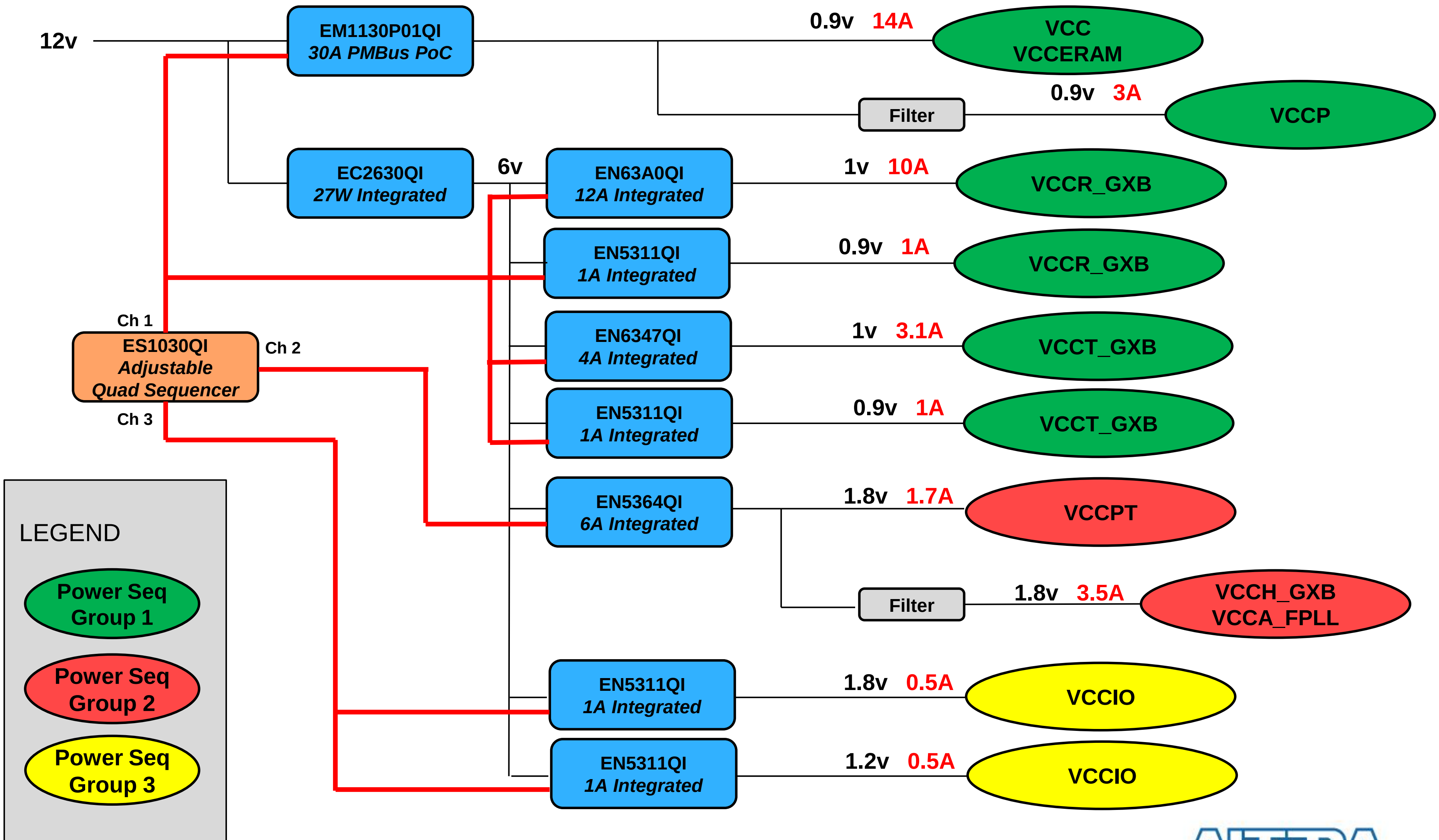
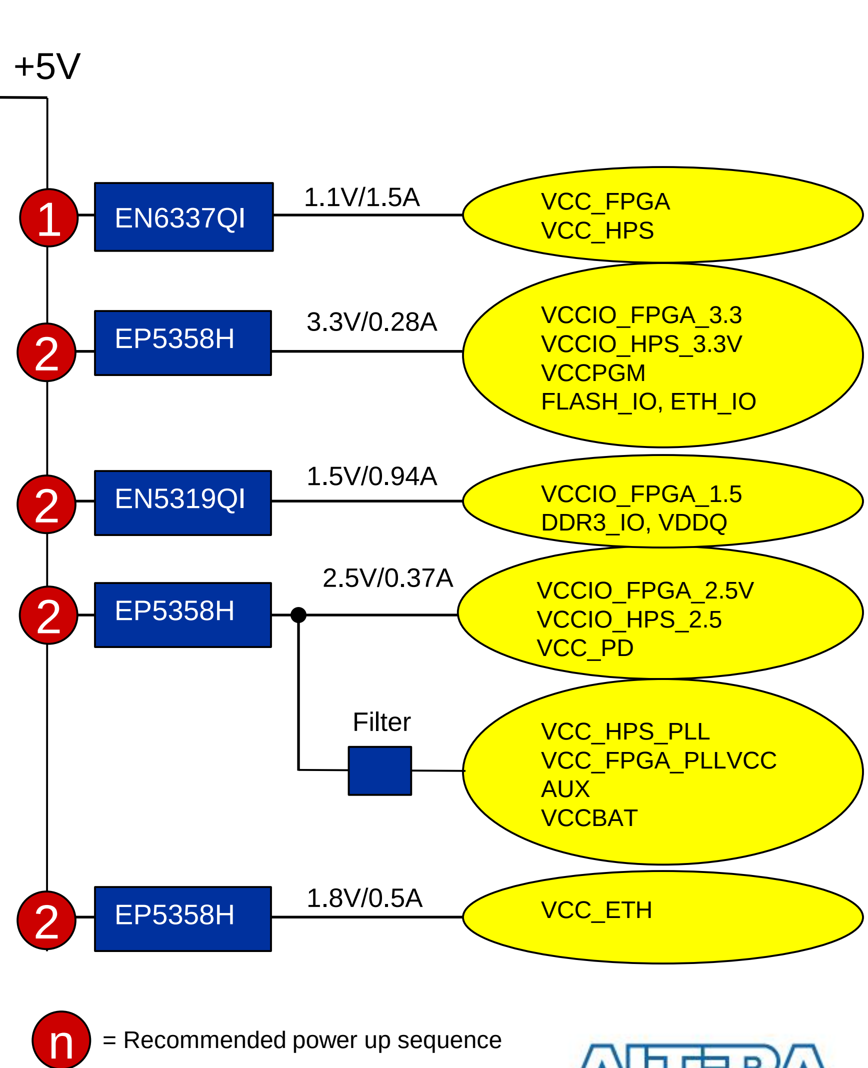
Power Tree Examples

Aria 10 Power Tree



Low Power Cyclone V SoC IBA Example

Power Rail	Vout(V)	Iout(A)	Vin(V)	Regulator	Solution Size (mm2)
12V BUS					
IBA +5V	**5.00**	**1.355**	**12.0**	**ER2120**	**200**
Rails powered by IBA					
VCC_FPGA VCC_HPS	1.10	1.50	5.0	EN6337QI	75
VCCIO_FPGA_3.3 VCCIO_HPS_3.3V VCCPGM FLASH_IO Eth_IO	3.30	0.28	5.0	EP5358HUI	14
VCCIO_FPGA_1.5 DDR3_IO	1.50	0.94	5.0	EN5319QI	55
VCCIO_FPGA_2.5V VCCIO_HPS_2.5 VCC_PD (Filtered) VCC_HPS_PLL VCC_FPGA_PLL VCCAUX VCCBAT	2.50	0.37	5.0	EP5358HUI	14
DDR3 VTT	0.75	0.20	1.5	EV1320QI	40
VCC_ETH	1.80	0.50	5.0	EP5358HUI	14
Solution Footprint (mm2)					**412**



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Thank You

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