Transceiver Toolkit for Arria 10 Devices

Training Agenda & Objectives

- Transceiver Toolkit overview
  - What is the Transceiver Toolkit and how is it useful to FPGA designers? Sub-bullet
- Enabling Transceiver Toolkit support
  - Configure your Arria® 10 design to enable Transceiver Toolkit support
- Using the Transceiver Toolkit
  - Setup and launch the Transceiver Toolkit to perform a high speed link test
  - Perform Bit Error Rate (BER) testing using the Auto Sweep feature
  - Select the PMA settings for your transceivers which gives best signal integrity on your board

Transceiver Toolkit for Arria 10 Devices

Transceiver Toolkit Overview

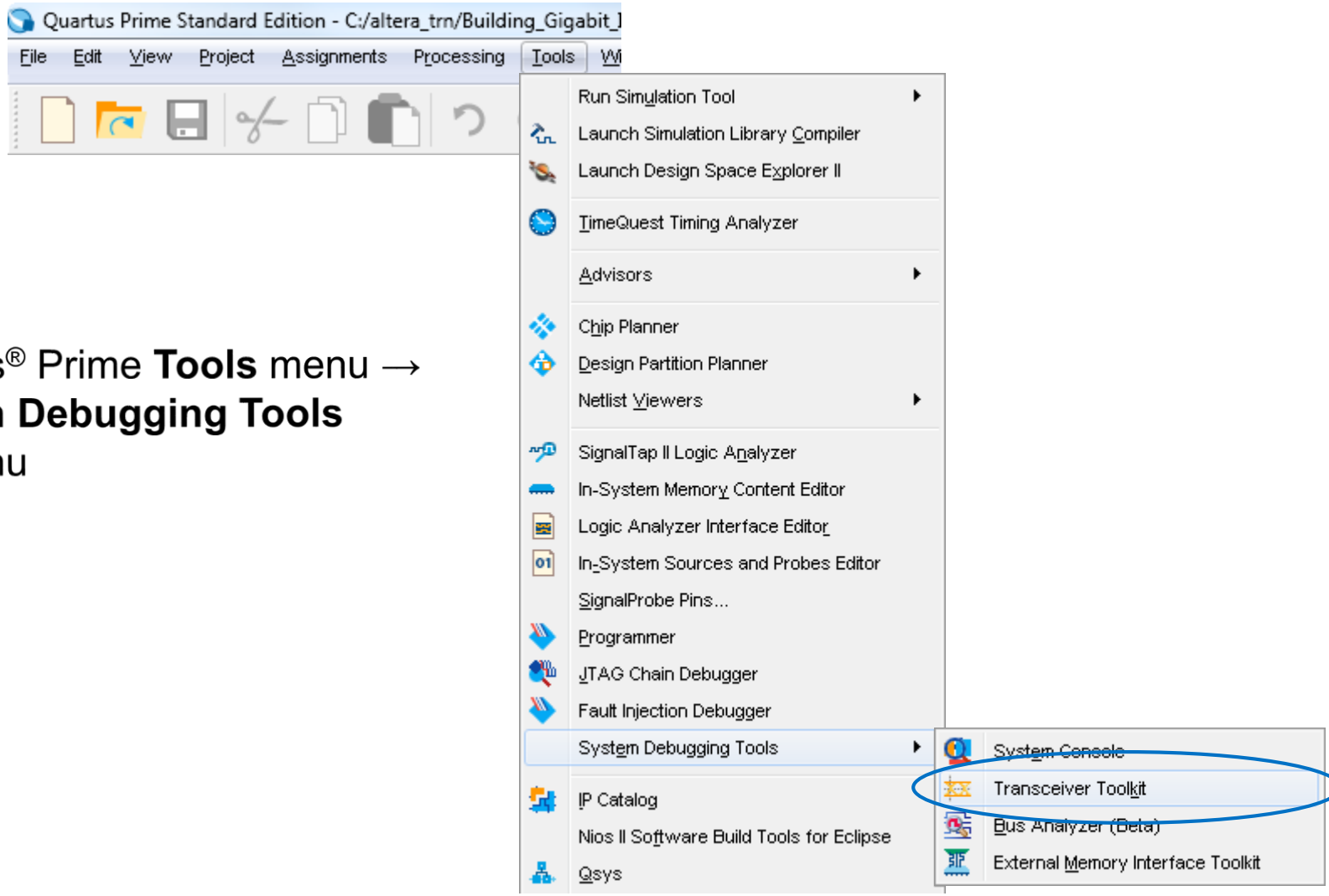
Quartus Prime Transceiver Toolkit

*The **Transceiver Toolkit** is a powerful analog verification tool that…*

- Quickly analyzes the transceiver signal quality and performance
- Generates and checks psuedo-random binary sequence (PRBS) patterns to measure the BER
- Dynamically changes I/O buffer settings under automatic or manual control
- Supports a variety of design situations
- Comes free with any licensed version of the Quartus Prime software

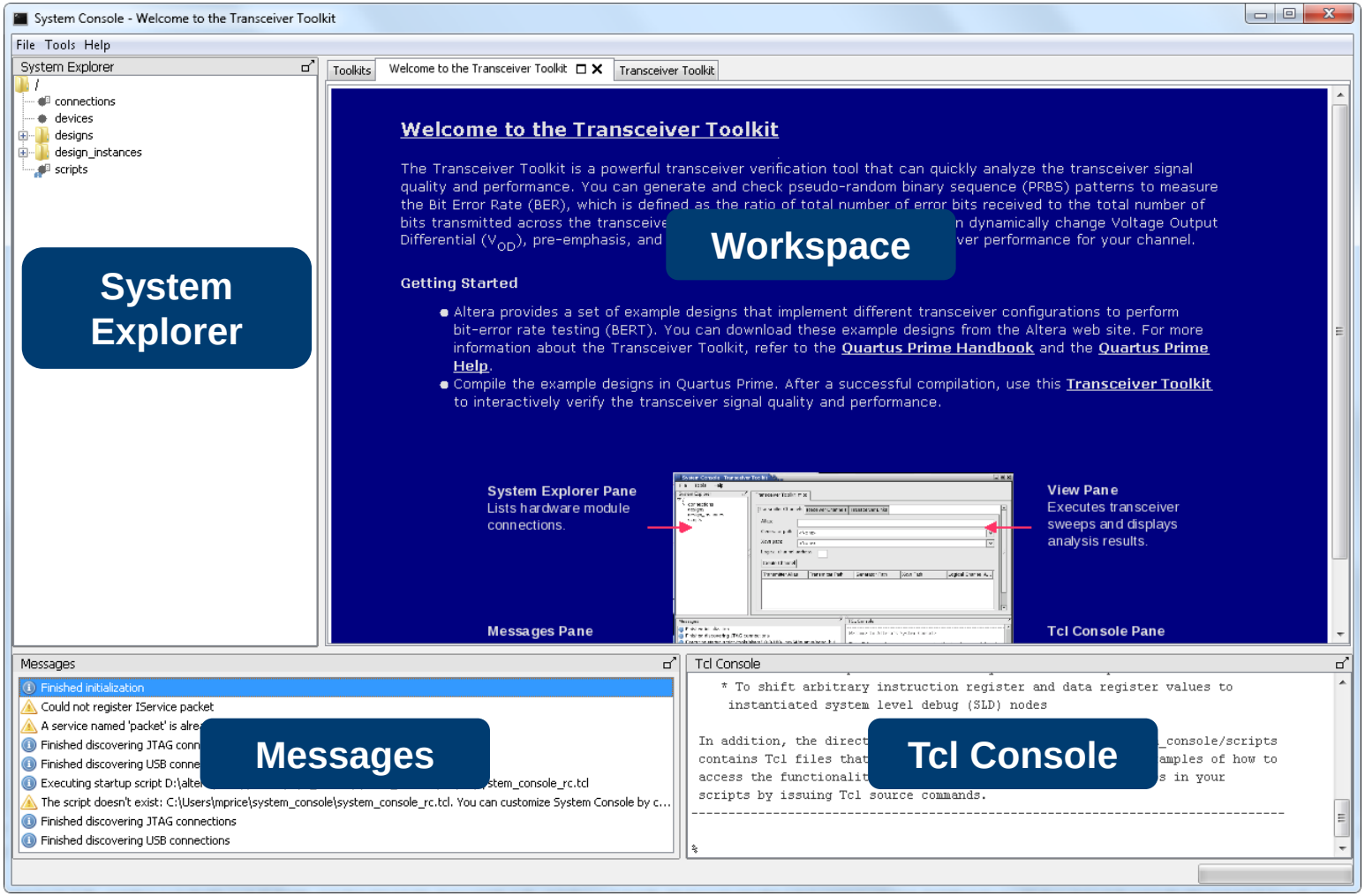
Opening the Transceiver Toolkit

- Quartus® Prime **Tools** menu → **System Debugging Tools** submenu



Transceiver Toolkit GUI

Built into the System Console



**** For more details on using the System Console, see the online training entitled System Console***

Features

- Easy to use UI for changing RX and TX PMA options to fine tune signal integrity
  - V_{OD} (TX)
  - Pre-emphasis (TX)
  - Equalization (RX)
  - Equalization DC gain (RX)
- Management of multiple BER tests and run them in parallel
  - Test single or multiple channels
  - Test single or multiple FPGAs
- Generation and checking of PRBS7, PRBS15, PRBS23 and PRBS31 patterns
- AEQ and DFE support
- Auto Sweep support

Auto Sweep

- Sweeps PMA settings through a range of supported values set by the designer
- Chooses best value based on target BER set by designer
- Stores previous Auto Sweep runs for comparison

Transceiver Toolkit for Arria 10 Devices

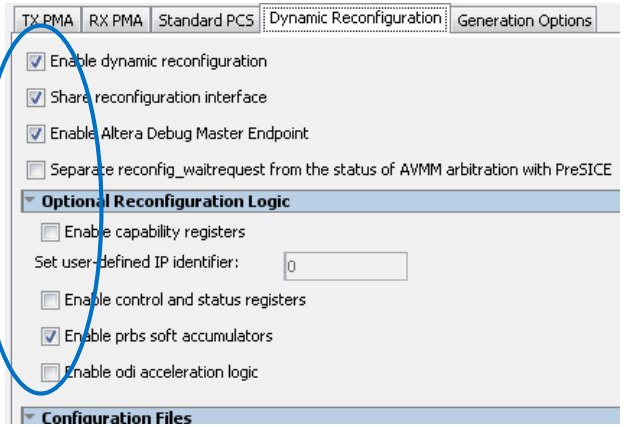
Enabling Transceiver Toolkit support

Auto Sweep

- Special JTAG interface synthesized by Quartus Prime software in FPGA logic when enabled
- Provides access to memory mapped reconfiguration register space in transceiver channels and PLLs
  - ADME logic masters the channel/PLL Avalon®-MM slave interface
  - Functions in parallel to any existing reconfiguration control logic
- Allows System Console to automatically detect and control transceiver channels directly
  - Qsys system not required
  - JTAG to Avalon Master Bridge connection not required

Enabling Transceiver Toolkit Support (1)

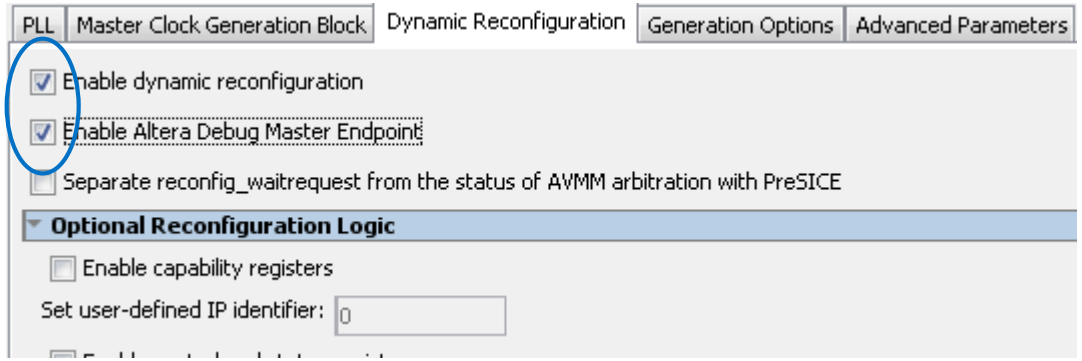
- Must enable support on Native PHY and Transceiver PLL IP cores
- In Native PHY IP parameter editor, select



  - Enable dynamic reconfiguration
  - Share reconfiguration interface
    - If more than one channel in PHY instance
  - Enable ADME
  - Enable PRBS soft accumulators
    - Turns on transceiver channel's hard PRBS generator and checker

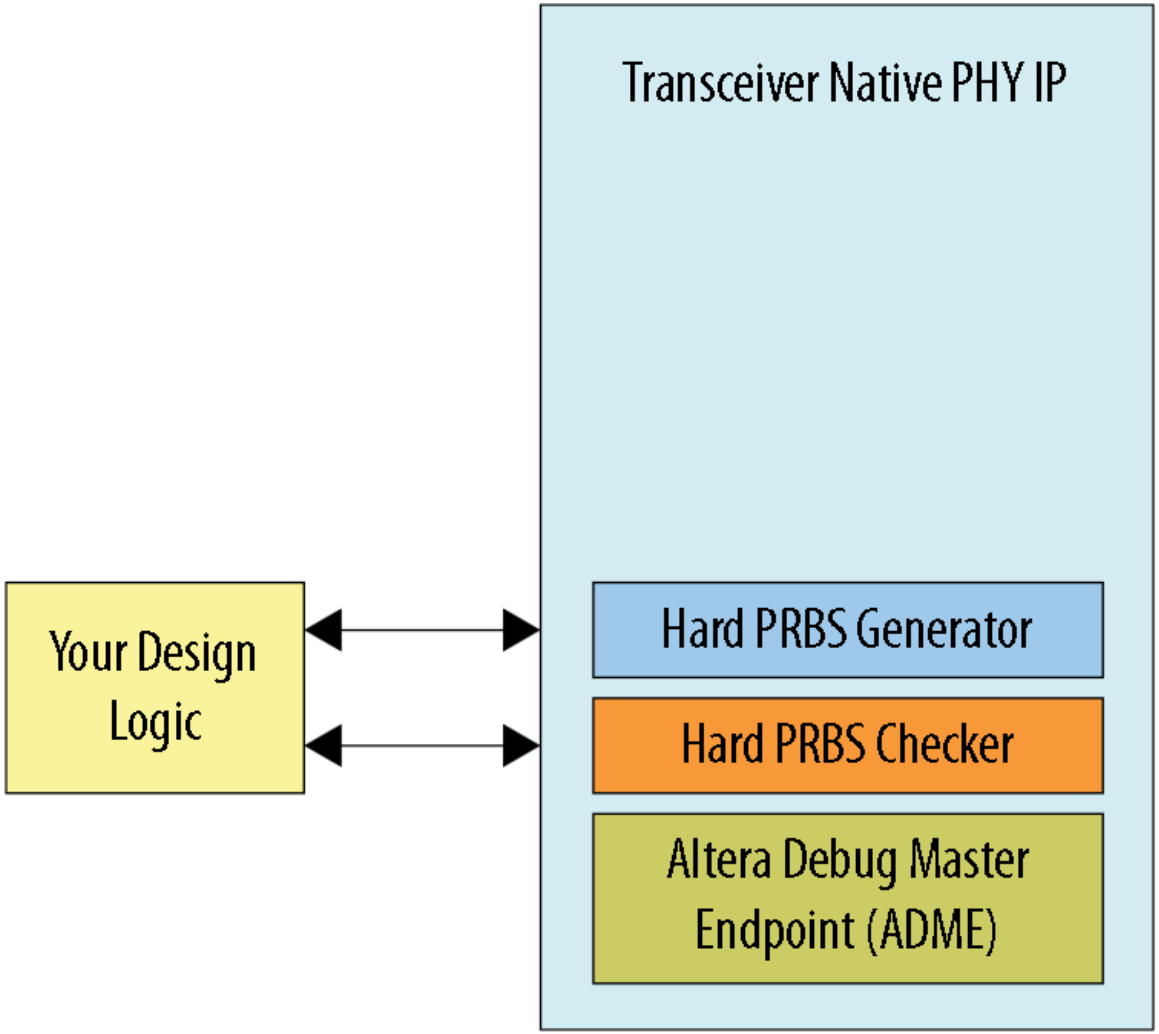
Enabling Transceiver Toolkit Support (2)

- In Transceiver PLL IP parameter editor, select



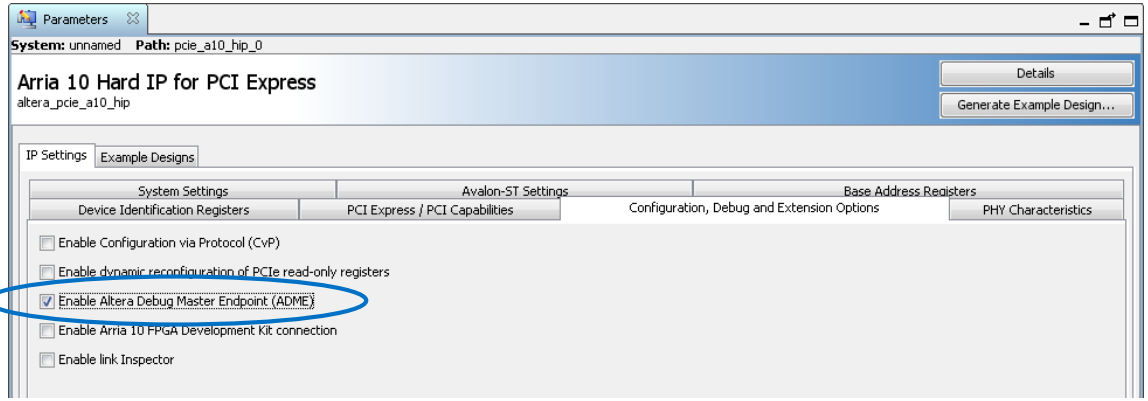
  - Enable dynamic reconfiguration
  - Enable ADME

Design Example Block Diagram

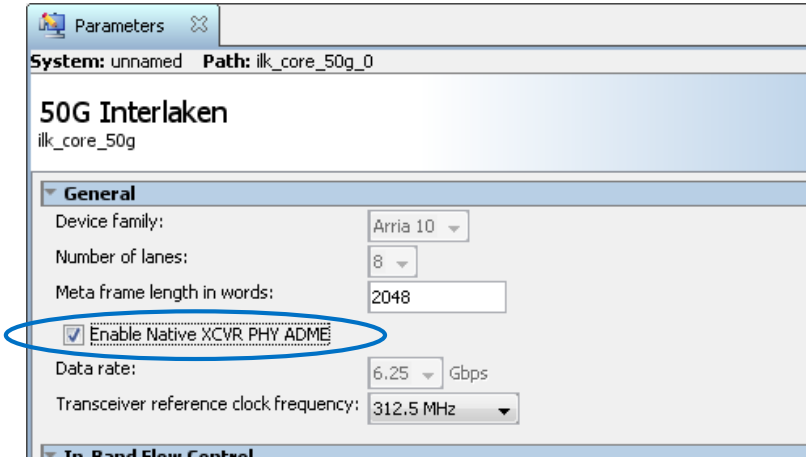


What about Other Intel IP Cores?

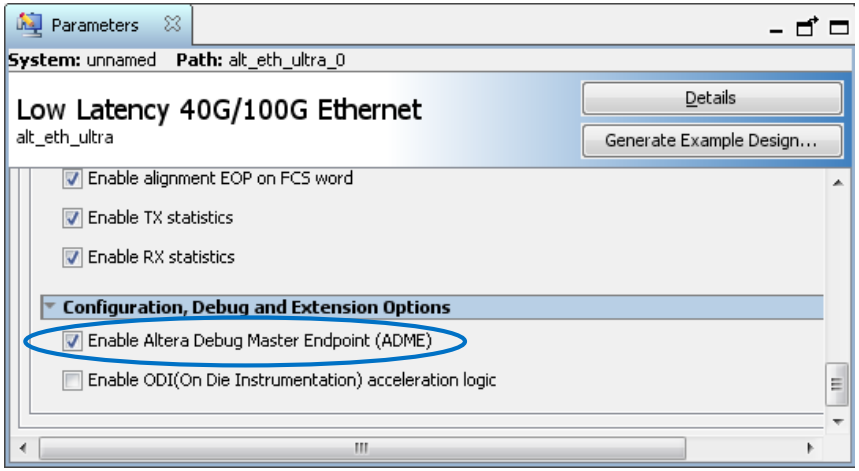
- Protocol-specific IP must have option to enable ADME



Hard IP for PCI Express Parameter Editor



50G Interlaken Parameter Editor

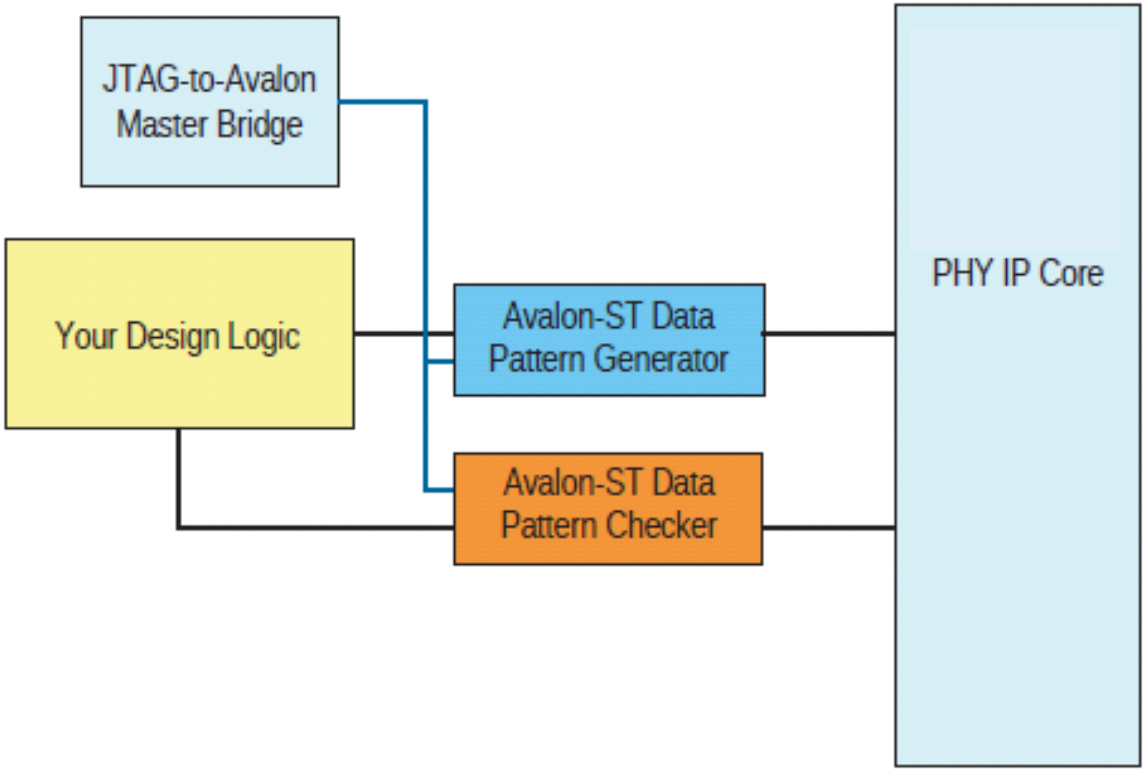


40G/100G Ethernet Parameter Editor

ADME Alternative: Pattern Generator/Checker IP Cores

- Connect Data Pattern Generator/Checker IP cores found in Quartus Prime IP Catalog and Qsys IP Catalog
  - Disable the PRBS soft accumulators
  - Hard PRBS blocks replaced with soft PRBS blocks in FPGA fabric
  - Similar to 28-nm Transceiver Toolkit flow
- Advantages
  - Support for BER error injection
  - Support for PRBS7, PRBS15, PRBS 23 and PRBS 31 in data widths of 32 to 128 bits
  - Support bypass mode to allow custom traffic to pass
- Disadvantage
  - Requires instantiating and connecting JTAG to Avalon Master Bridge component for control

ADME Alternative Block Diagram



Intel Wiki Demonstration Designs

- Fully functional design examples
  - http://www.alterawiki.com/wiki/High_Speed_Transceiver_Demo_Designs_For_Current_and_Older_Families#Transceiver_Toolkit_Designs
- Target Arria 10 development kits
  - Arria 10 GX FPGA Development Kit (https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-a10-gx-fpga.html)
  - Arria 10 GX Transceiver Signal Integrity Development Kit (https://www.altera.com/products/boards_and_kits/dev-kits/altera/kit-a10-gx-si.html)

Transceiver Toolkit Designs

- **UPDATED (16/12/2015) Arria10 GX SI Board (ES3): 24 Channel Transceiver Toolkit design at 12.5 & 10.3125 Gbps (QSFP+) using 3 Native PHY's (includes tcl file with multiple useful procedures)**
  http://www.alterawiki.com/wiki/File:Arria10_SIBoard_24Ch_TTK_ES3.zip (15.1.1 B189)
- **UPDATED (12/11/2015) Arria10 GX PCIe Development Kit (ES2) : 12 Channel Transceiver Toolkit design at 12.5 Gbps with rev. parallel loopback routed to FMC connector A (non-bonded) (includes tcl file listed on top of the page)**
  http://www.alterawiki.com/wiki/File:Arria10_Devkit_12Ch_TTK_with_reverse_parallel_loopback.zip (15.1 B185)
- **(08/05/2015) Arria10 GX SI Board: 20 Channel Transceiver Toolkit design at 10.3125 Gbps using 2 Native PHY's (includes tcl file with multiple useful procedures)**
  http://www.alterawiki.com/wiki/File:Arria10_SIBoard_20Ch_2_Phy_TTK.zip (15.0.1 B147)
- **(26/11/2014) Arria10 GX PCIe Development Kit: 12 Channel Transceiver Toolkit design at 10.3125 Gbps with optional Nios Control (non-bonded)**
  http://www.alterawiki.com/wiki/File:Arria10_Devkit_12Ch_TTK_with_Nios.zip (14.0A10s B578 0.03)

Transceiver Toolkit for Arria 10 Devices

Using the Transceiver Toolkit

Example User Flow

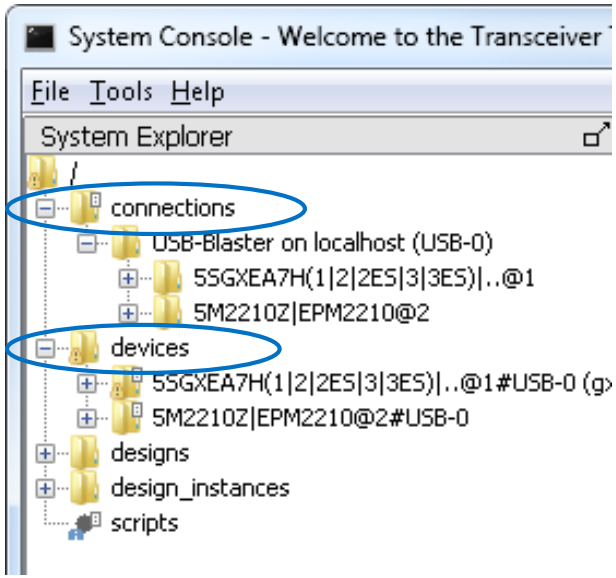
1. Set up board(s)
2. Open Transceiver Toolkit (Quartus Prime Tools menu) and check connections
3. Load design
4. Link hardware resources
5. Identify channels
6. Run tests
   - Run Auto Sweep
     - Select optimum range of PMA settings

1) Setting Up PC Board(s)

- Make sure the physical connections are made for the channel(s) you want to test
  - Loopback on the board (single device/channel)
  - Physical channel/link between devices (multiple devices)
  - Serial Loopback (in the Toolkit)

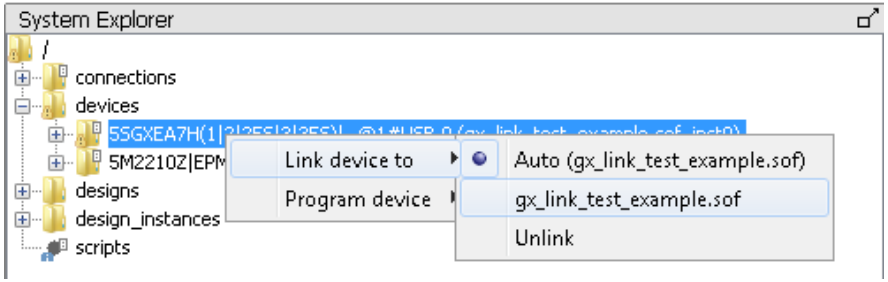
3) Load Design

- Verify device and JTAG connection appears in Device and Connections
  - If not, check cable connections/drivers
- Load your transceiver design project(s) with the
  - File menu → Load Project..
  - Project will auto-load if Transceiver Toolkit is started from Quartus Prime software with project open and compiled
  - Load multiple projects if testing multiple devices/boards

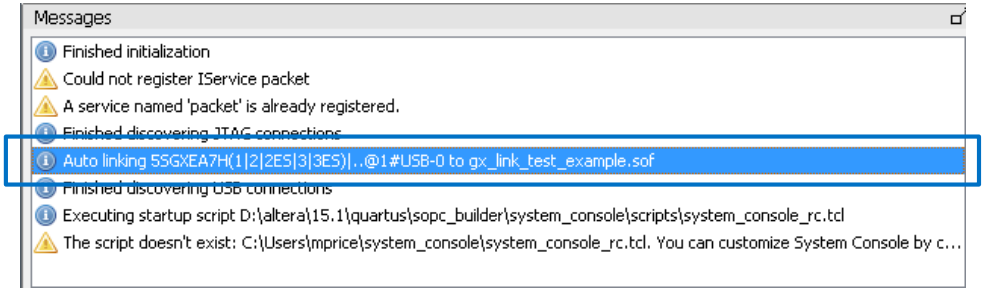


4) Link Hardware Resources

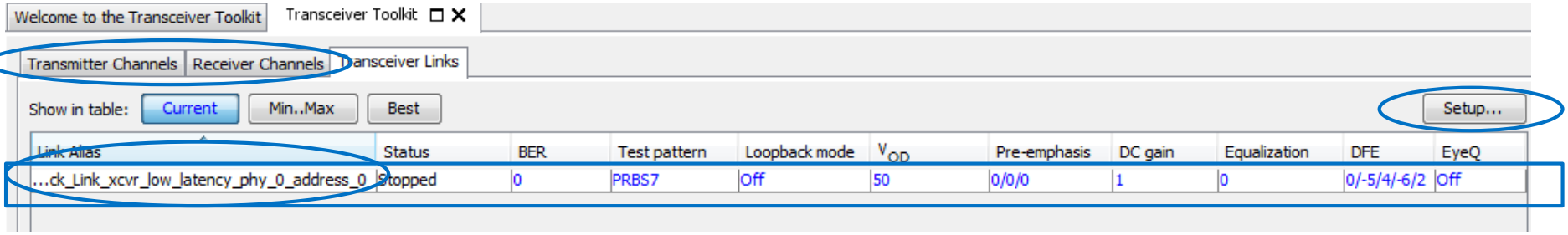
- Identifies the hardware resources connected
  - Assigns Quartus Prime project information to hardware



- Auto-linking performed when project loaded and device programmed with project

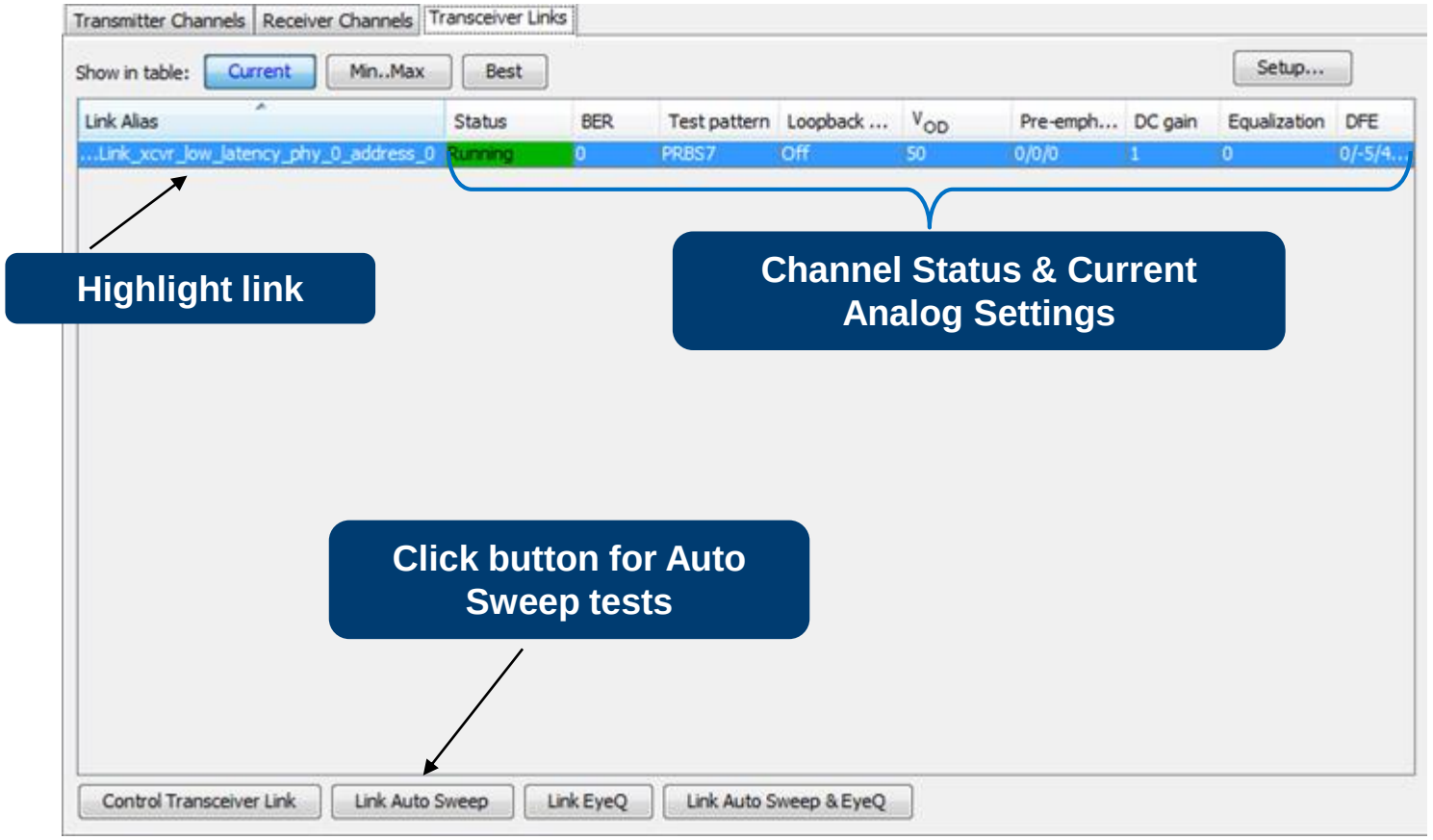


5) Identify Channels

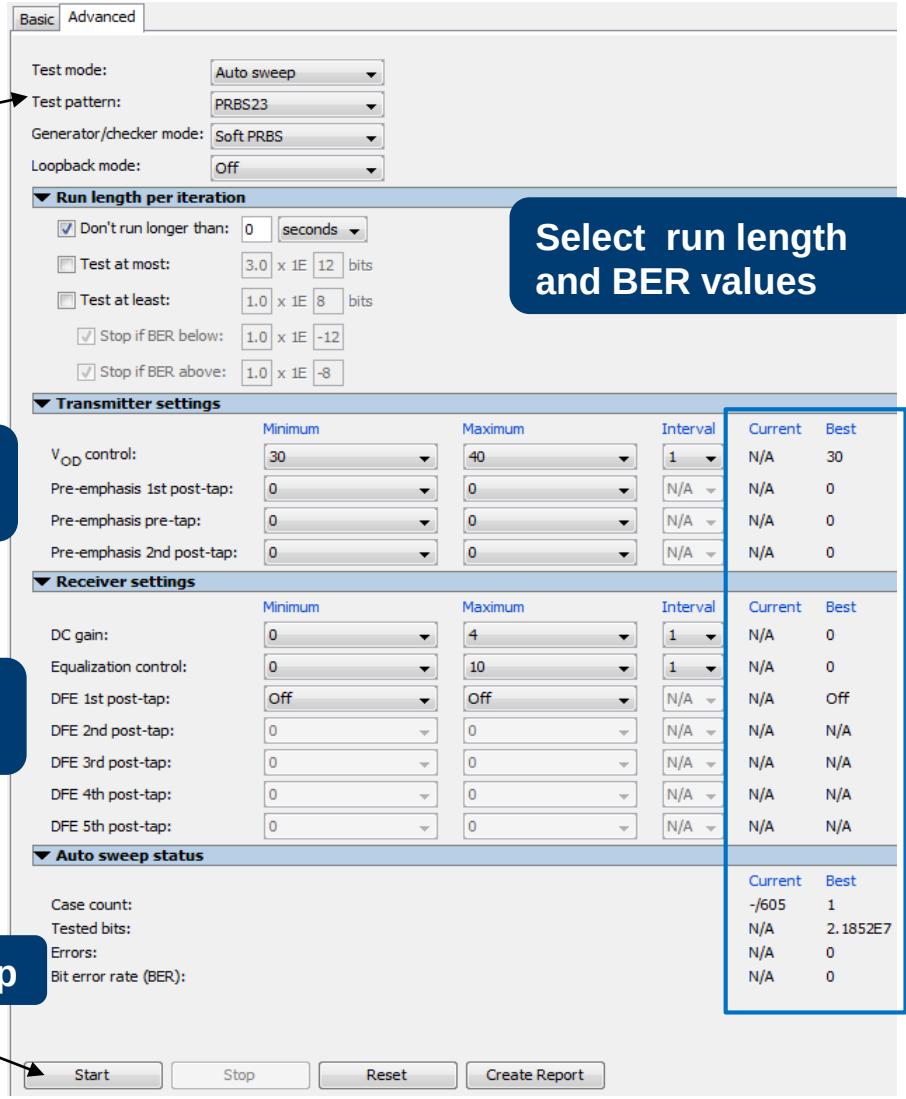


- Design RX and TX channels will automatically display in Transmitter Channels and Receiver Channels tabs
- Create link to indicate the TX→RX channel connections
  - Auto-links created between RX/TX paths in same channels
  - Create new links to connect TX and RX on different transceiver channels or different devices
  - Change link alias to create a more “user-friendly” link name

6) Run Tests


Transmitter Channels
Receiver Channels
Transceiver Links
Show in table:
Current
Min..Max
Best
Setup...
Link Alias
Status
BER
Test pattern
Loopback ...
V_{OD}
Pre-emph...
DC gain
Equalization
DFE
...Link_xcvr_low_latency_phy_0_address_0
Running
0
PRBS7
Off
50
0/0/0
1
0
0/-5/4...
Highlight link
Channel Status & Current Analog Settings
Click button for Auto Sweep tests
Control Transceiver Link
Link Auto Sweep
Link EyeQ
Link Auto Sweep & EyeQ

Running Auto Sweep



Choose PRBS pattern

Select run length and BER values

Choose TX PMA ranges and intervals to sweep

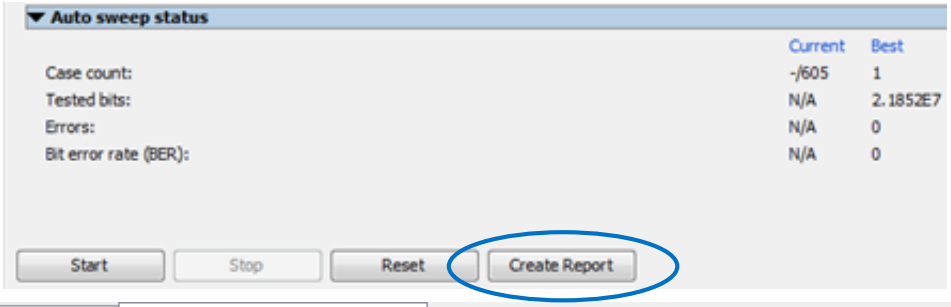
Sweep Results (Current and Best Value)

Choose RX PMA ranges and intervals to sweep

Right-click to populate fields with best value from sweep or values read back from the FPGA

Click Start to run Auto Sweep

BER Reports



Welcome to the Transceiver Toolkit | Transceiver Toolkit | Transceiver Link: Loopback_Link_xcvr_low_latency_phy_0_address_0 | Report: 2014-09-12 12:25:19

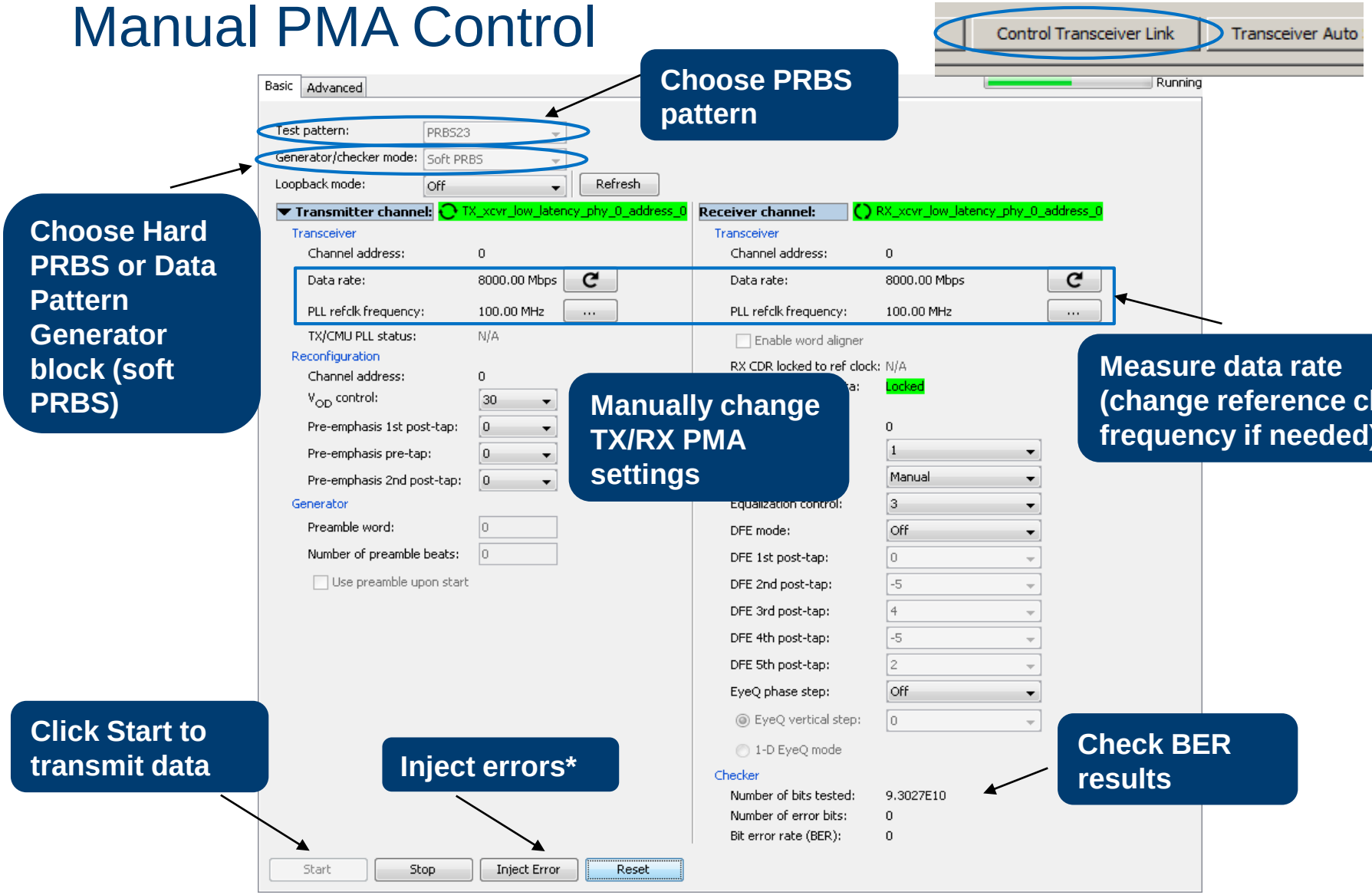
Report: 2014-09-12 12:25:19

<<Search>>

	Timestamp	Data Pattern	VOD Control	Pre-empha...	Pre-empha...	Pre-empha...	Pre-empha...	DC Gain	Equalizatio...	Equalizatio...	DFE 1st Tap	DFE 2nd Tap	DFE 3rd Tap	DFE 4th Tap	DFE 5th Tap	Df
1	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
2	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
3	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
4	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
5	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
6	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
7	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
8	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
9	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
10	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
11	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
12	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0
13	2014-09-12 ...	PRBS23	30	0	0	0	N/A	0	Manual	3	0	3	0	0	0	0

- Run Auto Sweep Report to compare BERs and # of tested bits to PMA settings
- Sort columns
- Export data (.CSV file) for further analysis

Manual PMA Control

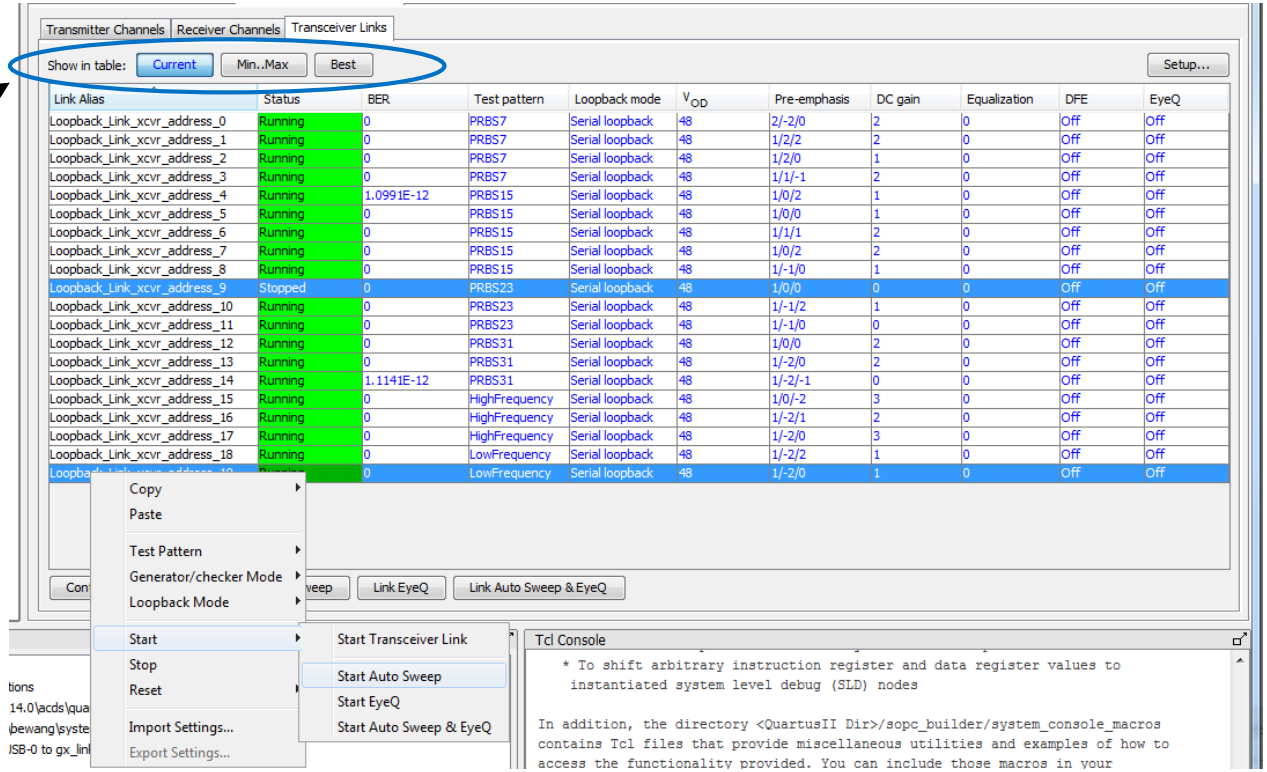


* *Supported with Data Pattern Generator blocks only*

Channel Manager (All Tabs)

- Control and view status of multiple channels simultaneously
- Copy and paste settings between channels
- Export and import settings to/from text files

Show all current values, max and min values for auto sweep or best values from last auto sweep



Example Usage Flow

- Perform a Auto-Sweep test to get best BER with various combinations of PMA settings
  - Alternative method: check the Best Case column from an Auto Sweep for the settings and enter those PMA values directly in the Transmitter and Receiver control panels
- Before employing DFE, use other PMA settings
  - If BER = 0, then leave DFE off
  - If BER > 0, then use best combination of other PMA settings and sweep DFE settings

Transceiver Toolkit for Arria 10 Devices

Summary

Course Summary

- Use the Transceiver Toolkit to perform high speed link tests in your system
- Enable Transceiver Toolkit support in your Arria 10 FPGA design
- Use Transceiver Toolkit features such as Auto Sweep to perform BER testing and choose analog settings to optimize signal integrity

More Details on Transceiver Toolkit

- Transceiver Toolkit demos
  - https://www.youtube.com/watch?v=qh4sGSB0DVc
  - https://www.youtube.com/watch?v=xWuB7RLM_aw
  - https://www.youtube.com/watch?v=PbXu2oPnYBk
- Online documentation
  - Debugging Transceiver Links, Quartus Prime Handbook, Volume 3
    - https://documentation.altera.com/#/00014470-AA$AA00055412
  - Quartus Prime 16.1 online help
    - http://quartushelp.altera.com/16.1/index.htm#program/syscon/syscon_db_load.htm

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Hands on labs
1 day long
Class schedules at
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[Instructor-led Training]

Intel Technical Support

- Reference Quartus Prime software on-line help
- Quartus Prime Handbook
- World-wide web: http://www.altera.com
  - Search for answers to problems with Knowledge Database
  - Download literature
  - View design examples
  - View online trainings
- MySupport: http://www.altera.com/mysupport
- Field applications engineers: contact your local Altera® sales office
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