USB Type-C Design Implementations – Overview & Test Solution

Seo Dong-Hyun

KEYSIGHT TECHNOLOGIES

USB Type-C Overview

KEYSIGHT TECHNOLOGIES

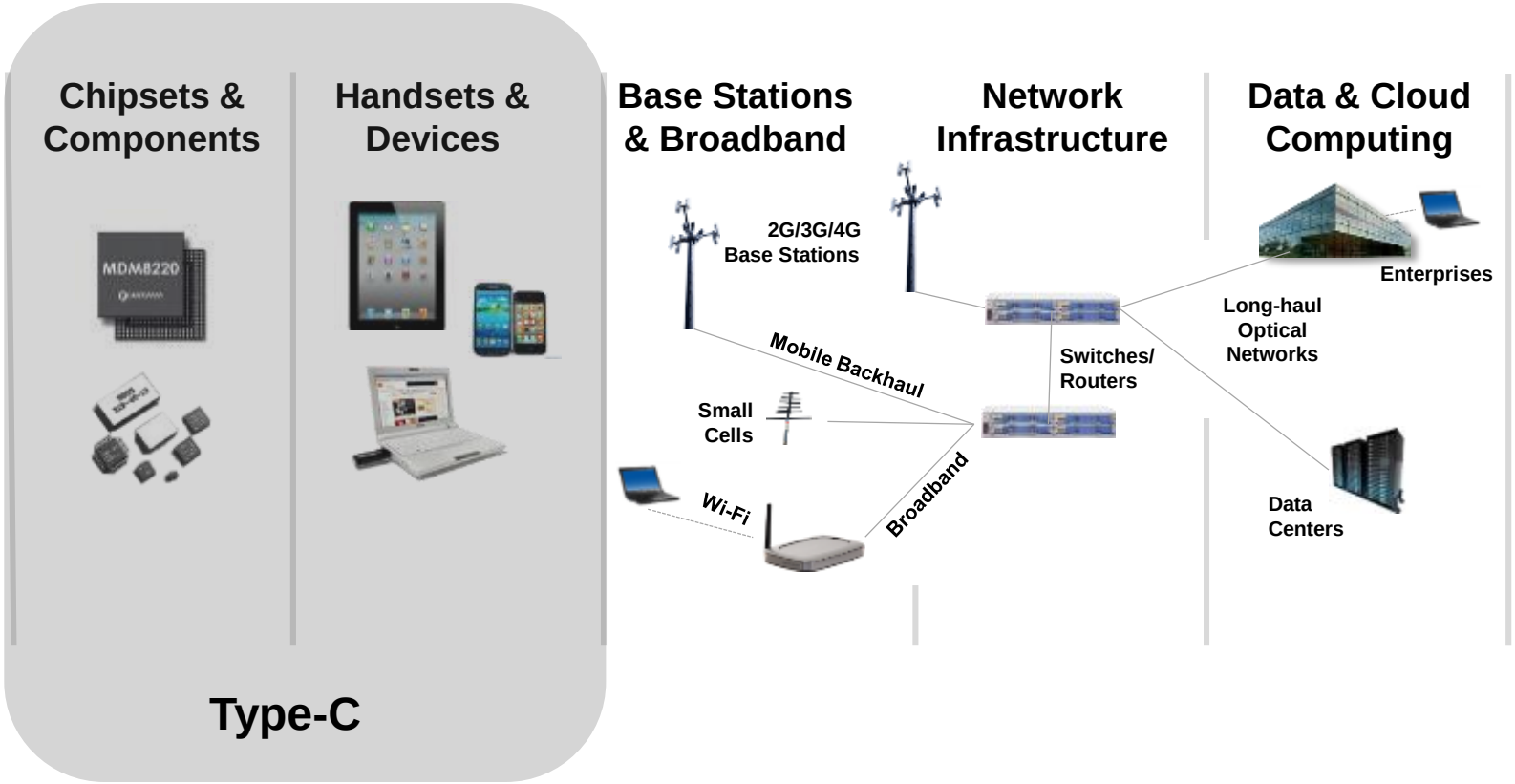
What is the USB Type-C Connector?

"One connector to rule them all"

Original USB Industry Drivers	Type-C Industry Drivers
Single connector type/Expandability	Broad application in standards
Performance/Speed	10 Gb/s with path to 40 Gb/s
Power	Can handle 5 Amps at 20Volts
Ease of Use for End-User	Reversible (can be flipped)

The Communications Ecosystem

Where does USB-C fit?



Why Does It Matter?

Simplicity and Capability to consumer….

……Complexity to Designers, Integrators, and Validators

Speed

Speeds of the Future and
Backwards Compatibility

Power

Up to 100 W

Power direction no longer fixed

Standards Integration

MHL Mobile High-Definition Link

DisplayPort

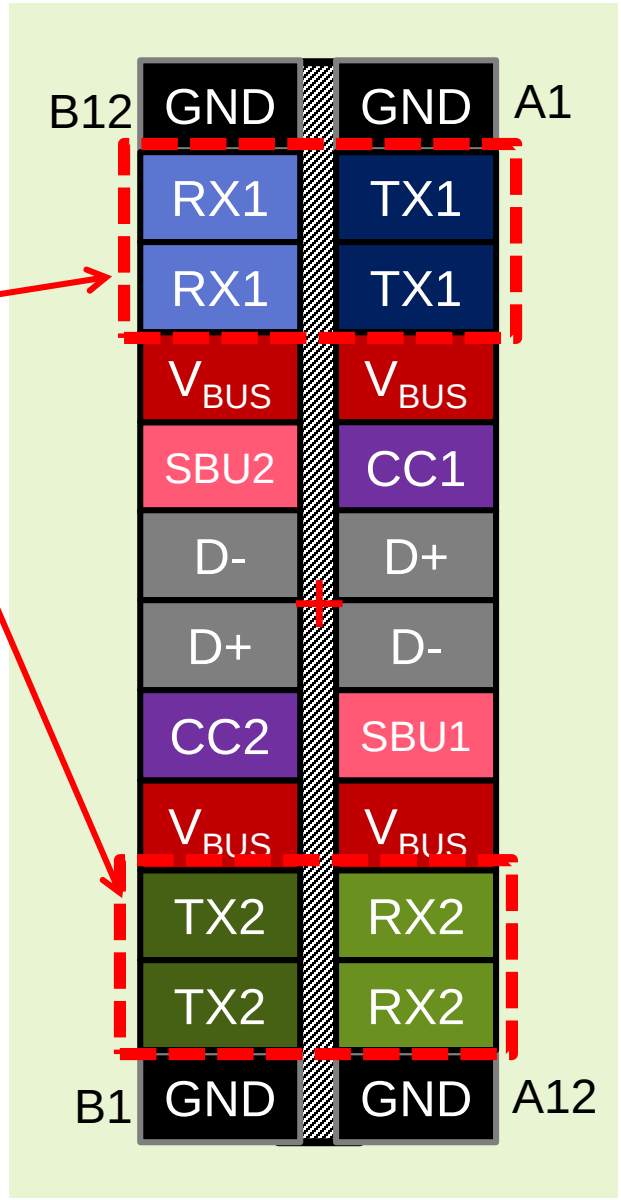
SUPERSPEED+ USB 10Gbps

THUNDERBOLT

USB Type C Signal Plan

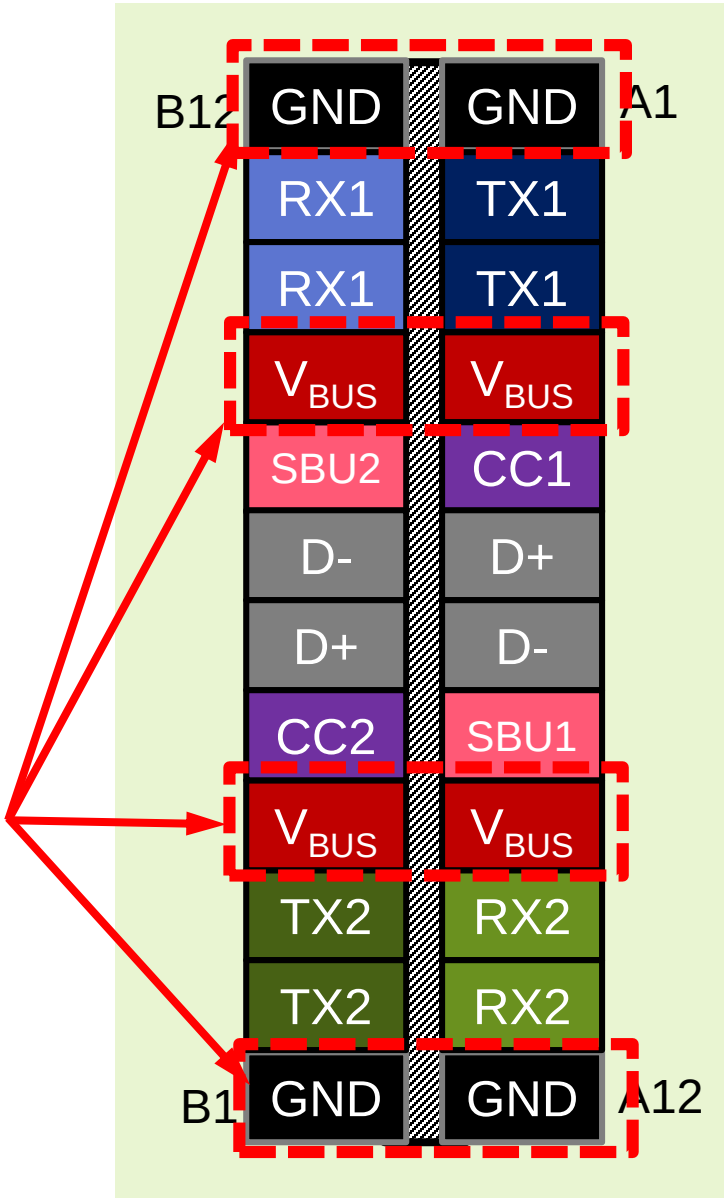
High Speed Lanes

4 High Speed Lanes:
Up to 20Gbs each



USB Type C Signal Plan

Power Pins



Power Pins

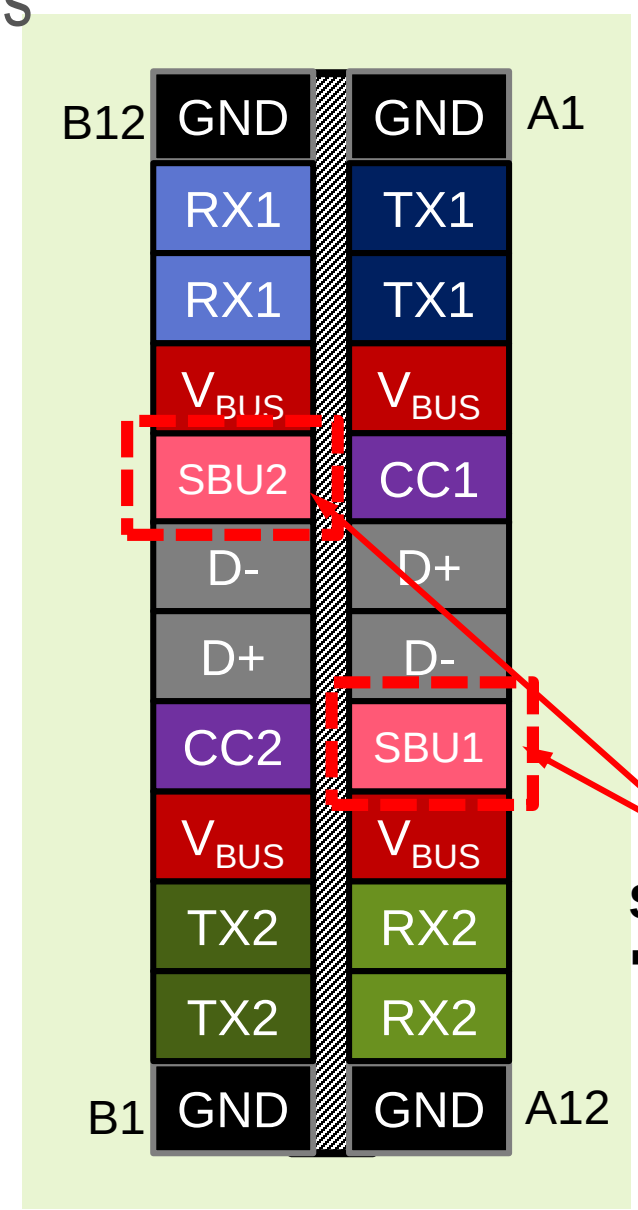
- **4 GND**
- **4 Supply Pins**

Handles up to 5 amps

KEYSIGHT TECHNOLOGIES

USB Type C Signal Plan

Sideband Use Pins

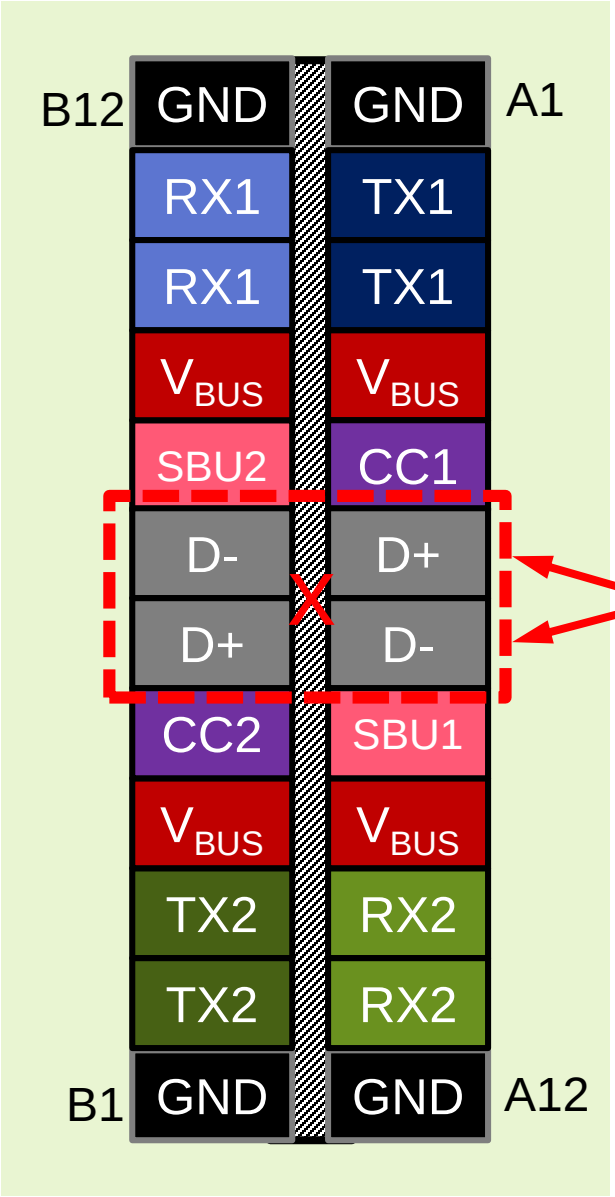


SBU lines:

- **Extra lines for alternate use**

USB Type C Signal Plan

USB2.0 Pins

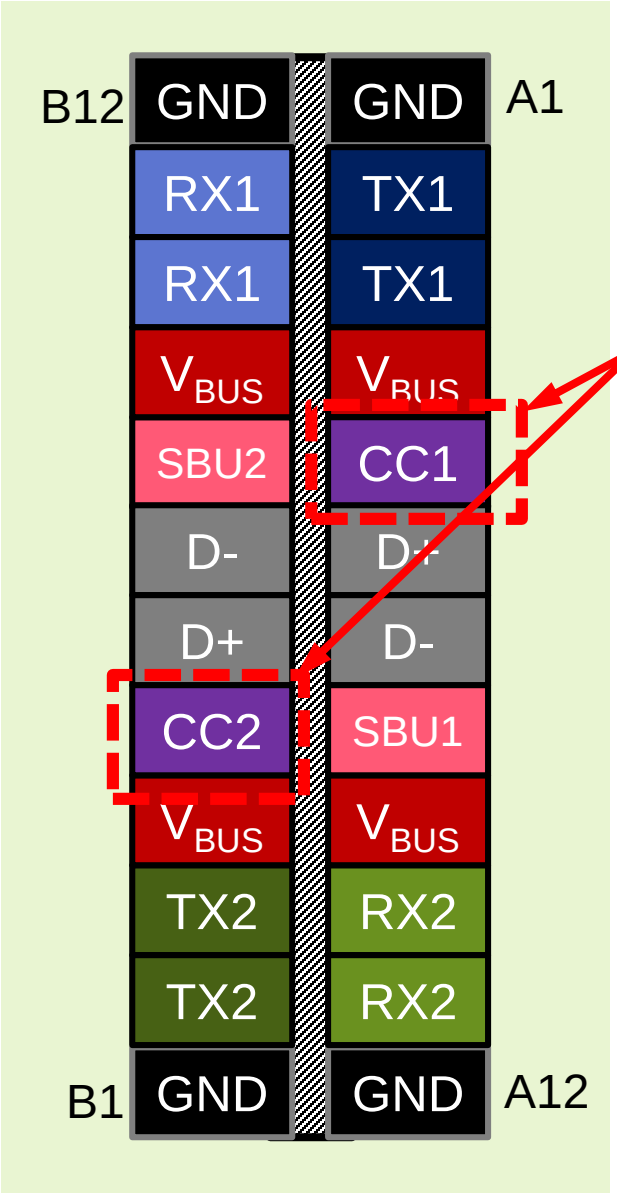


USB2 lines:

- **USB2 operation**
- **Link Communication**

USB Type C Signal Plan

CC Pins



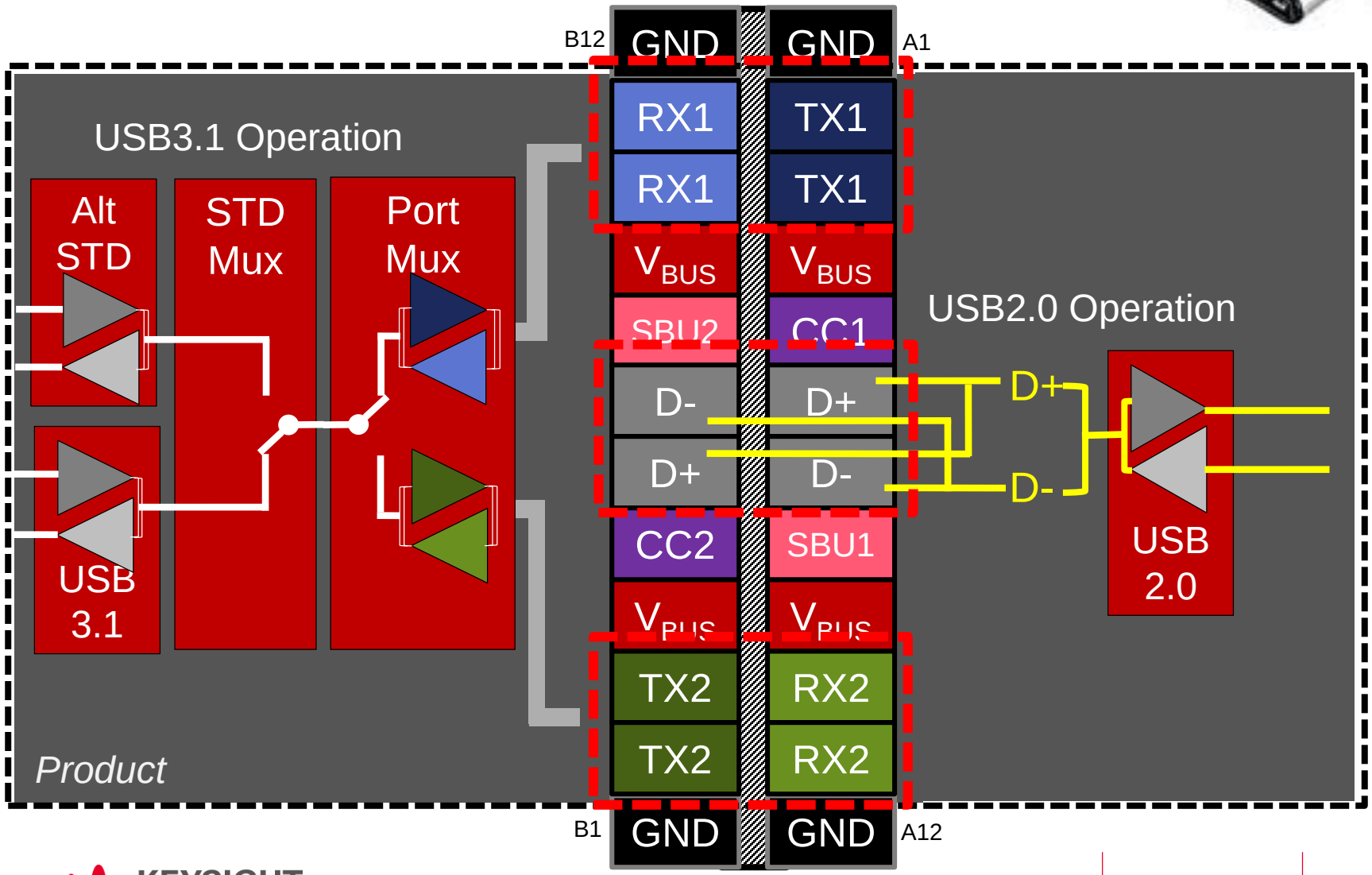
CC lines for:

- **Configuration Mngmt,**
- **Supply Power to Cable**
- **Power Delivery Communication**

KEYSIGHT TECHNOLOGIES

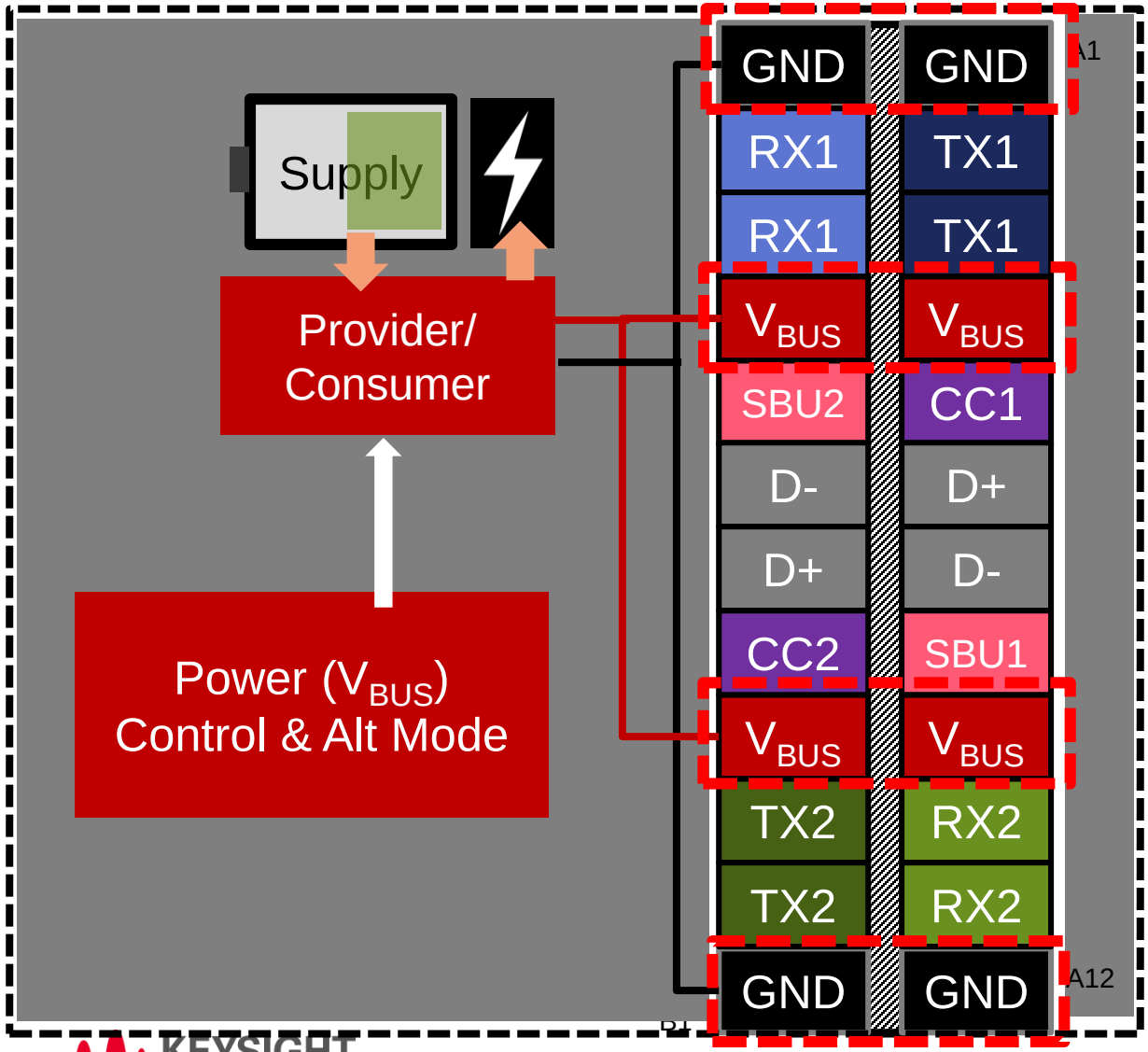
USB Type C Port Function

USB3.1 & USB2.0



USB Type C Port Function

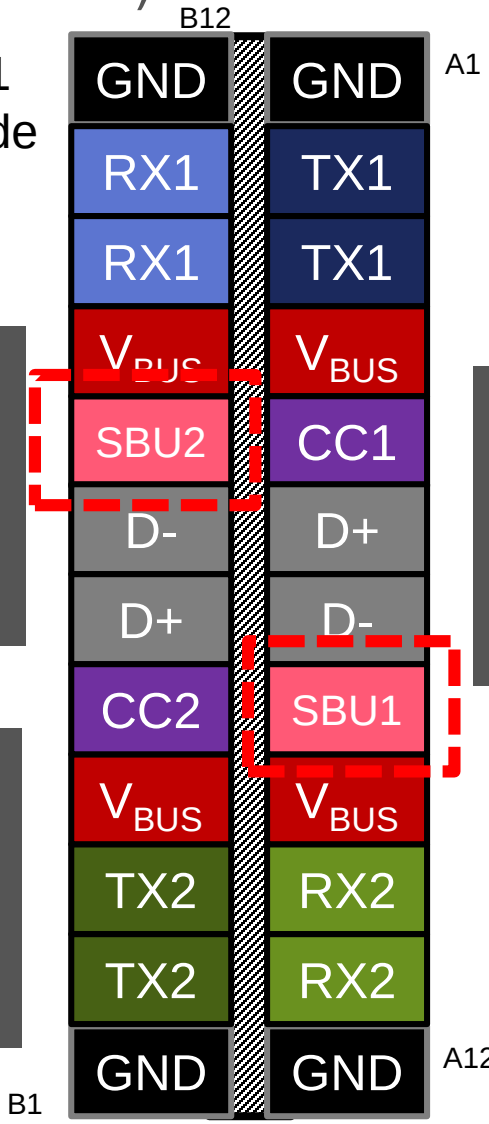
Power Lines



USB Type C Port Function

SBU Lines (Sideband Use)

SBU lines NOT used in USB3.1
Become active in alternate mode only to support the alternate technology.



DisplayPort

SBU1 -> AUX +
SBU2 -> AUX -

Thunderbolt

SBU1 -> LSRX
SBU2 -> LSTX

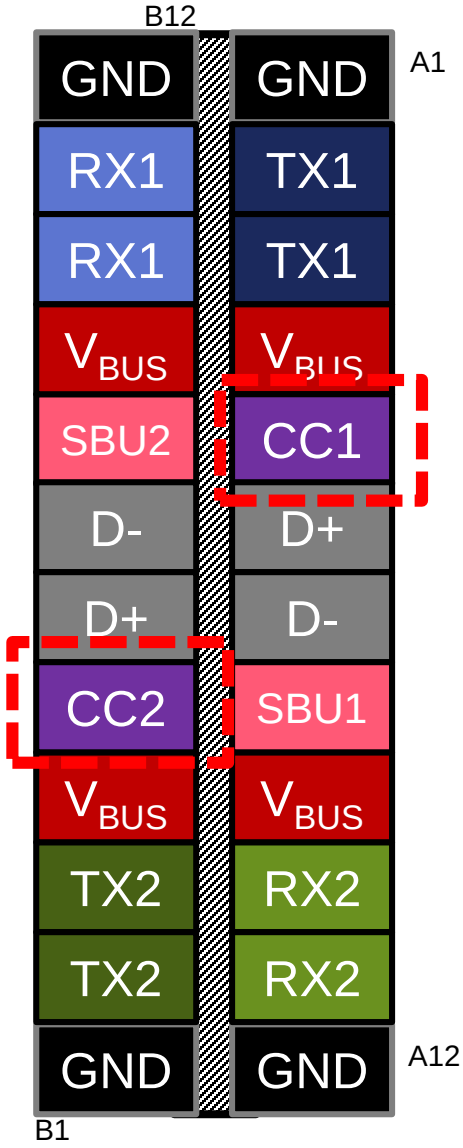
MHL

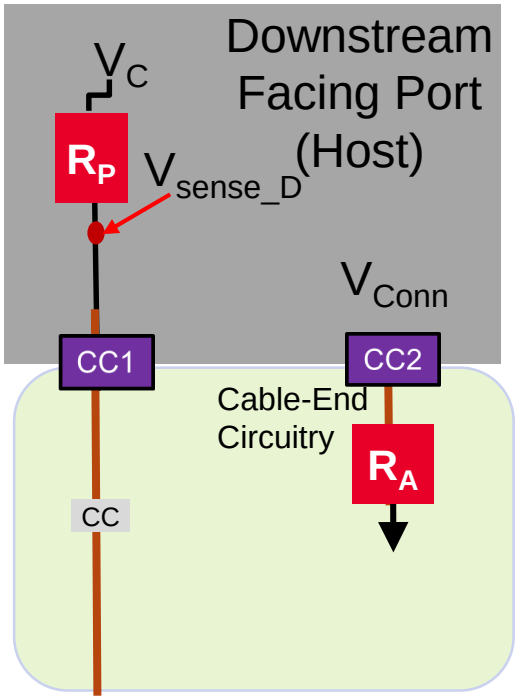
SBU1 -> e-CBUS-S
SBU2 -> e-CBUS-S

USB Type C Port Function

CC Lines (Configuration Channel)

CC1 and CC2 Sensed for Termination:
If cable termination (R_A) is present at CCn Then CCn=>V_{CONN}

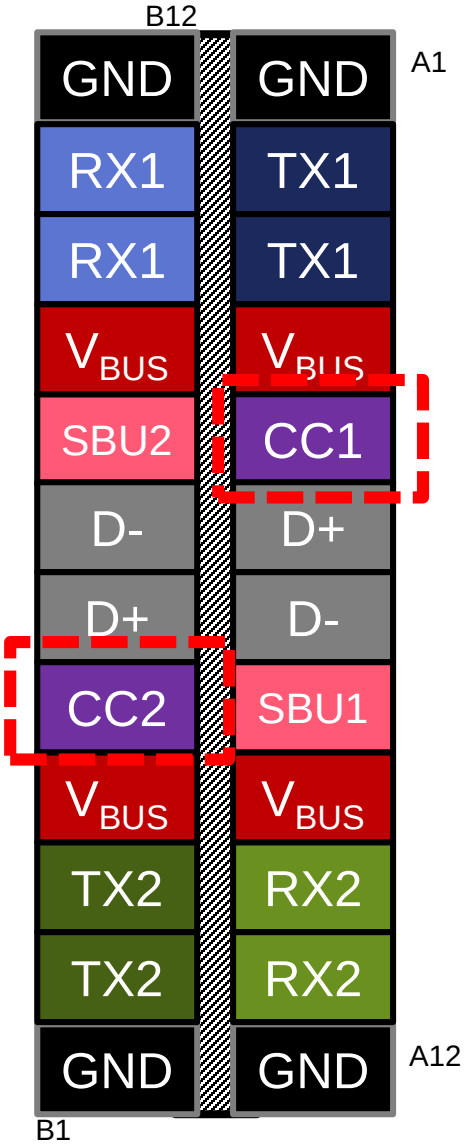


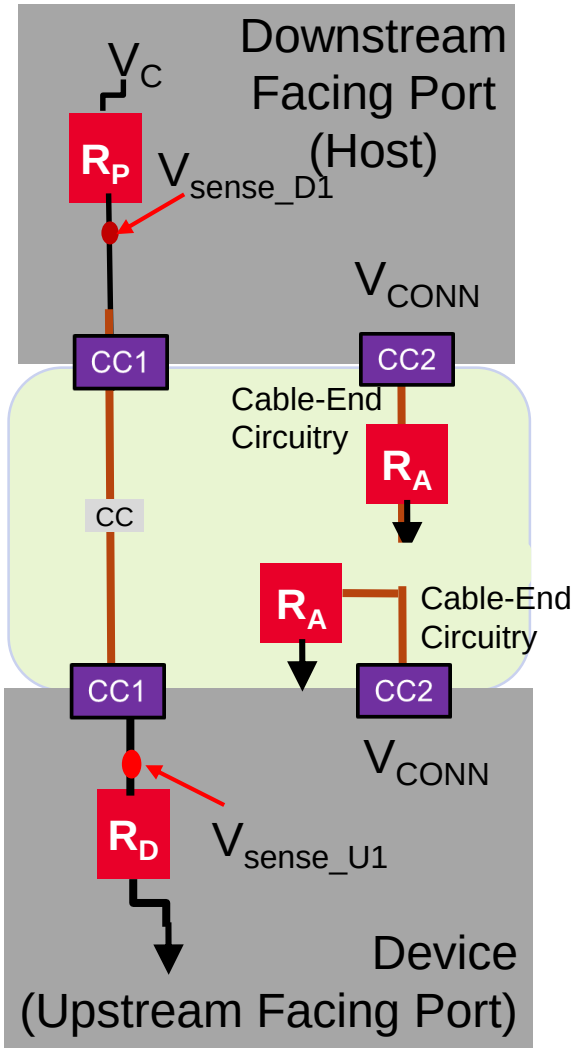


USB Type C Port Function

CC Lines (Configuration Channel)

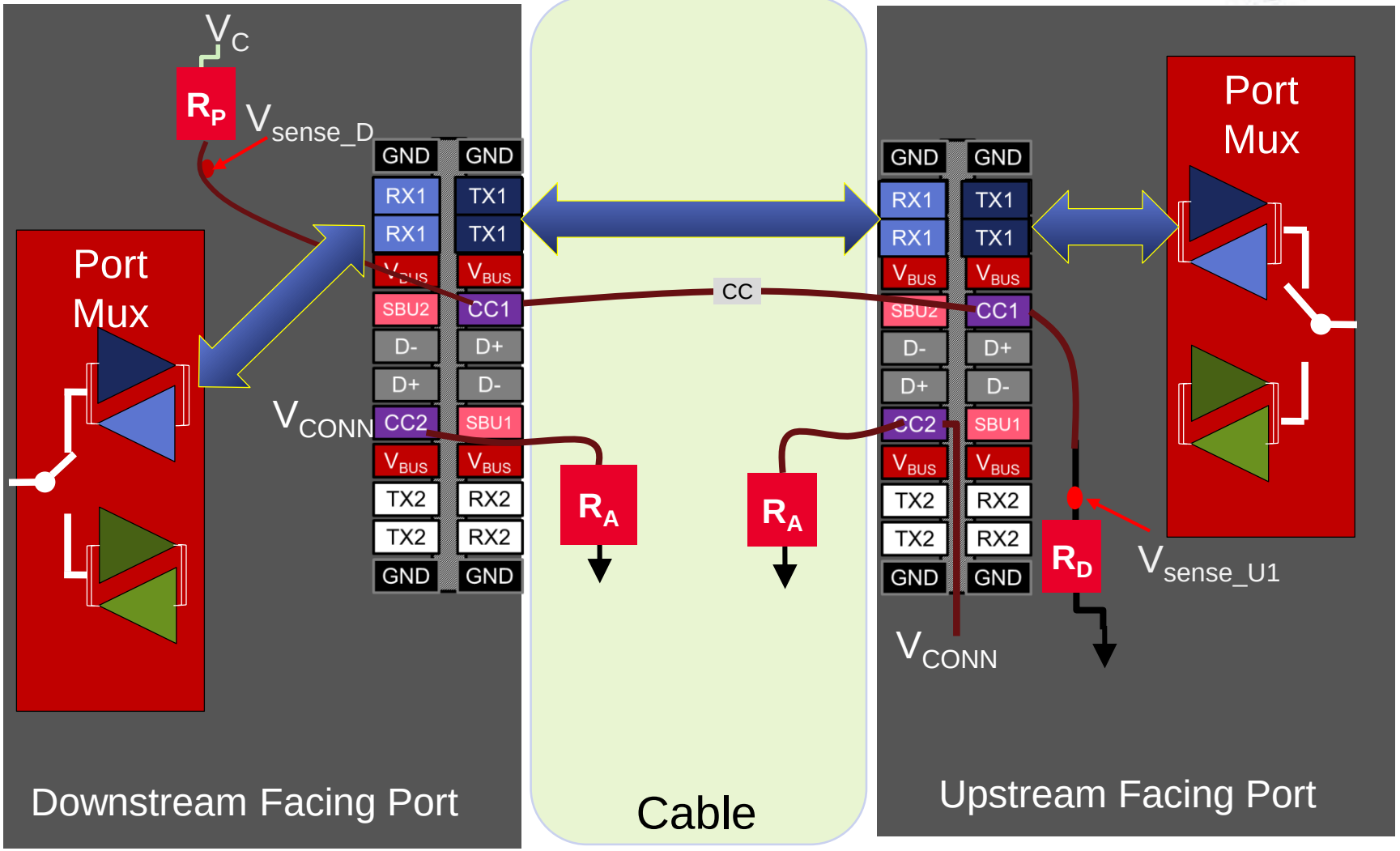
CC1 and CC2 Sensed for Termination:
If cable termination (R_A) is present at CCn Then
CCn=>V_{CONN}
Else
When Link partner terminated then Port orientations are known and CC Line becomes the power delivery channel.





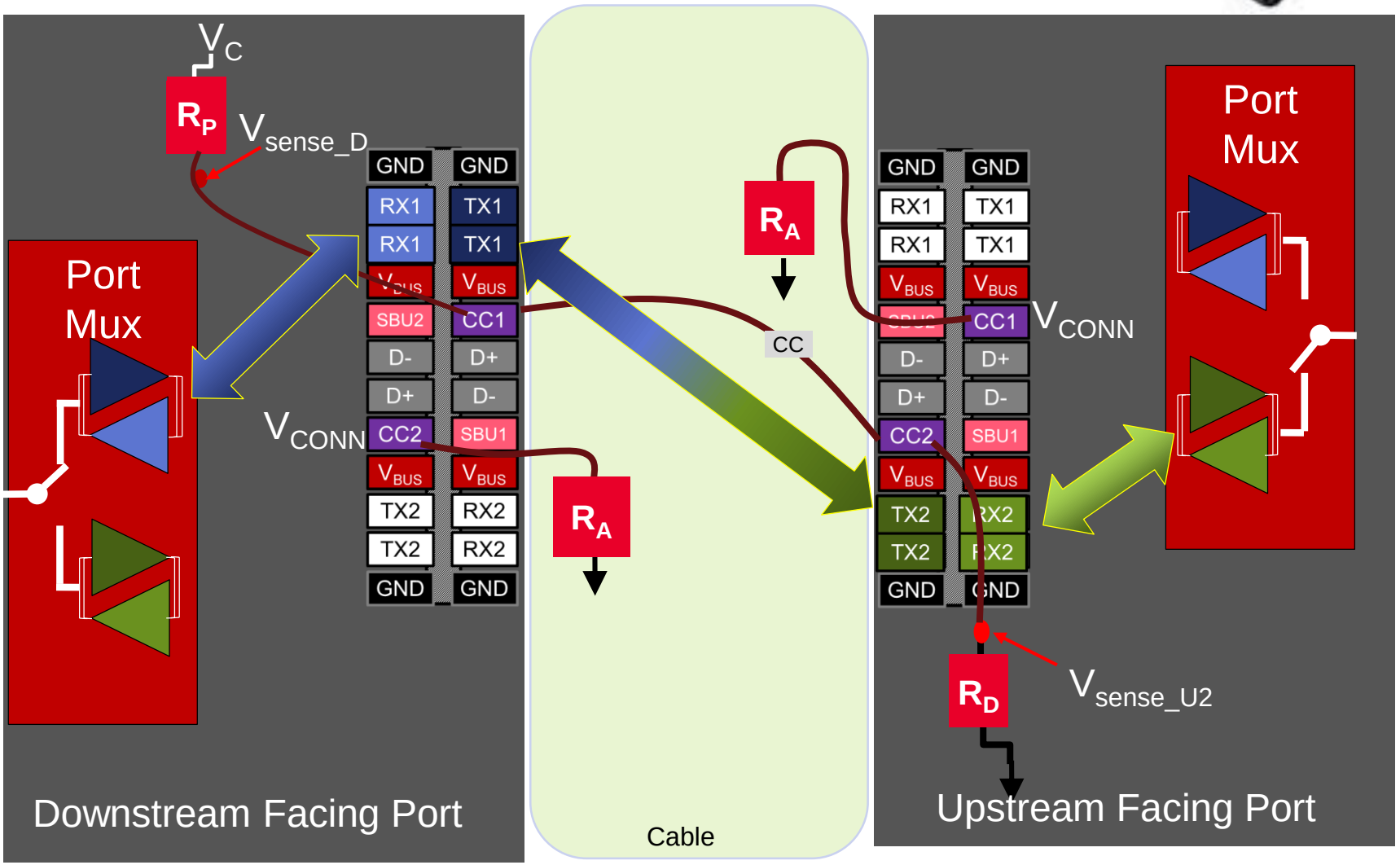
USB Type C Port Function

Port Configuration

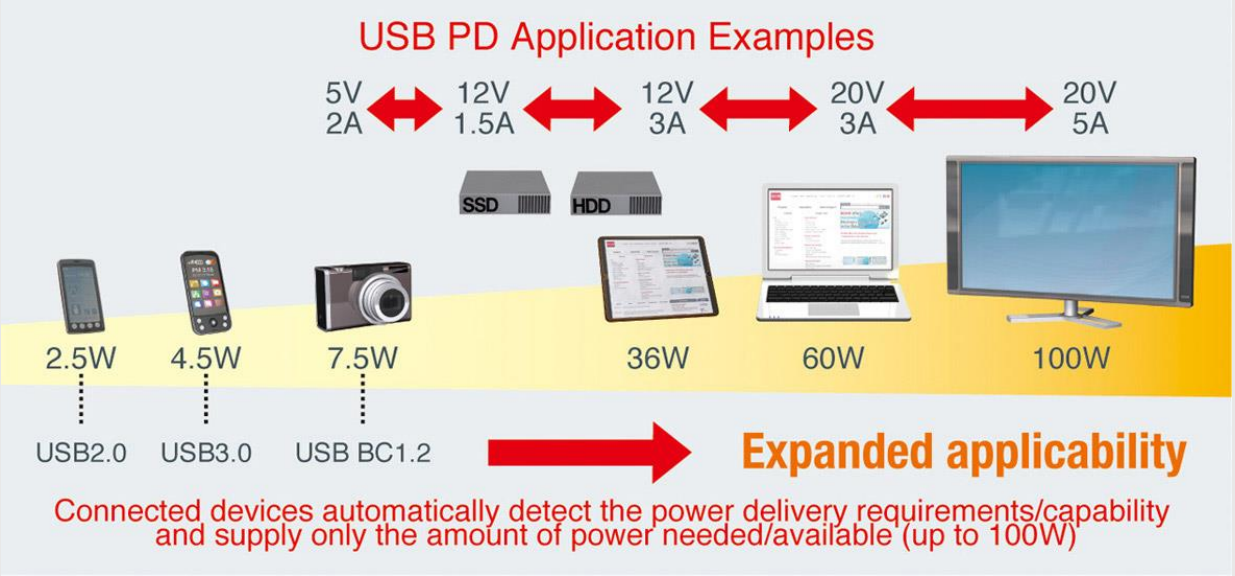


USB Type C Port Function

Port Configuration (Cable Flip at UFP)



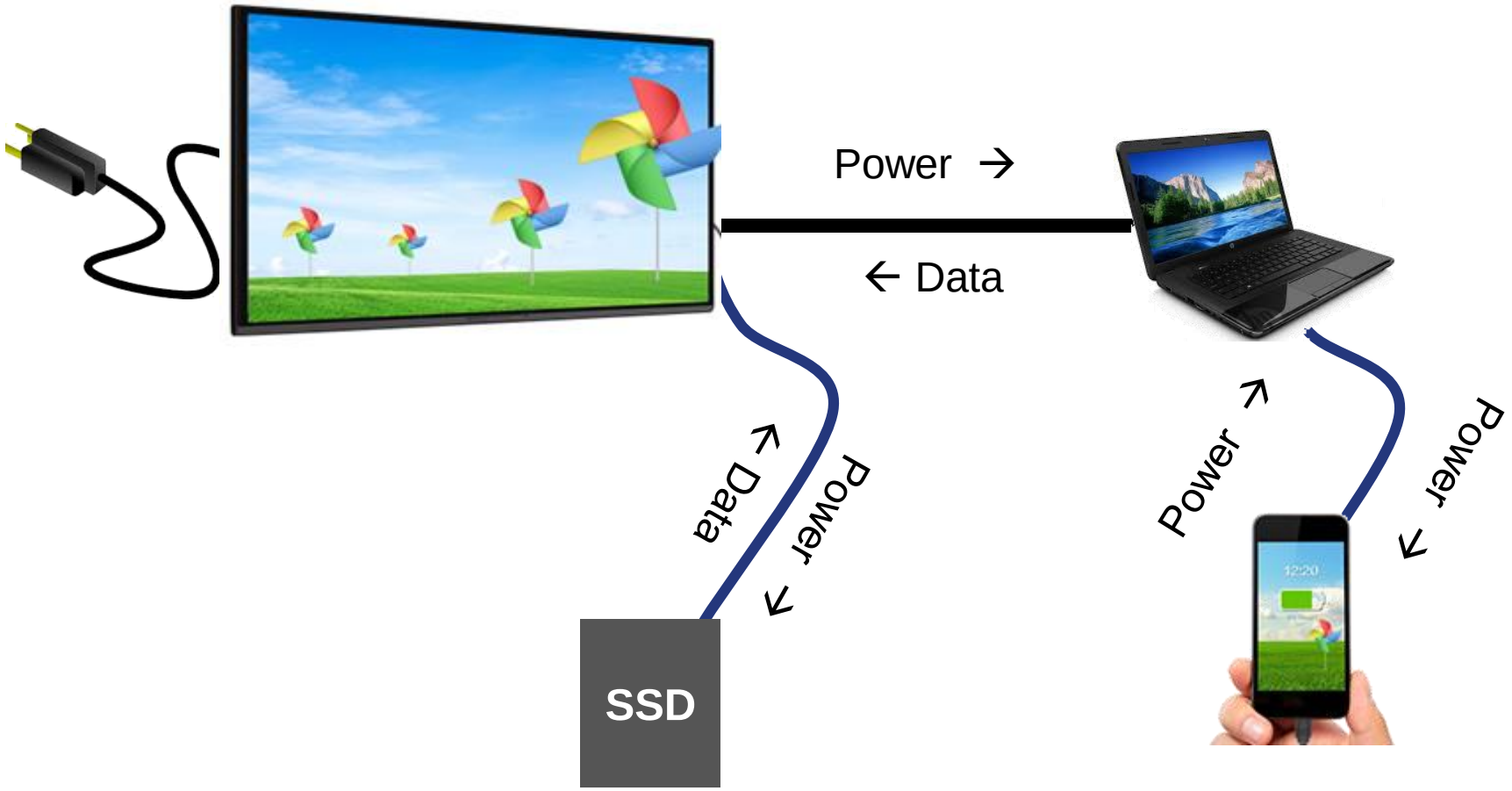
USB Type-C PD (Power Delivery) Validation Solutions



KEYSIGHT TECHNOLOGIES

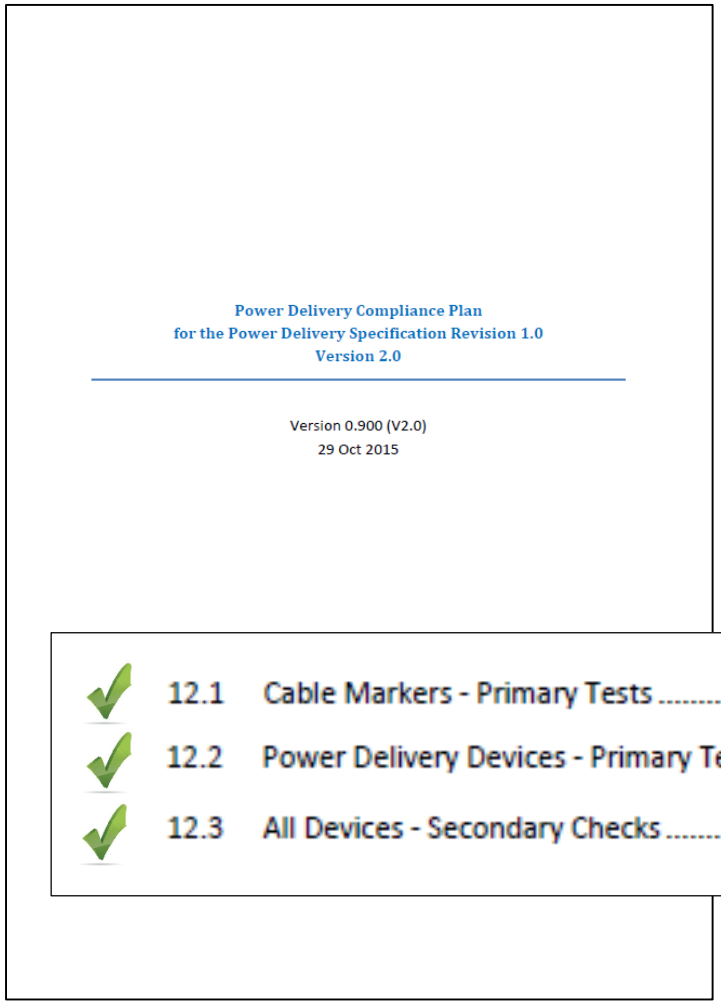
USB Power Delivery Example

Only 1 traditional wall power cord



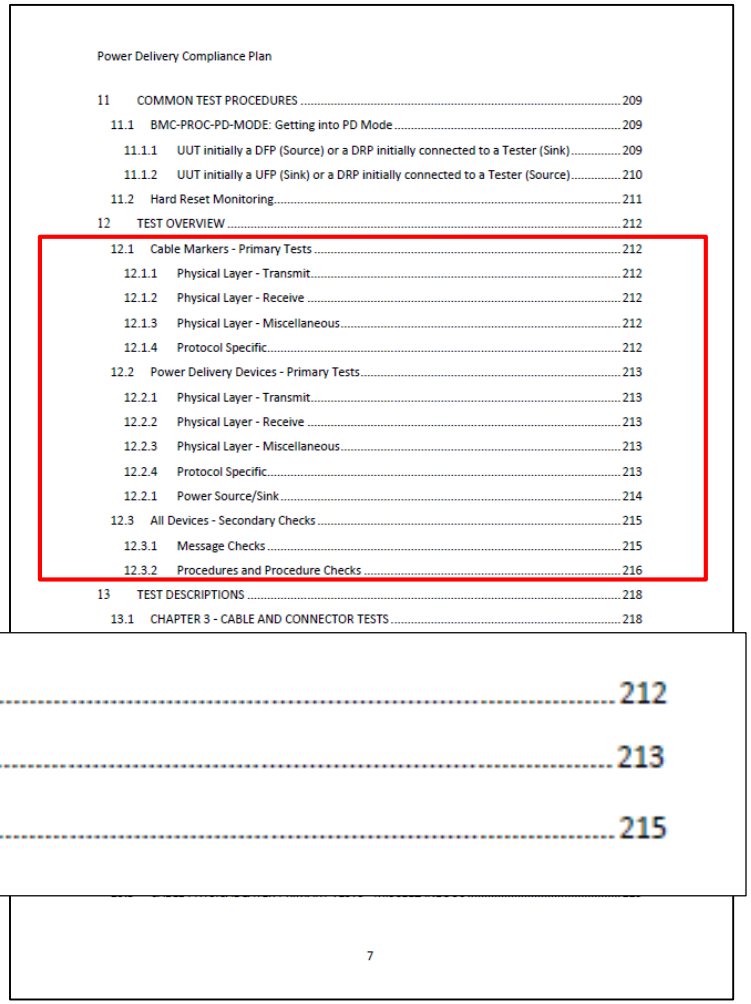
USB-PD Specification Test Plan

Three Test Sections



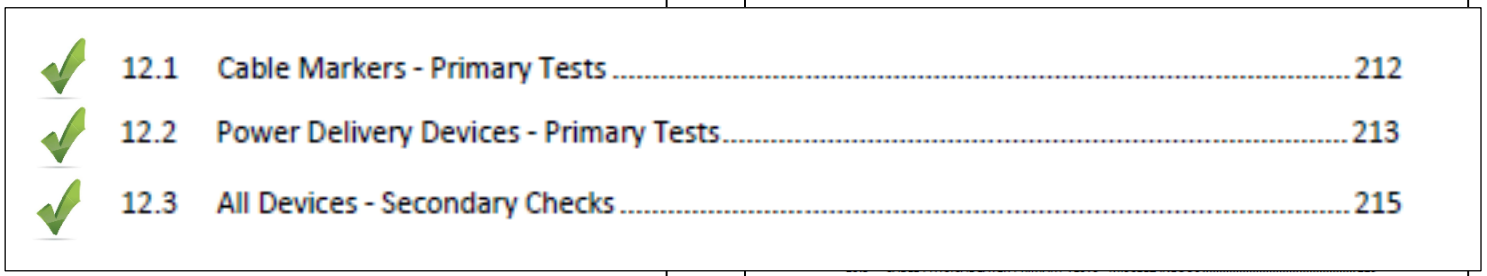
Power Delivery Compliance Plan
for the Power Delivery Specification Revision 1.0
Version 2.0

Version 0.900 (V2.0)
29 Oct 2015



Power Delivery Compliance Plan

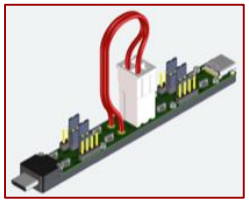
7

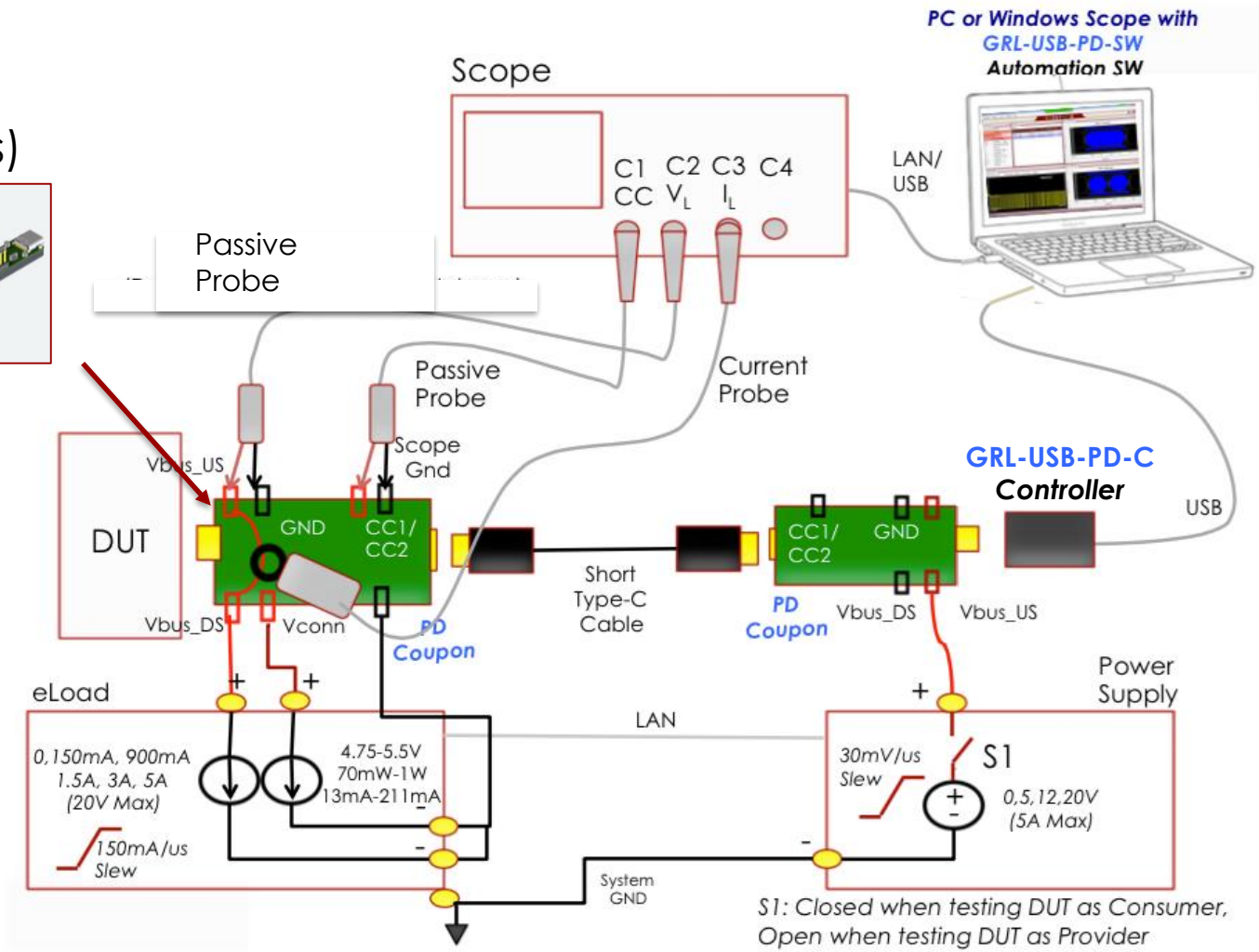


Chapter 5: Physical Layer Test
(Provider/Consumer)

GRL
GRANITE RIVER LABS

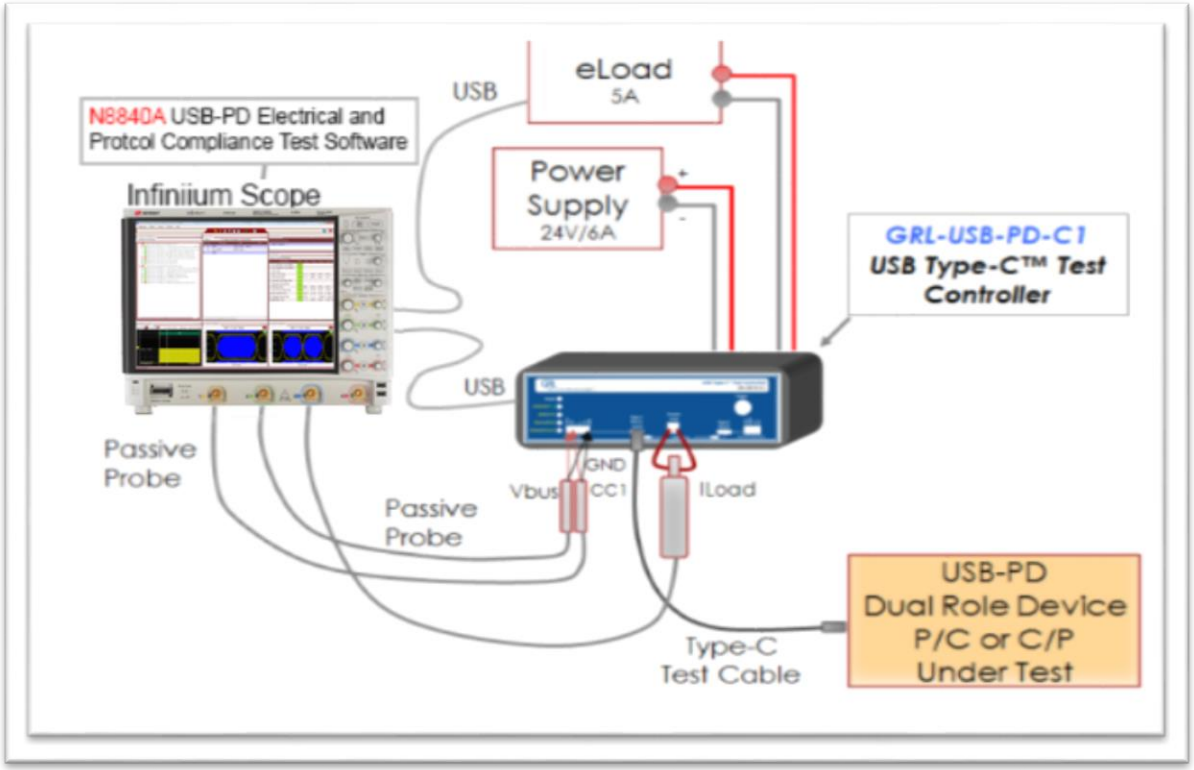
USB-PD Coupon(s)





USB-PD Device Testing using N8840A

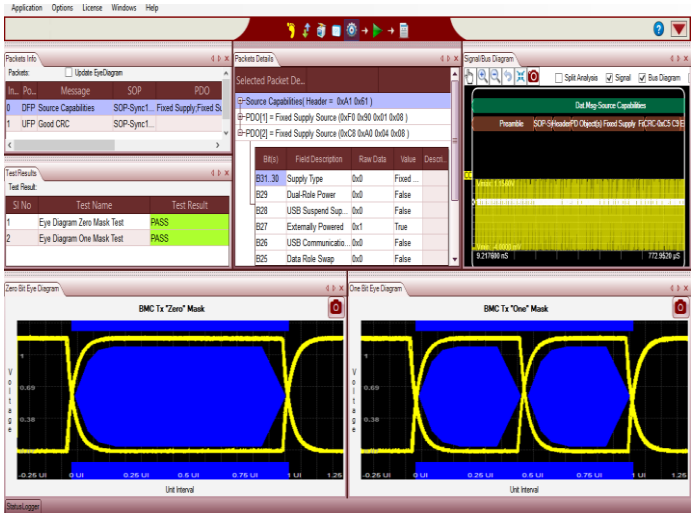
Test setup – Dual Role Devices (P/C or C/P)



- Requires electrical load (eLoad) and current probe for load test
- SMPS Power Adapter will be sufficient however an external power supply is recommended if a clean power source is needed for Vconn

N8840A USB-PD Electrical and Protocol Compliance Test Software

Power Delivery Compliance Testing

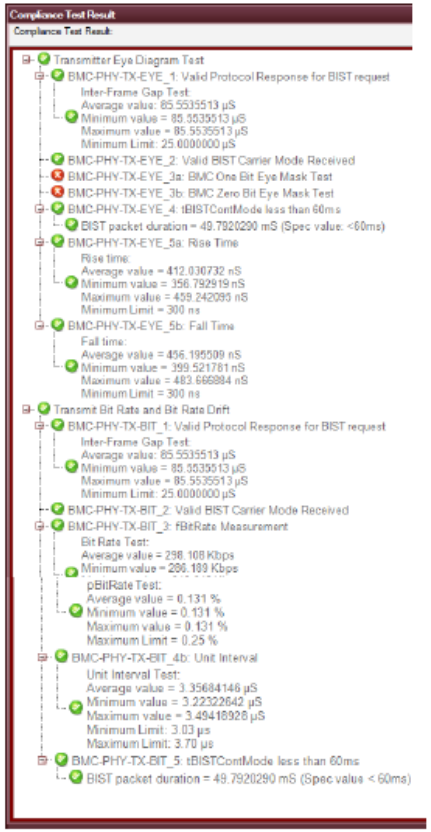


- Runs on Infiniium based oscilloscopes
  - S-Series recommended for hardware protocol trigger
- Performs BMC-PHY Compliance tests
- Performs BMC-PROT Compliance tests
- Performs BMC-POW Compliance tests
- Automates Compliance tests when used with Type-C Test Controller
- Developed in partnership with GRL (Granite River Labs)

USB-PD Device Testing using N8840A

Compliance Test Results

BMC PHY

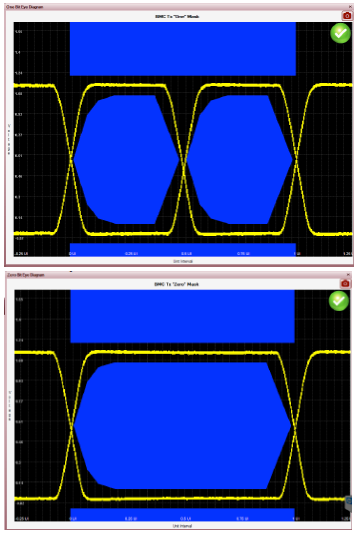


Power Loads and Transitions

- 12.11.1 POW_SRC_LOAD_P_PC
  - POW_SRC_LOAD_P_PC_1
    - DUT failed to send PING message when contracted to greater than 5V
  - POW_SRC_LOAD_P_PC_2
  - POW_SRC_LOAD_P_PC_PDO1_5V_3A
    - POW_SRC_LOAD_P_PC_3
    - POW_SRC_LOAD_P_PC_4
    - POW_SRC_LOAD_P_PC_5
    - POW_SRC_LOAD_P_PC_6
      - Load Current set to 0.75: Voltage drop = 0.032V (Limit: 0.25V)
      - Load Current set to 1.5: Voltage drop = 0.031V (Limit: 0.25V)
      - Load Current set to 2.25: Voltage drop = 0.265V (Limit: 0.25V)
      - Load Current set to 3: Voltage drop = 0.41V (Limit: 0.25V)
      - Load Current set to 2.25: Voltage drop = 0.283V (Limit: 0.25V)
      - Load Current set to 1.5: Voltage drop = 0.025V (Limit: 0.25V)
      - Load Current set to 0.75: Voltage drop = 0.044V (Limit: 0.25V)
  - POW_SRC_LOAD_P_PC_PDO2_12V_3A
    - POW_SRC_LOAD_P_PC_3
    - POW_SRC_LOAD_P_PC_4
    - POW_SRC_LOAD_P_PC_5
    - POW_SRC_LOAD_P_PC_6
      - Load Current set to 0.75: Voltage drop = 0.165V (Limit: 0.6V)
      - Load Current set to 1.5: Voltage drop = 0.075V (Limit: 0.6V)
      - Load Current set to 2.25: Voltage drop = 0.277V (Limit: 0.6V)
      - Load Current set to 3: Voltage drop = 0.422V (Limit: 1V)
      - Load Current set to 2.25: Voltage drop = 0.227V (Limit: 1V)
      - Load Current set to 1.5: Voltage drop = 0.007V (Limit: 1V)
      - Load Current set to 0.75: Voltage drop = 0.172V (Limit: 1V)
- 12.11.4 POW_SRC_TRANS_P_PC
  - POW_SRC_TRANS_P_PC_1
  - POW_SRC_TRANS_P_PC_2
    - POW_SRC_TRANS_P_PC_1_2
    - POW_SRC_TRANS_P_PC_2_1
    - POW_SRC_TRANS_P_PC_1_3
    - POW_SRC_TRANS_P_PC_3_2
    - POW_SRC_TRANS_P_PC_2_3
    - POW_SRC_TRANS_P_PC_3_1

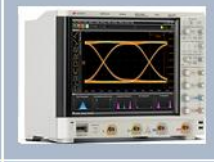
Power Role Swap

- POW_SWAP_PC_SRC_REQ
  - PROC_PD_MODE
  - PROT_PROC_SWAP_UUT_SRC
    - UUT could not initiate Power Role Swap
- POW_SWAP_PC_SNK_SRC
  - PROC-PD-MODE
  - PROT-PROC-SWAP-TSTR-SNK
  - PROT-PROC-SWAP-TSTR-SRC
- POW_SWAP_PC_SNK_SNK
  - PROC-PD-MODE
  - PROT-PROC-SWAP-TSTR-SNK
  - PROT-PROC-SWAP-UUT-SNK



PD Compliance Test Configuration

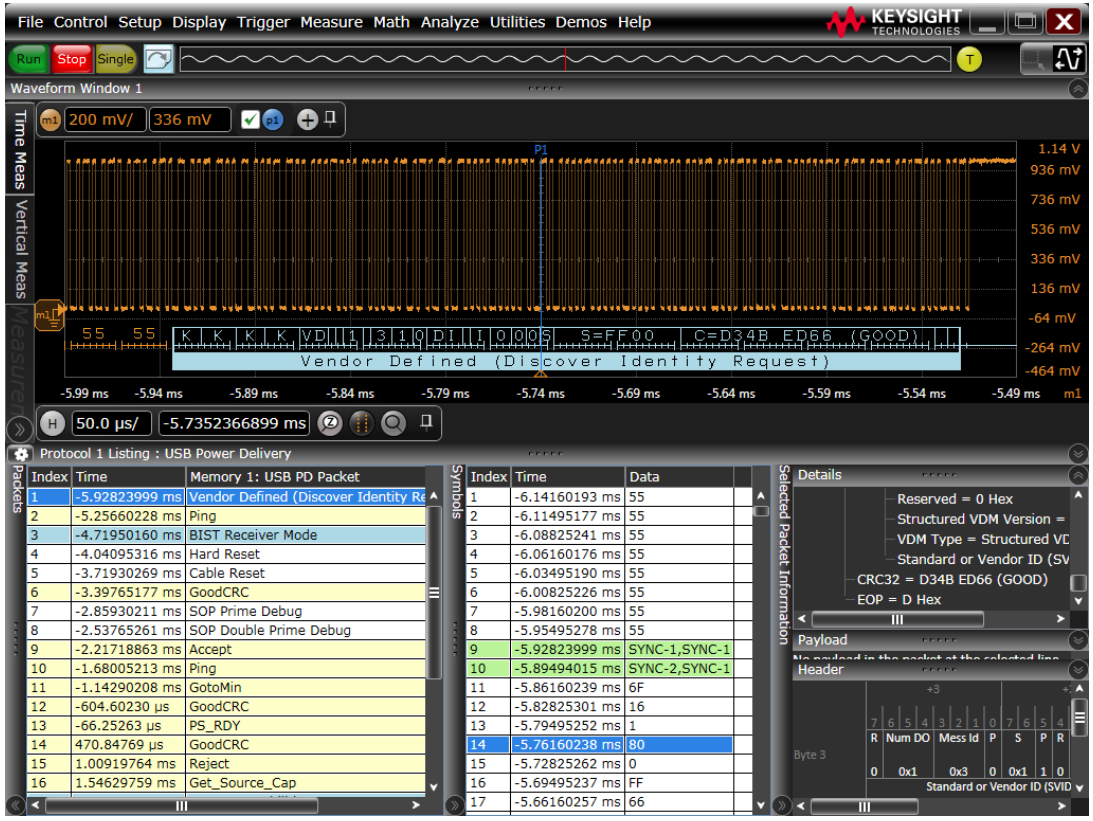
Dual Role Port (DRP) Test

Recommended Scope	Scope	Probe	
S-Series	 x1	 Passive Probe 10:1 500 MHz x2 N2873A (included with scope)	 1147A or N2893A x1
Compatible Scopes	**Scope**	**Probe Adapters**	
9000 Series	 x1	Passive Probe 10:1 500 MHz x2 N2873A (included with scope)	
90000X / V-Series	 x1	 High Impedance Adapter N5449A (includes passive probe) x 2	
Q-Series	 x1		
90000Q / Z-Series	 x1		
90000A Series	 x1	 E2697A x 2	 N2782B and N2279A

Required Products	
	N8840A x1
	PD controller x1 *(GRL-USB-PD-C1)*
	N3301A x1 *eLoad Mainframe*
	N3303A x1 *250W eLoad Module*
	82357B x1 *USB/GPIB Cable*
	PD coupon x1 *(USB3.1-C-PDC)*

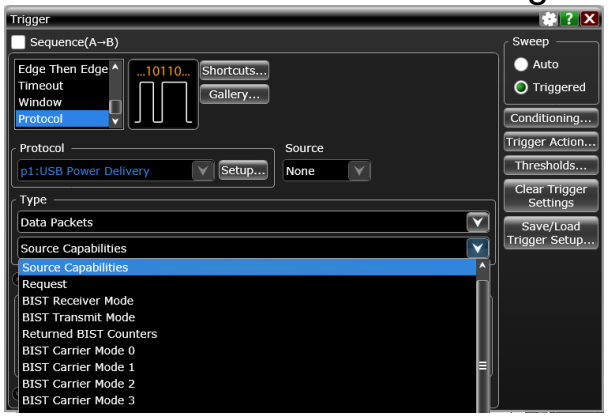
N8837A USB-PD Protocol Trigger and Decode

Keysight Power Delivery protocol decode and hardware triggering with S-Series



USB PD protocol decoding window example

USB PD CC and Vbus line signal

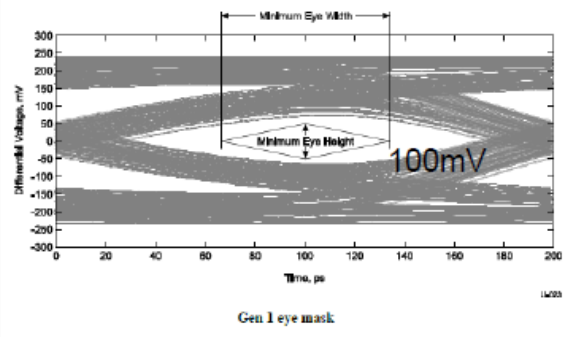
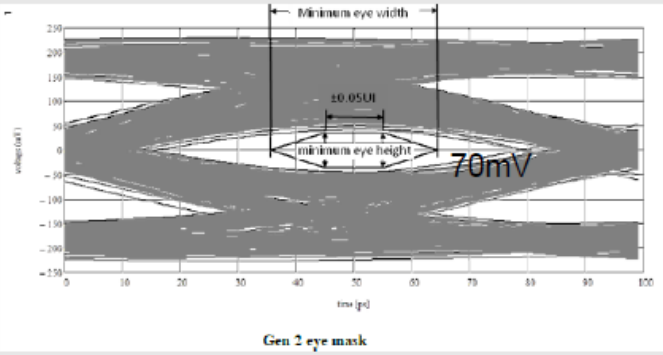


Hardware serial trigger in S-Series

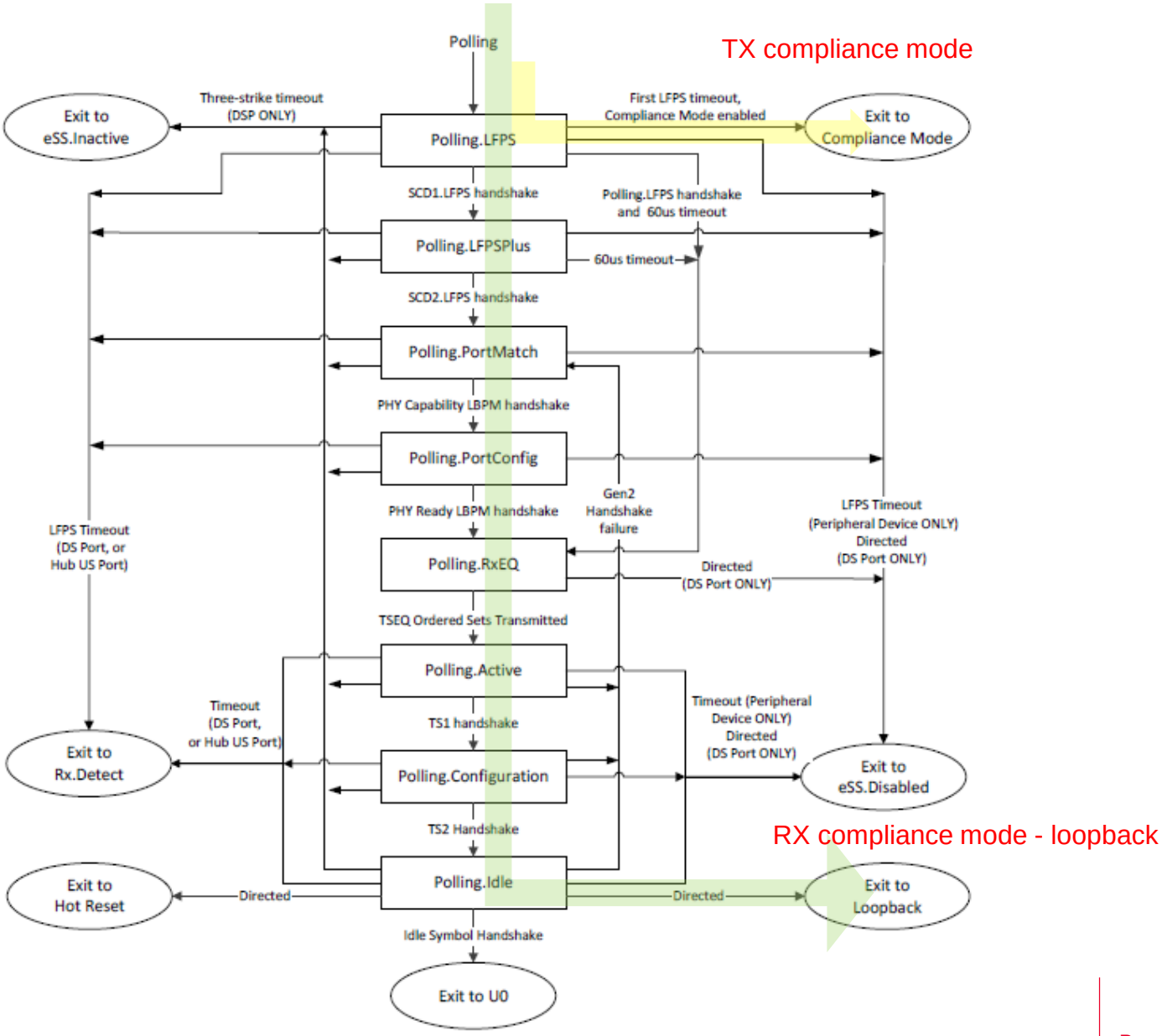
USB 3.1 Overview

KEYSIGHT TECHNOLOGIES

USB 3.1 Gen1 and Gen2

	Gen1	Gen2
Data rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b (20% additional bandwidth over 8b/10b)
Tx REF EQ	Normative Post: -3 dB	Informative Pre: 2.2 dB Post: -3.1 dB
Rx REF EQ	CTLE	CTLE (6 level) + 1 tap DFE
CDR (JTF BW)	4.9 MHz	7.5 MHz
Eye Height / Mask	 Gen 1 eye mask	 Gen 2 eye mask
TJ	132 psec (0.66 UI)	71.4 psec (0.714 UI)
Target Channel	3 meter (-17 dB @ 2.5 GHz)	1 meter -23 dB @ 5 GHz

USB 3.1 LTSSM

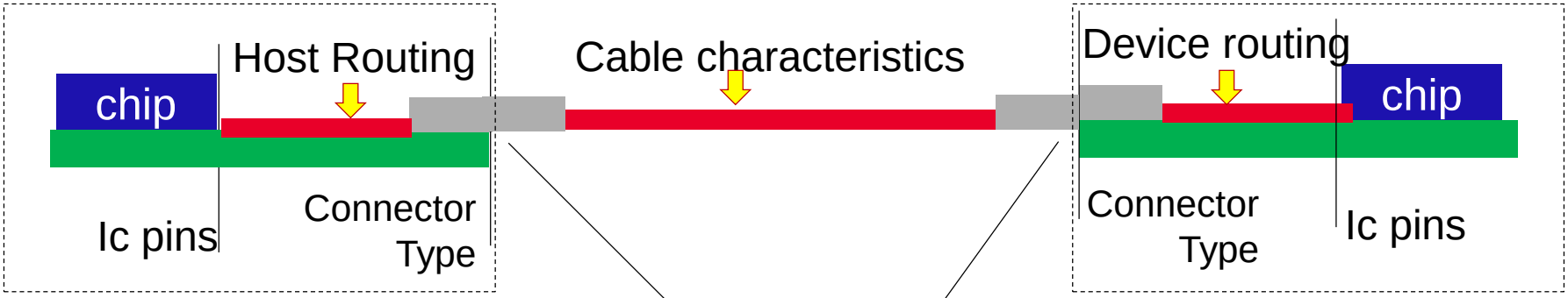

Polling
TX compliance mode
Exit to eSS.Inactive
Three-strike timeout (DSP ONLY)
Polling.LFPS
First LFPS timeout, Compliance Mode enabled
Exit to Compliance Mode
SCD1.LFPS handshake
Polling.LFPS handshake and 60us timeout
Polling.LFPSPlus
60us timeout
SCD2.LFPS handshake
Polling.PortMatch
PHY Capability LBPM handshake
Polling.PortConfig
LFPS Timeout (DS Port, or Hub US Port)
PHY Ready LBPM handshake
Gen2 Handshake failure
LFPS Timeout (Peripheral Device ONLY) Directed (DS Port ONLY)
Polling.RxEQ
Directed (DS Port ONLY)
TSEQ Ordered Sets Transmitted
Polling.Active
Timeout (DS Port, or Hub US Port)
Timeout (Peripheral Device ONLY) Directed (DS Port ONLY)
TS1 handshake
Exit to Rx.Detect
Polling.Configuration
Exit to eSS.Disabled
TS2 Handshake
RX compliance mode - loopback
Exit to Hot Reset
Directed
Polling.Idle
Directed
Exit to Loopback
Idle Symbol Handshake
Exit to U0

USB 3.1 Compliance Patterns

Table 6-13. Compliance Pattern Sequences

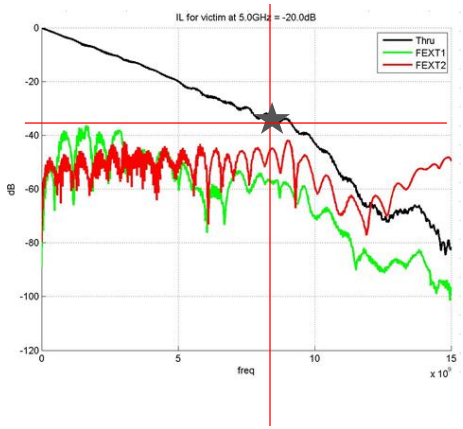
Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences.
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	~~With ~~wWithout de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP9		Pseudo-random data pattern (see section 6.4.4.1)
CP10	AAh	Nyquist pattern at 10Gb/s. This is not 128b132b encoded.
CP11	CCh	Nyquist/2 at 10Gb/s, This is not 128b132b encoded.
CP12	LFSR15	Uncoded LFSR15 for PHY level testing and fault isolation. This is not 128b132b encoded. The polynomial is x^15+x^14+1.
CP13	64 1's and 0's	With pre-shoot defined in section 6.7.5.2 (no de-emphasis). Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP14	64 1's and 0's	With de-emphasis defined in section 6.7.5.2 (no pre-shoot). Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP15	64 1's and 0's	With pre-shoot and de-emphasis defined in section 6.7.5.2. Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.
CP16	64 1's and 0's	No de-emphasis or pre-shoot. Repeating 64 1's and then 64 0's at 10Gb/s. This is not 128b132b encoded.

USB3.1 Channel Budget



Loss at Nyquist is identified here. Channel Models (s-parameters) required.

Data Rate	Host	Connector	Cable	Connector	Device
5G	10dB	Std A	7.5dB	Std B	2.5dB
5G	10dB	Std A	3.5dB	Micro B	6.5dB
5G	6.5dB	C	7dB	C	6.5dB
5G	10dB	Std A	3.5dB	C	6.5dB
5G	6.5dB	C	4dB	Std B	2.5dB
5G	6.5dB	C	4dB	Micro B	6.5dB
10G	8.5dB	Std A	6dB	Std B	8.5dB
10G	8.5dB	Std A	6dB	Micro B	8.5dB
10G	8.5dB	Std A	6dB	C	8.5dB
10G	8.5dB	C	6dB	Std B	8.5dB
10G	8.5dB	C	6dB	Micro B	8.5dB
10G	8.5dB	C	6dB	C	8.5dB

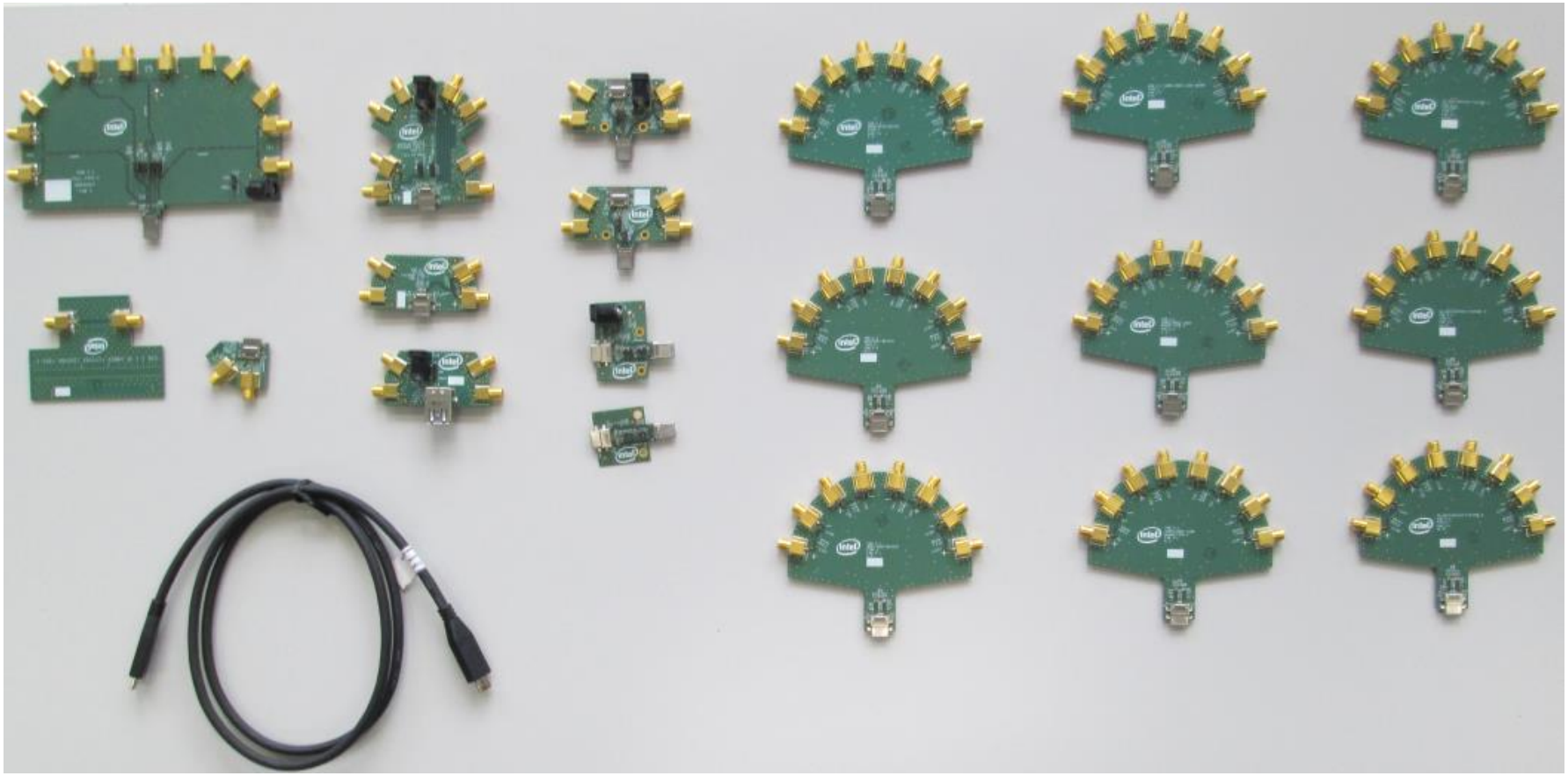


USB 3.1 Type-C TX Test Solutions

KEYSIGHT TECHNOLOGIES

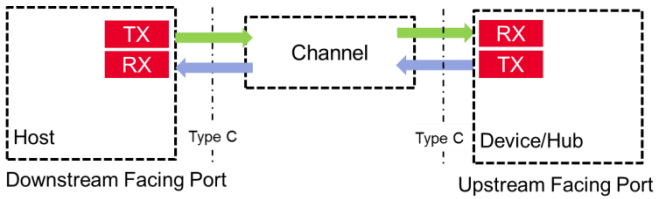
USB 3.1 gen2 10Gb/s

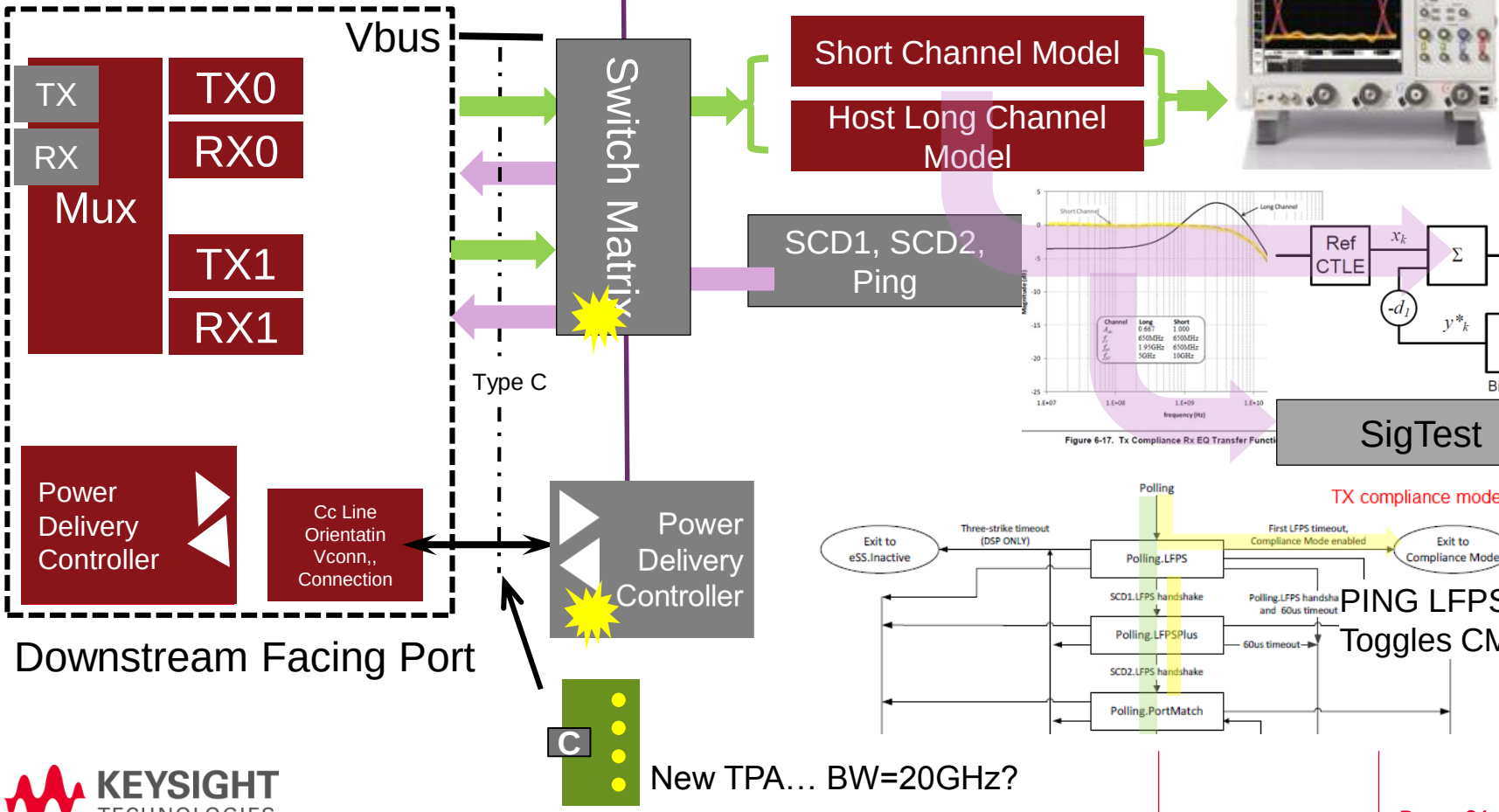
USB 3.1 Type C Fixture Kit rev 2 HW channel



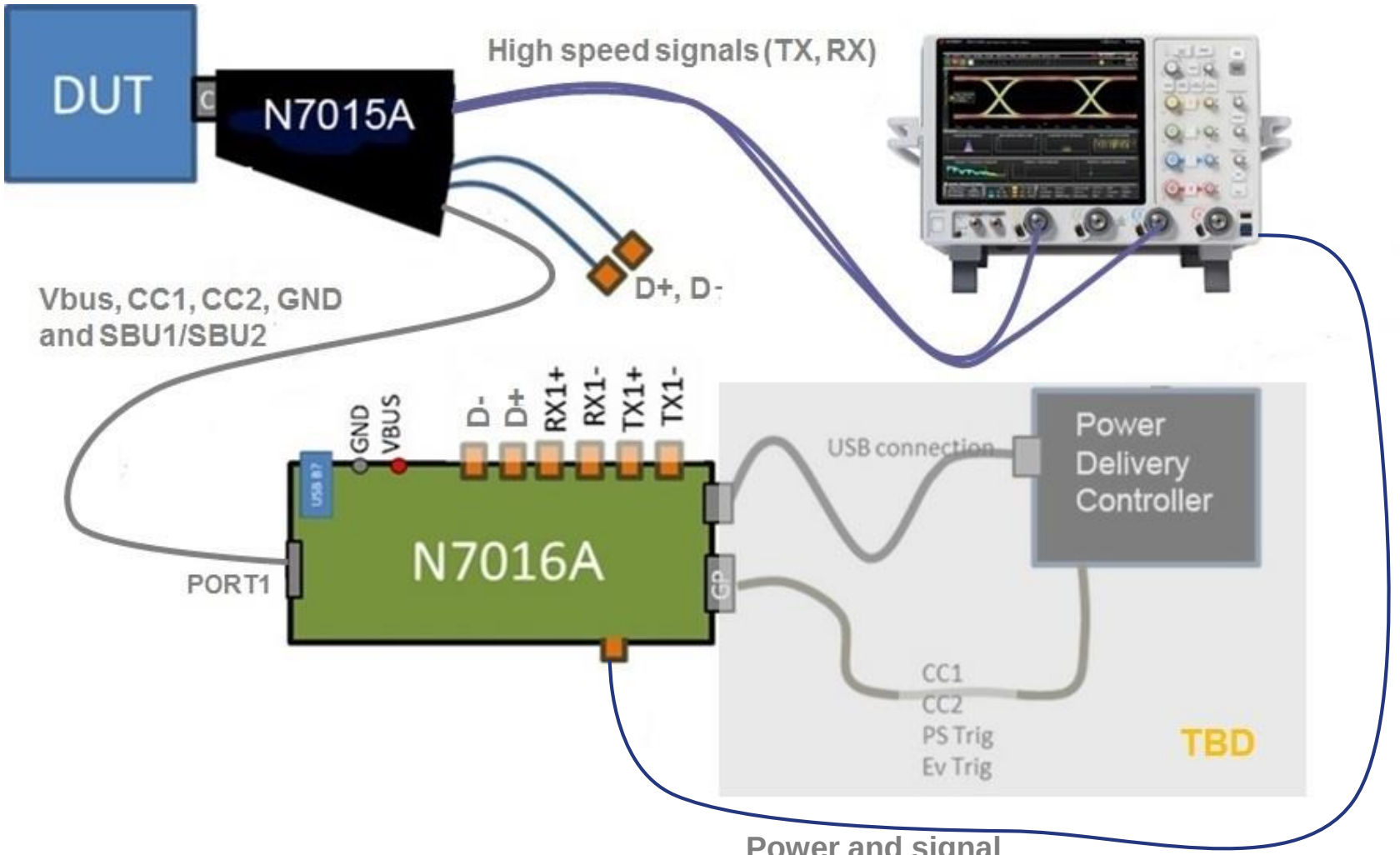
Testing USB 3.1

TX w/Type C

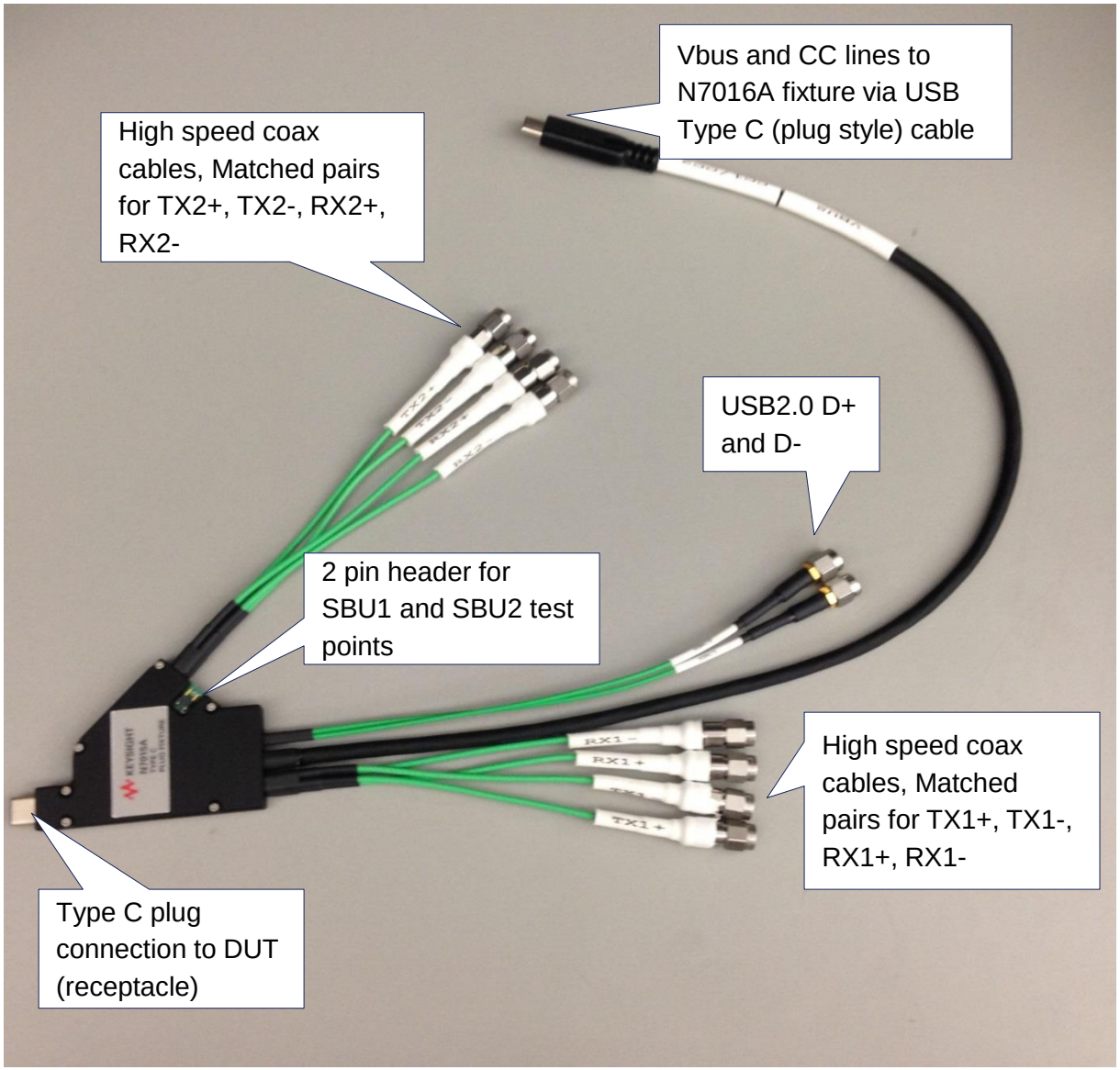




High level Test Setup for USB C-Connector



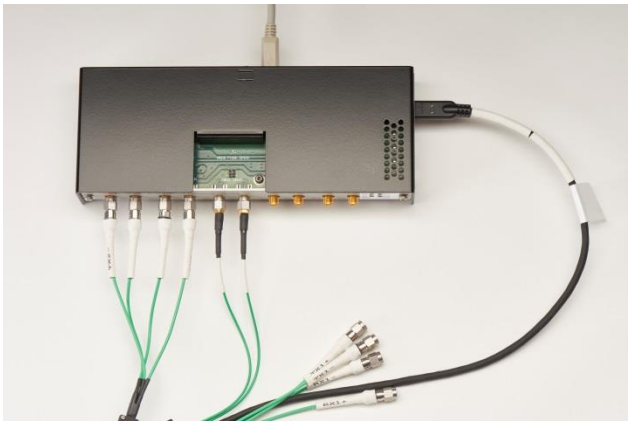
N7015A Type C Test Fixture



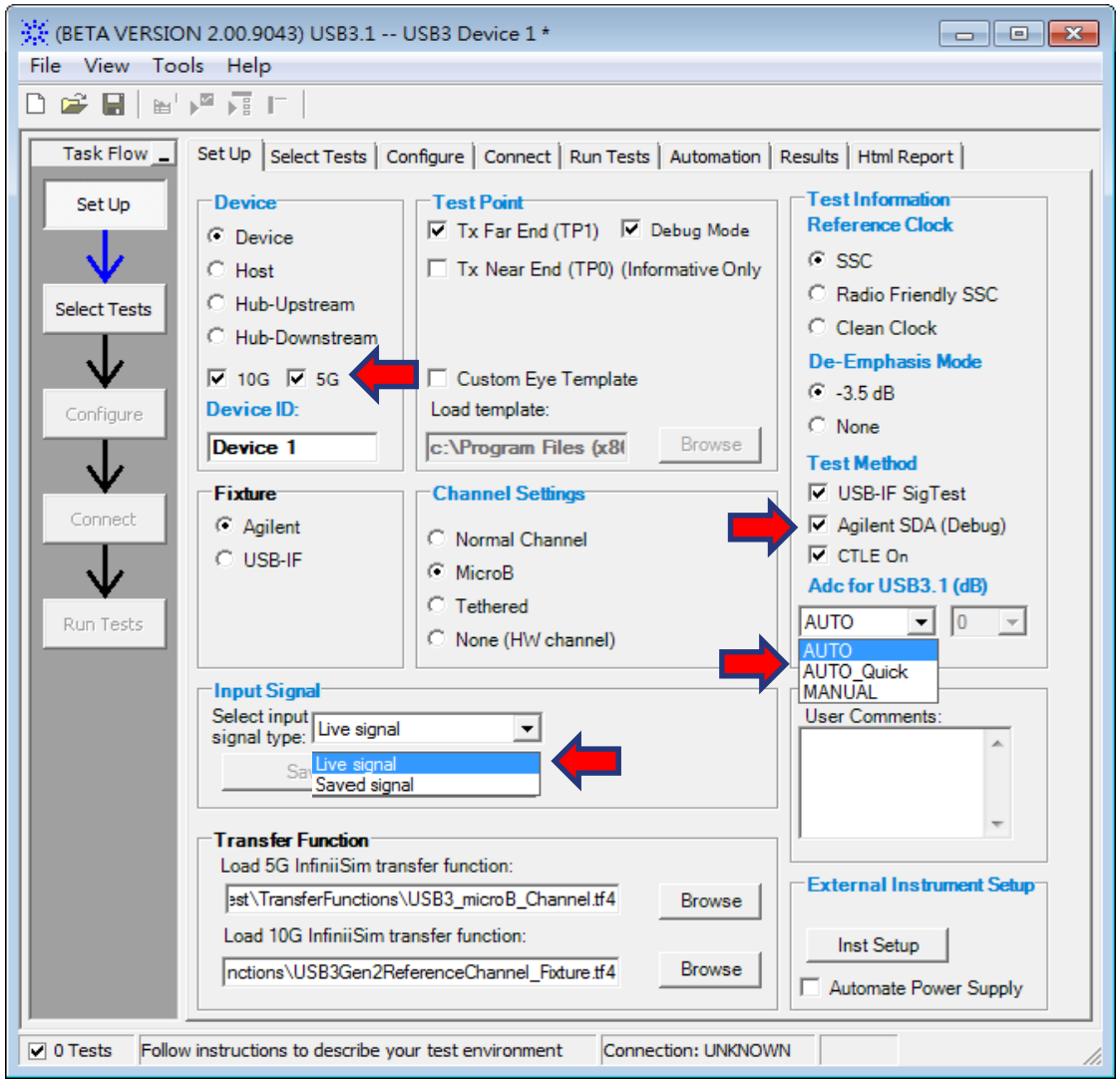
- High speed (TX/RX) and D+/D- lanes to scope through coax cables
- N7015A de-embedding models will be created and integrated in to compliance applications and Infiniium baseline software
- Power and Control signals to low speed N7016A fixture though type C cable
- View SBU1/2 signals

N7016A Type-C low speed signal access and control fixture

- Connects to N7015A through a captive C type cable (port 1) conveying CC_1, CC_2, SBU1, SBU2, V_{BUS} and GND
- Controls to terminate CC_1, CC_2 independently (Ra, Rp, Rd)
- Control to load Vconn (2 different loadings possible)
- External power for power consumers
- Type C receptacle to plug into other devices or cables (port 2)
- USB2.0 interface for external control from application or standalone SW on a PC



U7243B USB 3.1 TX Compliance Application



Keysight solution features:

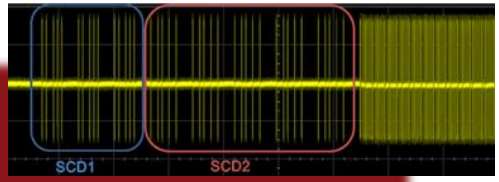
- ✓ Support USB3.1 Gen1/Gen2
- ✓ USB-IF Sigtest & Keysight SDA algorithm
- ✓ CTLE Adc scan
- ✓ Support live & saved waveform
- ✓ USB-IF and customer's embedded transfer function
- ✓ External instrument for triggering SCD1/2, LBPM and toggle Compliance Pattern

U7243B USB 3.1 TX Compliance Application

Set Up | Select Tests | Configure | Connect | Run Tests | Automation | Results | Html Report

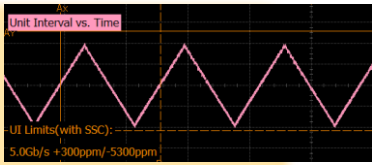
- All USB3 Tests
  - 5G Test
  - 10G Test
    - 10G Transmitter Low Frequency Periodic Signaling Tests
    - 10G SCD and LBPS Tests
      - 10G LBPS tPWM
      - 10G LBPS tLFPS_0
      - 10G LBPS tLFPS_1
      - 10G SuperSpeedPlus Capability Declaration (SCD1)
      - 10G SuperSpeedPlus Capability Declaration (SCD2)
      - 10G SCD Rise Time
      - 10G SCD Fall Time
      - 10G SCD Duty Cycle
      - 10G SCD Period
      - 10G SCD tRepeat
      - 10G SCD tBurst
      - 10G SCD Differential Voltage
      - 10G SCD Common Mode Voltage
    - 10G Transmitter SSC Tests
      - 10G TSSC-Freq-Dev-Min
      - 10G TSSC-Freq-Dev-Max
      - 10G SSC Modulation Rate
      - 10G SSC df/dt
    - 10G eye measurement test
      - CTLE_Adc Selection
    - 10G Transmitter Eye Far End (TP1) Tests (Agilent SDA)(CTLE On)
      - 10G Far End Template Test (SDA)(CTLE ON)
      - 10G Far End Differential Output Voltage (SDA)(CTLE ON)
      - 10G Far End Random Jitter (SDA)(CTLE ON)
      - 10G Far End Maximum Deterministic Jitter (SDA)(CTLE ON)
      - 10G Far End Total Jitter at BER-12 (SDA)(CTLE ON)
    - 10G Transmitter Eye Far End (TP1) Tests (USB-IF SigTest)(CTLE On)
      - 10G Far End Random Jitter (CTLE ON)
      - 10G Far End Maximum Deterministic Jitter (CTLE ON)
      - 10G Far End Total Jitter at BER-12 (CTLE ON)
      - 10G Far End Template Test (CTLE ON)
      - 10G Far End Differential Output Voltage (CTLE ON)

Gen 1 test items, LFPS, SSC, eye mask, Jitter



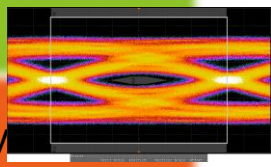
Gen2 LFPS, tRepeat, tBurst , tPWM, tLFPS_0, tLFPS_1

SSC test items



Select/Scan for optimal Adc of CTLE

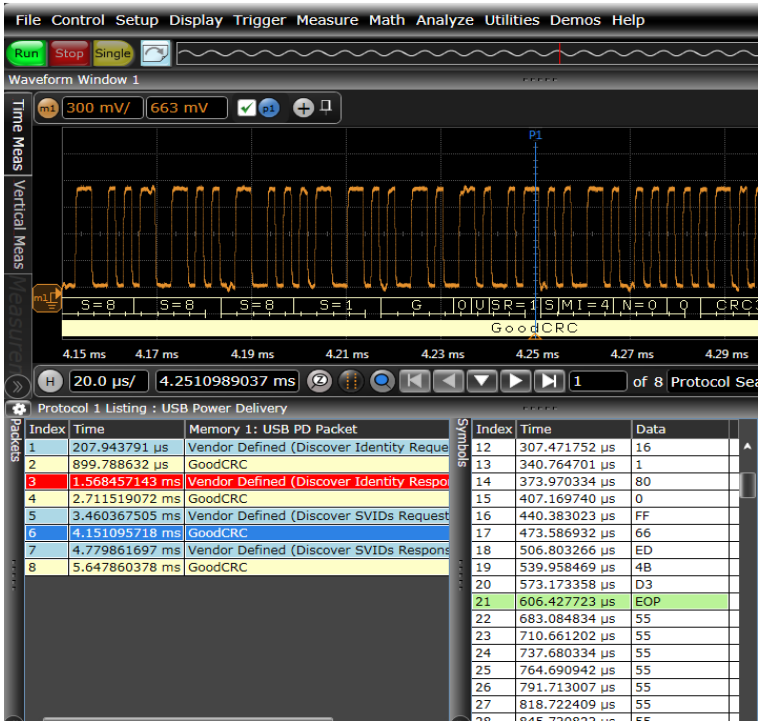
Eye mask and Jitter test by SDA algorithm



Eye mask and Jitter test by SigTest algorithm

N8821A/B USB 3.1 Gen1/Gen2 Protocol Trigger and Decode

- USB 3.1 Gen1 and Gen 2 protocol decode in less than 30 seconds
- Integrated software-based protocol-level triggers
- Save time and eliminate errors by viewing packets at the protocol level
- Use time-correlated views to quickly troubleshoot serial protocol problems back to their timing or signal integrity root cause



USB 3.1 Type-C RX Test Solutions

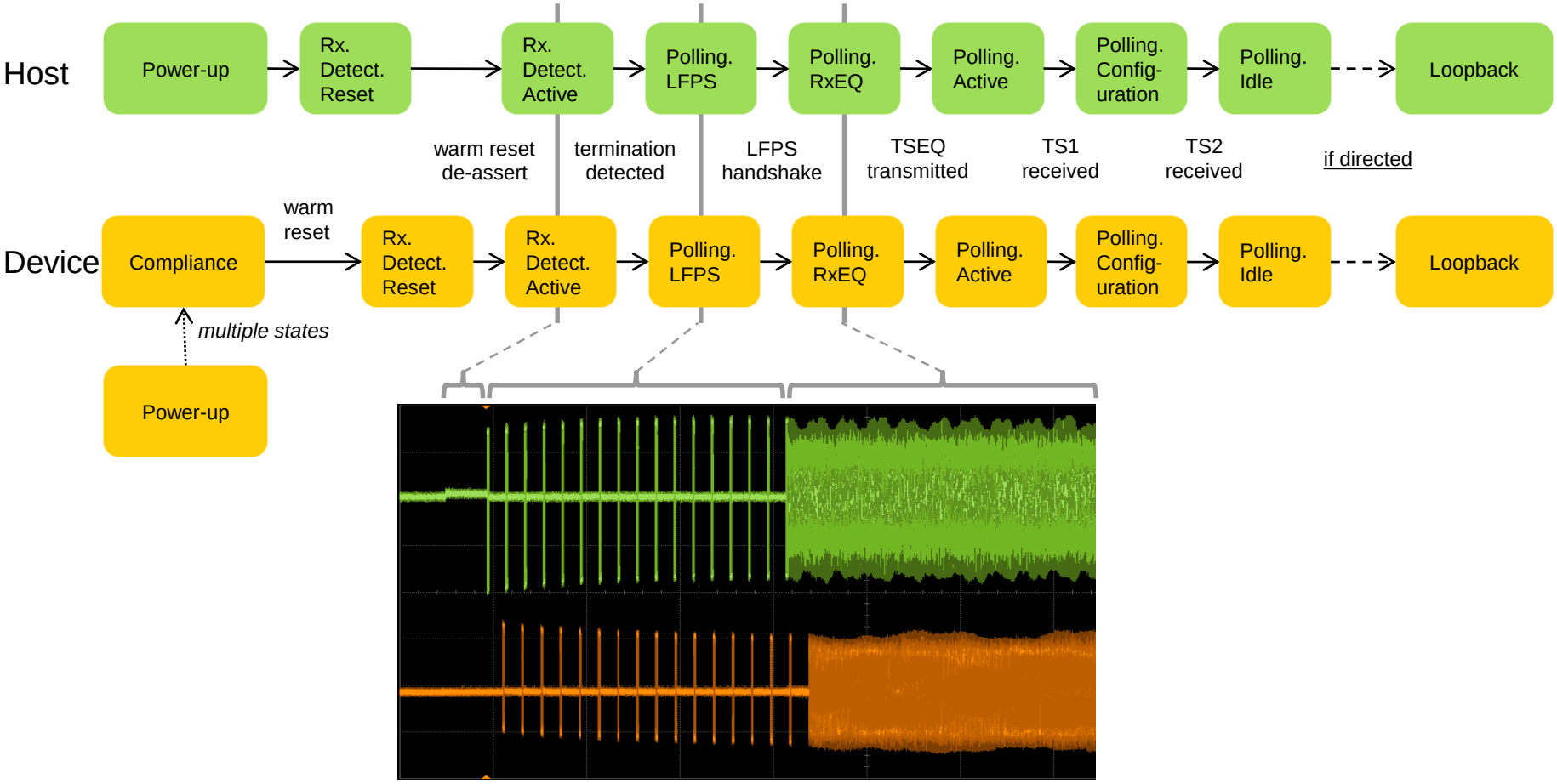
KEYSIGHT TECHNOLOGIES

USB 3.x Comparison

	USB 3.0 (aka USB 3.1 Gen 1 PHY)	USB 3.1 (aka USB 3.1 Gen 2 PHY)
Data rate	5Gb/s ±300ppm (SSC variations not accounted for)	10Gb/s ±300ppm (SSC variations not accounted for)
Coding	• 8b/10b • scrambler: G(X) = $X^{16} + X^5 + X^4 + X^3 + 1$ scrambler reset by COM (K28.5) or BRST seed: FFFFh • Symbol lock: K28.5, some implementations might be able to use K28.1or K28.7	• 128b/132b • scrambler: G(X) = $X^{23} + X^{21} + X^{16} + X^8 + X^5 + X^2 + 1$ scrambler reset by SYNC OS seed: 1D BFBCh • Block alignment: SYNC OS + SDS OS and realignment thr ough SKP OS
SKP	K28.1, K28.1	SKP OS with variable number of SKPs
LFPS		Device host capability negotiation is done during Low Frequen cy Periodic Signaling (LFPS) phase using LFPS modulation s chemes
CDR	PLL transfer: • f_{3dB} = 10MHz • $peaking_{max}$ = 2dB HPF transfer: • f_{3dB} = 4.9MHz • peaking ≈ 0dB • damping factor = 0.707	PLL transfer: • f_{3dB} = 15MHz • $peaking_{max}$ = 2dB HPF transfer: • f_{3dB} = 7.5MHz • peaking ≈ 0dB • damping factor = 0.707
SSC	• Modulation rate: 30kHz to 33kHz • Deviation: +0 to -4000(min)/-5000(max) • Max slew rate: 10ms/s	• Modulation rate: 30kHz to 33kHz • Deviation: +0 to -4000(min)/-5000(max) • New df/dt requirement: 1250 (max) ppm/µs instead of max slew rate spec
De-emphasis	Post: -3dB	Pre: 2.2dB Post: -3.1dB

Typical USB 3.0 Link Turn-on Sequence

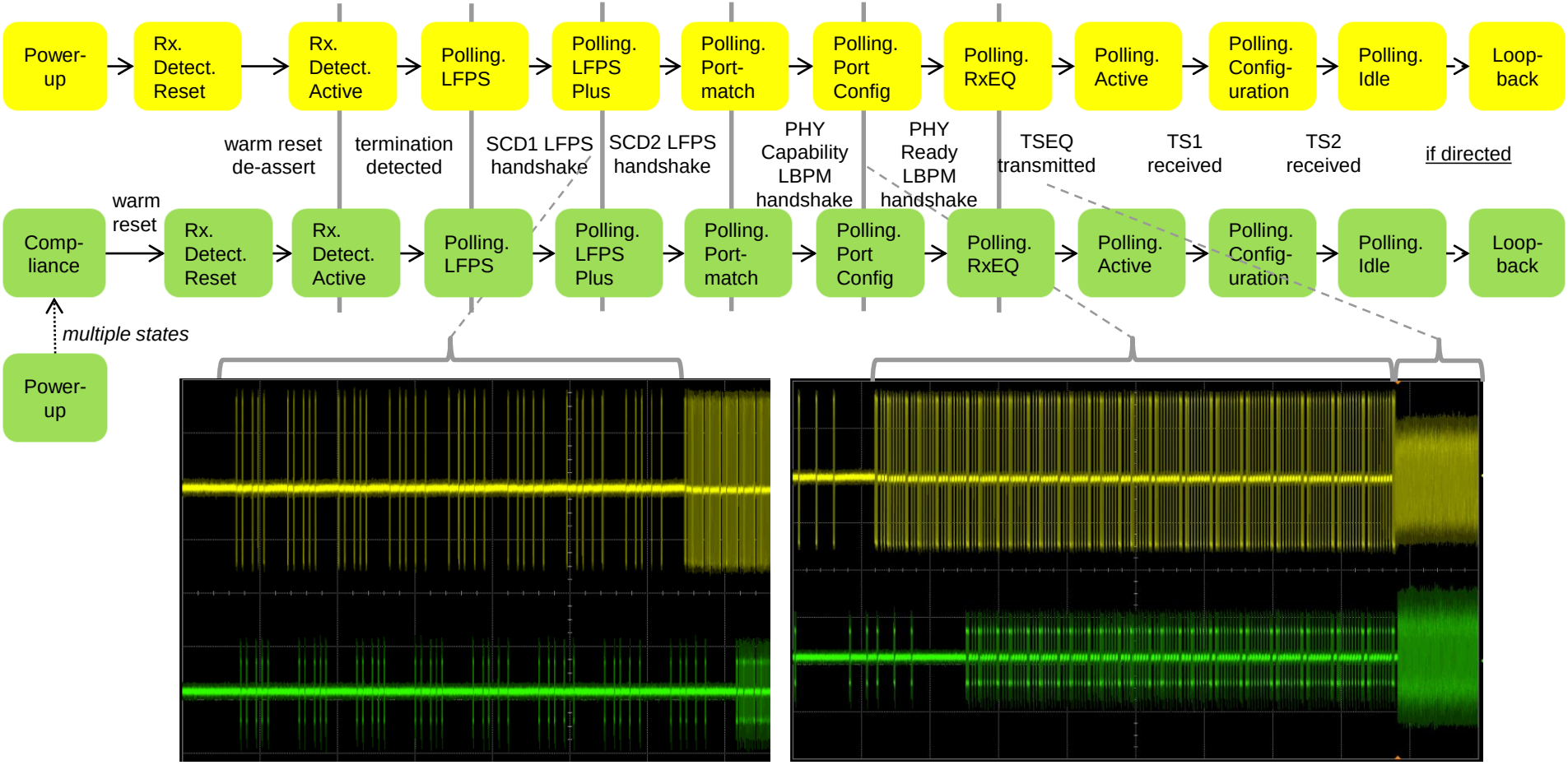
LTSSM states:



J-BERT's sequence trigger can be used to trigger scope captures for each trainings step ➔ in combination with scope's protocol decode very helpful for debugging a trainings sequence

Typical USB 3.1 Link Turn-on Sequence

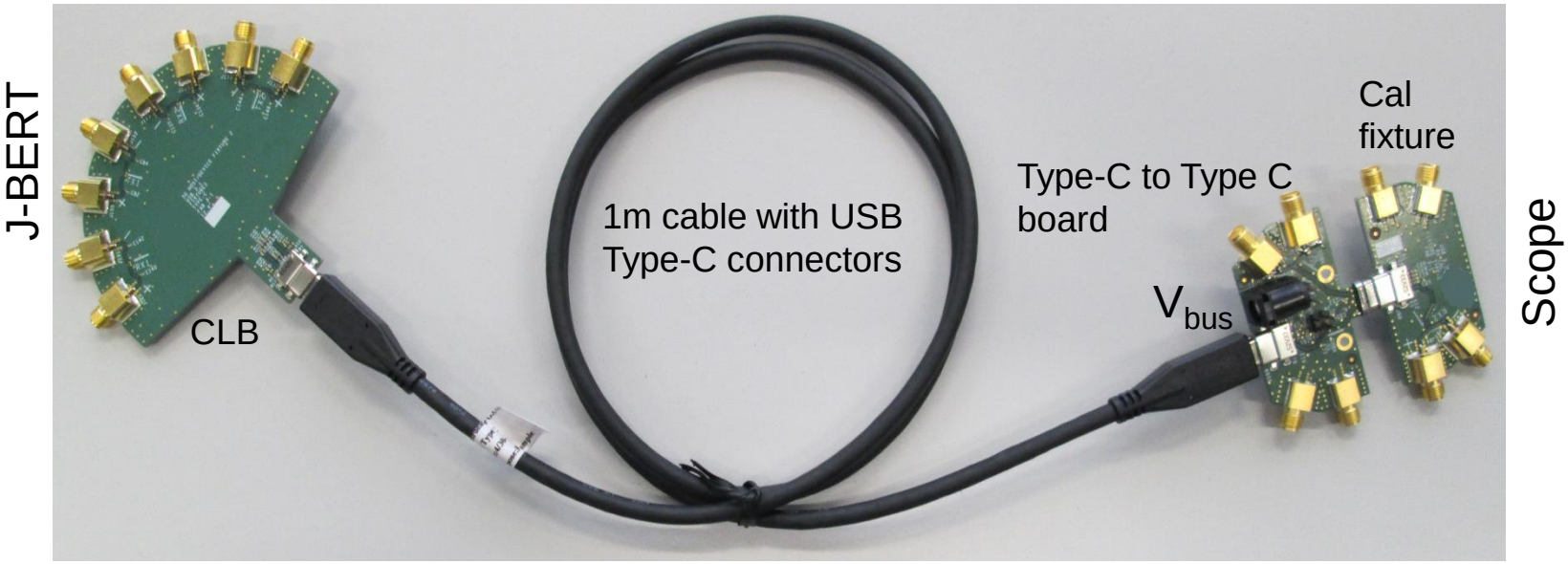
LTSSM states:



J-BERT's sequence trigger can be used to trigger scope captures for each trainings step ➔ very helpful for debugging a trainings sequence

USB 3.0/3.1 5Gb/s RX Test Calibration

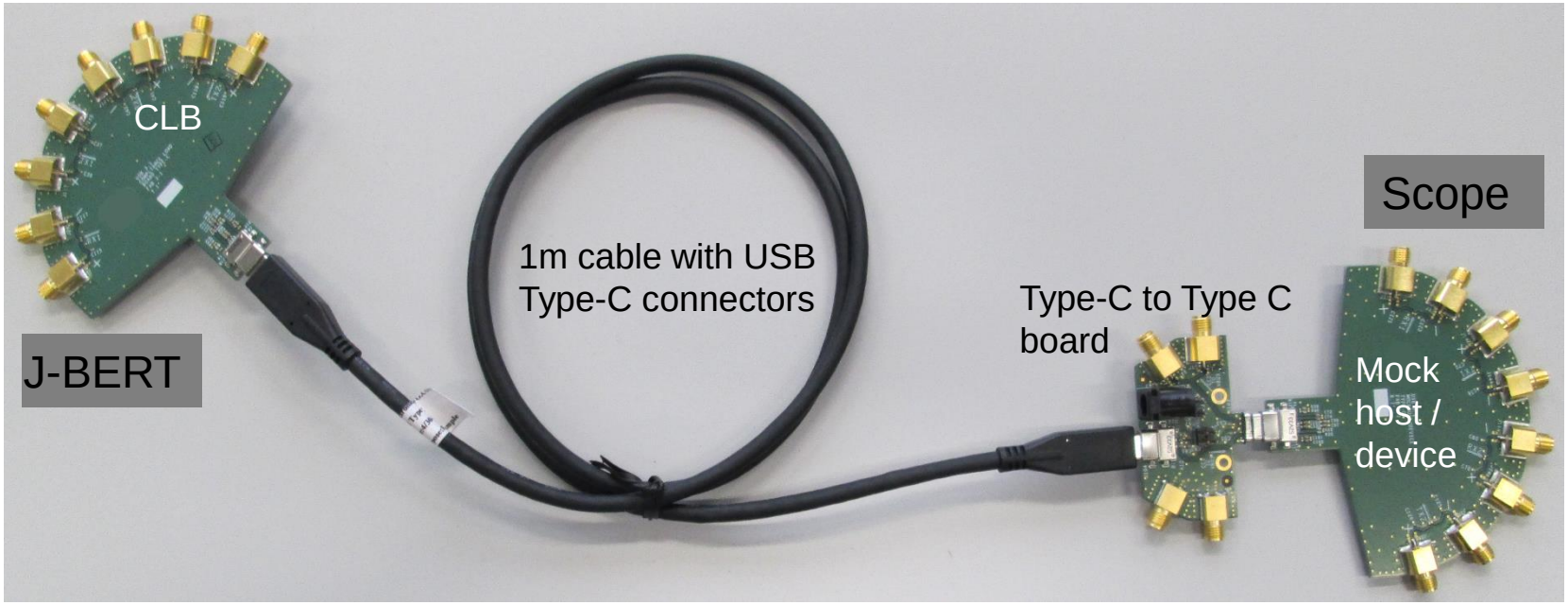
Compliance Test Channel – Type-C Connector



- Same setup for host or device with exception of Type-C to Type-C board:
  - Host RX – breakout for DUT TX to BERT RX channel, no V_{bus} connection
  - Host TX – no breakout, no V_{bus} connection
  - Device RX – breakout for DUT TX to BERT RX, V_{bus} connection
  - Device TX – no breakout, no V_{bus} connection
- Exact trace length of CLB is not defined yet
- 1m cable with USB Type-C connectors

USB 3.1 gen2 10Gb/s

USB 3.1 Type C 23dB Cal Channel



Compliance Load Board (CLB):

- A fixture set contains three CLBs with traces of different lengths to be able to adjust residual ISI

Four versions of Type-C to Type-C board:

- Host RX – breakout for DUT TX to BERT RX channel, no V_{bus} connection
- Host TX – no breakout, no V_{bus} connection
- Device RX – breakout for DUT TX to BERT RX, V_{bus} connection
- Device TX – no breakout, no V_{bus} connection

Mock-Up fixture:

- Simulates reference device/host loss. Used for calibration only.

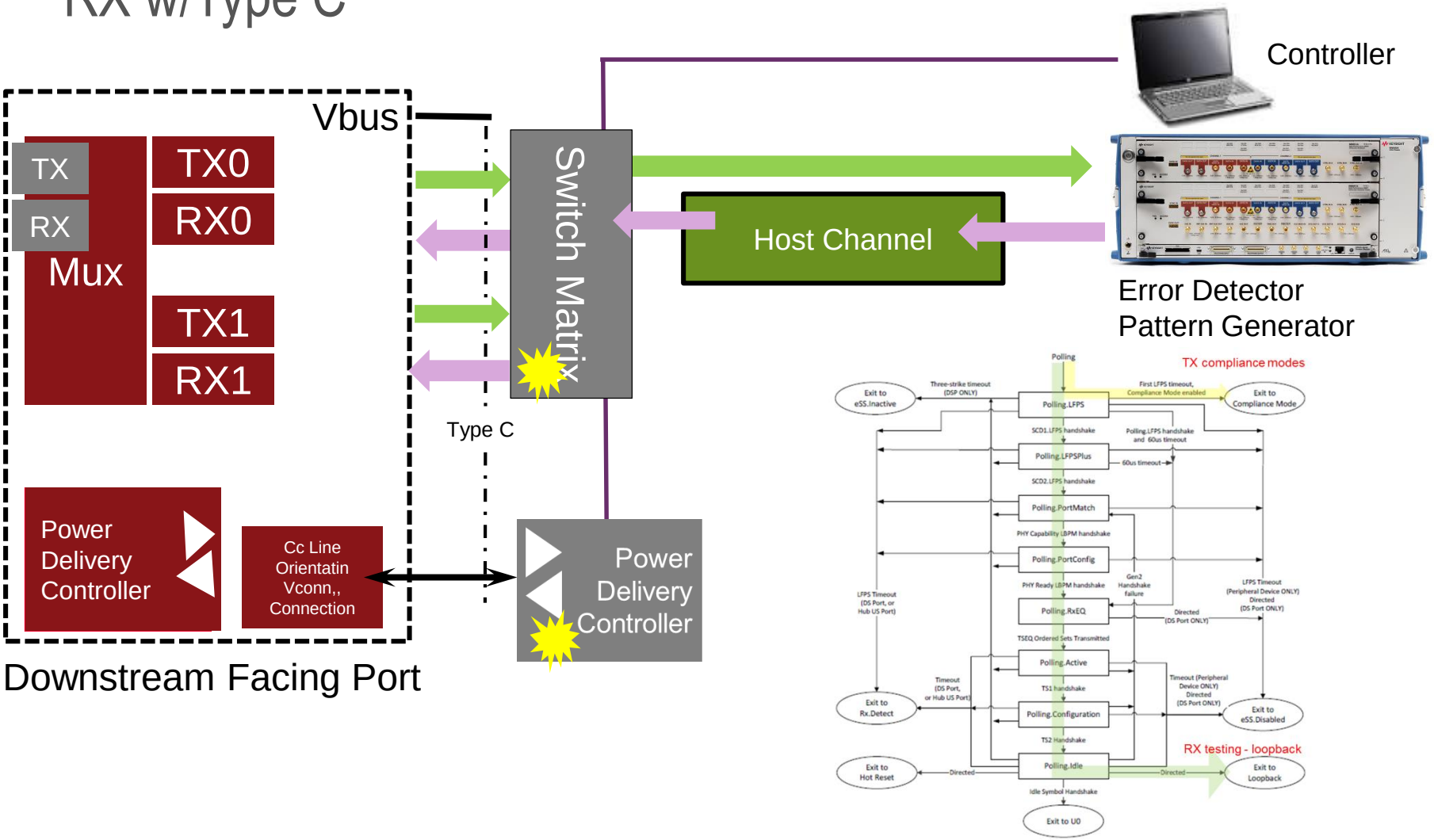
USB 3.1 gen2 10Gb/s

USB 3.1 Type C 14.5dB Test Channel

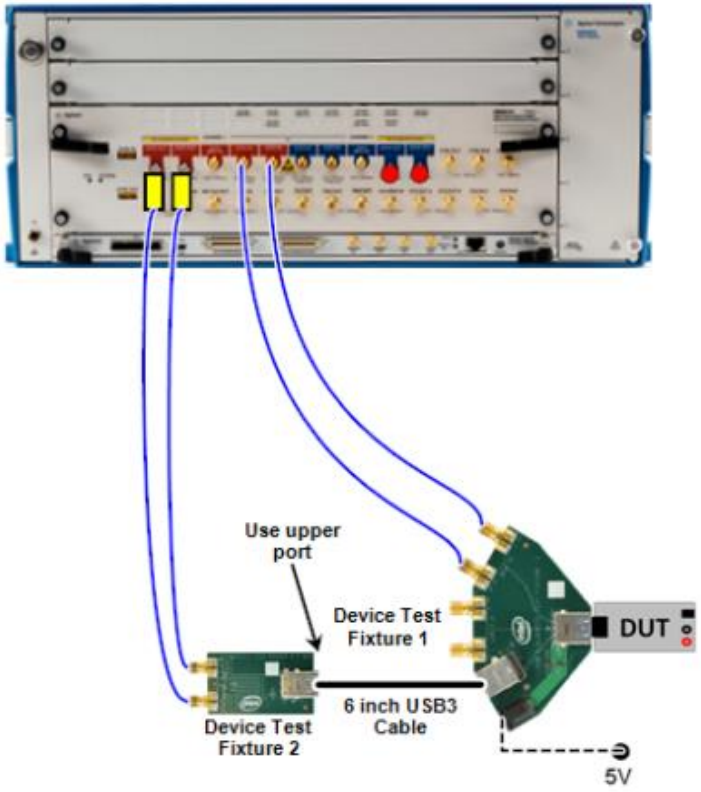
Unlike for USB 3.0/3.1 gen1 5G RX testing USB 3.1 gen2 10G RX compliance testing requires to test each test frequency for 10^{12} bits.

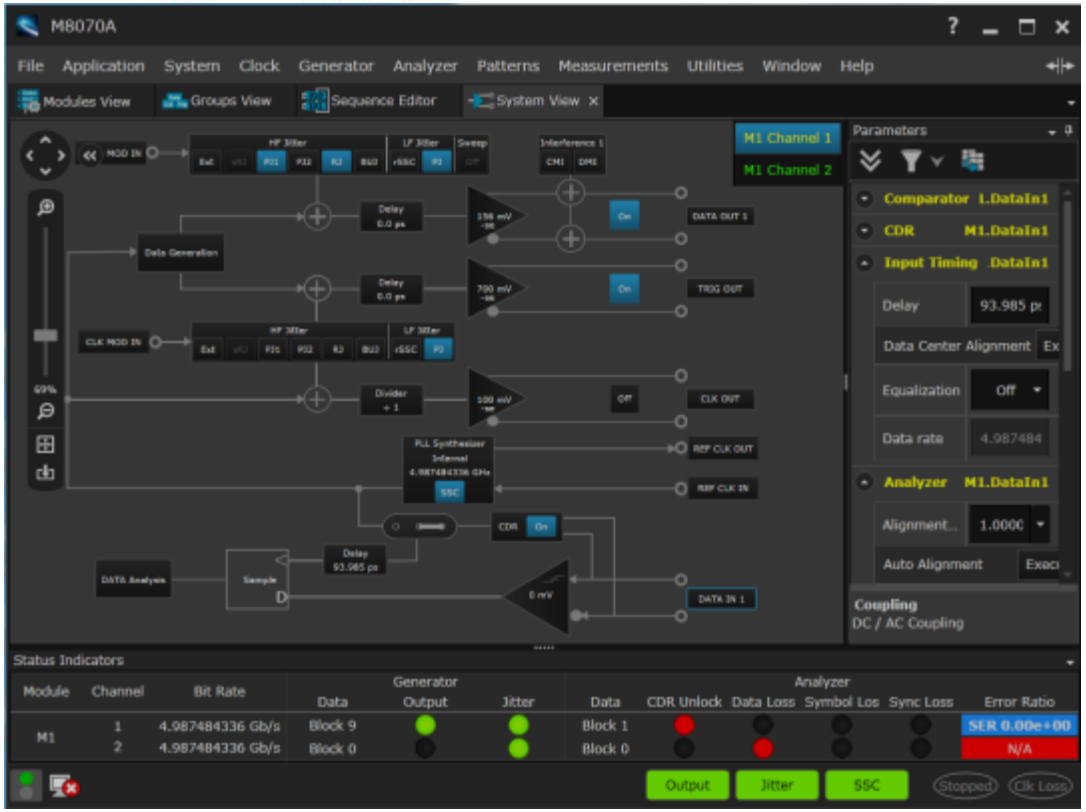
Testing USB 3.1

RX w/Type C



USB 3.1 Gen1/Gen2 Receiver Test Setup





Key capabilities:

- Analysis of coded & retimed data
- Support of **8b/10b and 128b/132b HW** coding and decoding as well as HW scrambling
- Generates calibrated stress conditions for RX test (SSC, SJ, RJ, De-emphasis, ISI)
- **Emulate LFPS 3-level signals** with built-in electrical idle for loopback training and via channel
- **Integrated Link Training, Tx Eq, Noise Impairment, Variable ISI, Receiver Equalizer/Eye Opener**

KEYSIGHT TECHNOLOGIES

N5990A Test Automation for USB

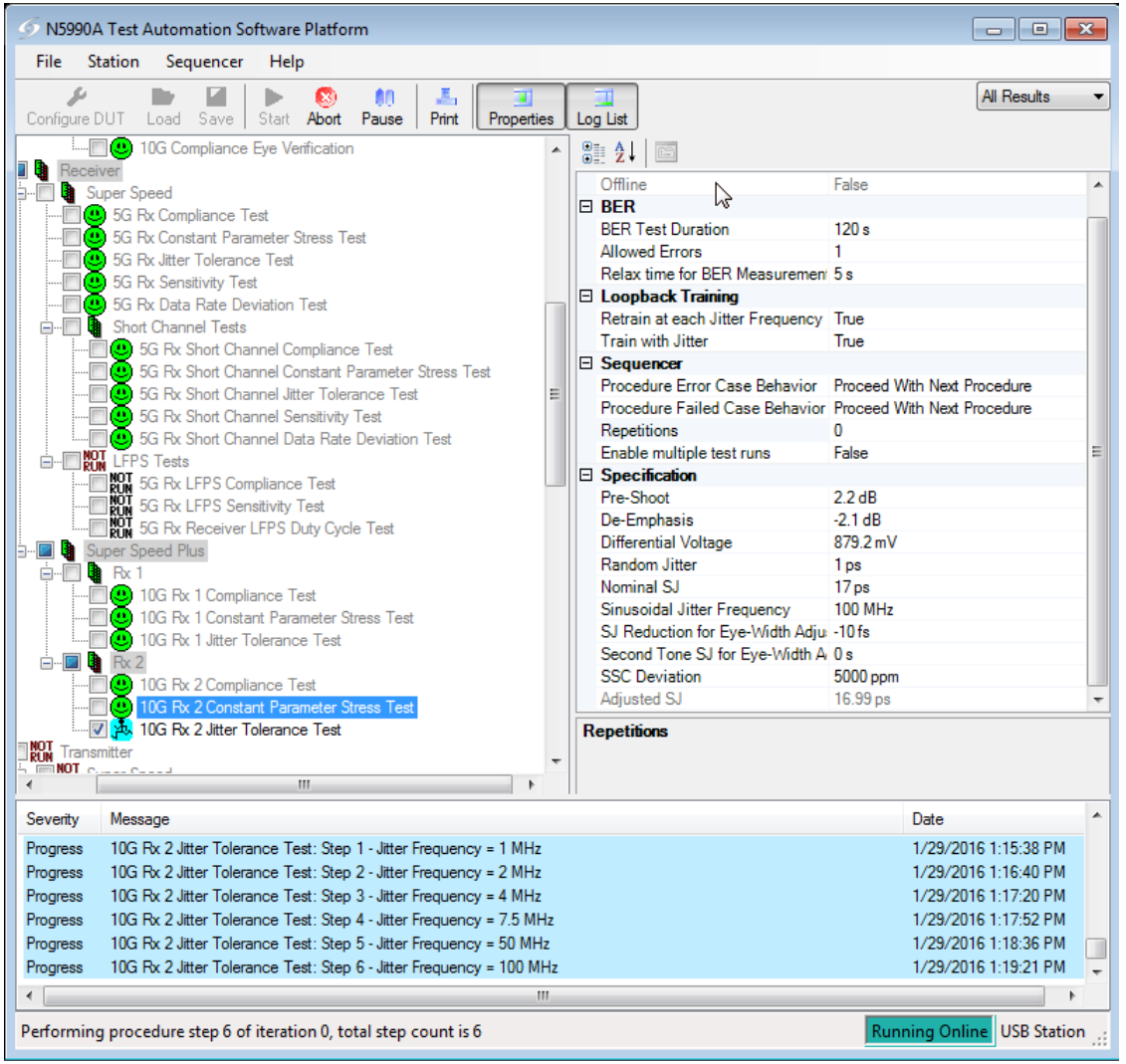
Test Overview

Compliance Tests:

- 5G RX Compliance long channel
- 5G RX Compliance short channel
- 5G RX Compliance LFPS
- 10G RX Compliance position 1
- 10G RX Compliance position 2

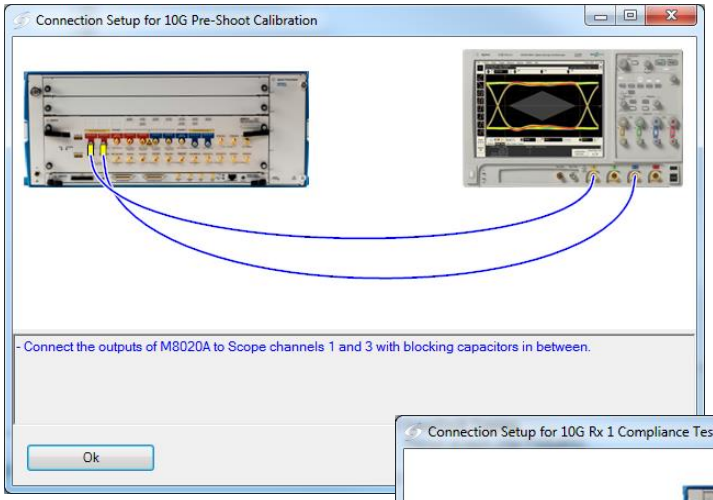
Characterization Tests:

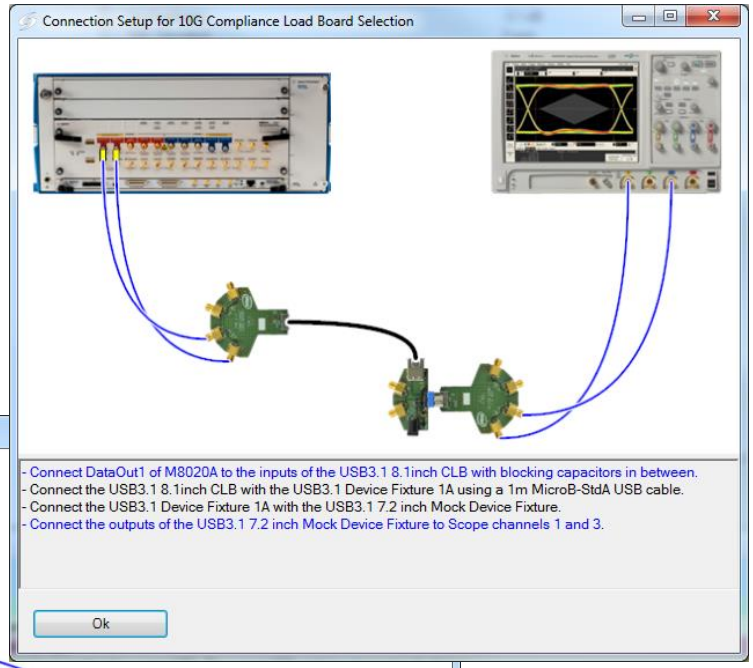
- RX constant parameter
- RX jitter tolerance (SJ margin)
- RX and LFPS sensitivity
- RX data rate deviation
- LFPS Duty Cycle

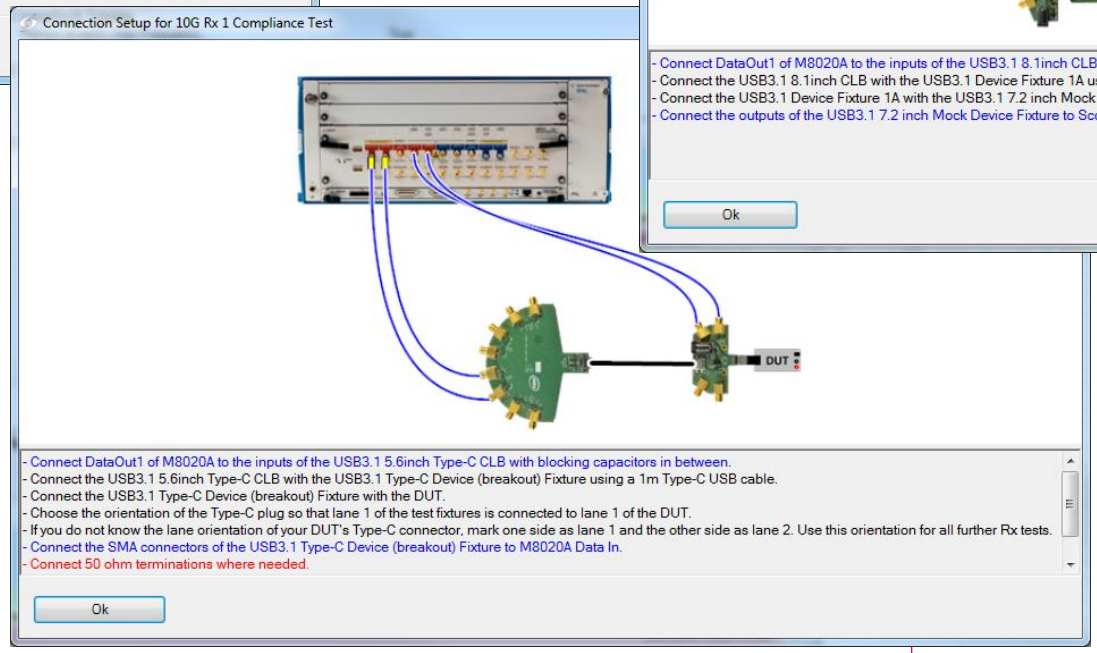


N5990A Test Automation for USB 3.0/3.1

Ease of Use







The N5990A Test Automation for USB 3.0/3.1 guides users through every setup changes with connection diagrams and detailed descriptions

Receiver Jitter Tolerance curve

Gen1 vs Gen2

- Rx Jtol RJ & Tx EQ updated by ECN
- Gen 2 define 7 SJ points in spec.
- Gen 1 define 5 SJ points in Spec, but 8 points in CTS

Symbol	Parameter	Gen 1	Gen 2	Units
f1	Tolerance corner	4.9	7.5	MHz
J_{Rj}	Random Jitter	0.0121	0.0100	UI rms
$J_{Rj\_p\text{-}p}$	Random Jitter peak- peak at 10^{-12}	0.17	0.141	UI p-p
J_{Pj_500kHZ}	Sinusoidal Jitter	2	2.56	UI p-p
J_{Pj_1Mhz}		1	1.28	UI p-p
J_{Pj_2MHz}		0.5	0.64	UI p-p
J_{Pj_4MHz}		N/A	0.32	UI p-p
J_{Pj_f1}		0.2	0.17	UI p-p
J_{Pj_50MHz}		0.2	0.17	UI p-p
J_{Pj_100MHz}		N/A	0.17	UI p-p
V_full_swing	Transition bit differential voltage swing	0.75	TBD	V p-p
V_EQ_level	Non transition bit voltage (equalization)	-3	Pre=2.2 Post= -3.1	dB

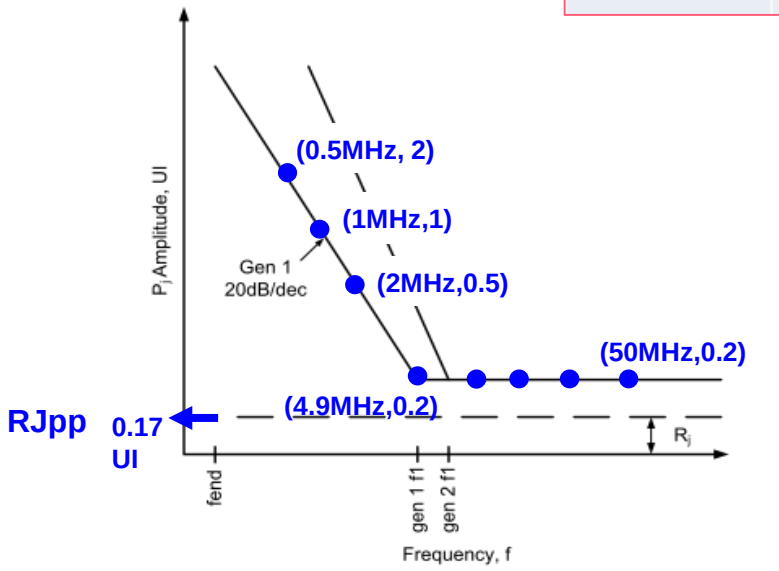


Figure 6-28. Jitter Tolerance Curve

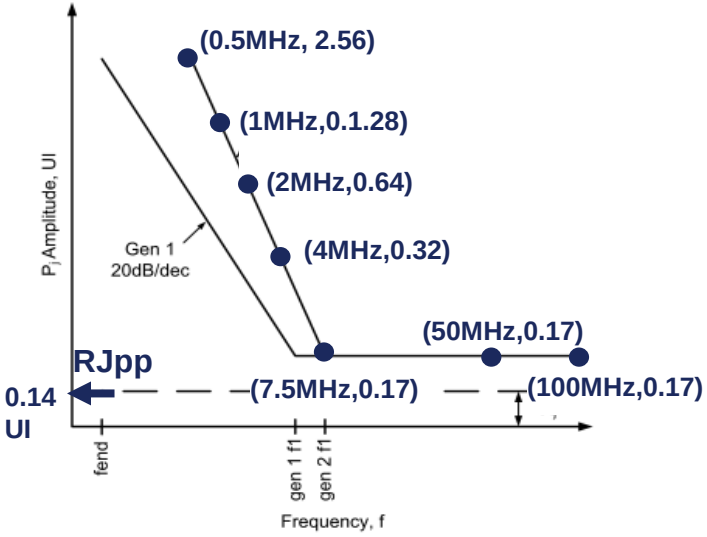
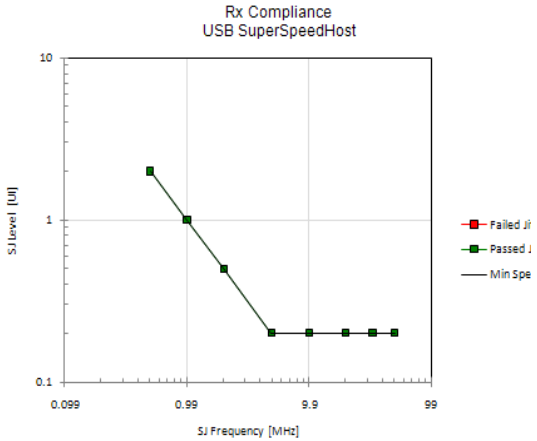
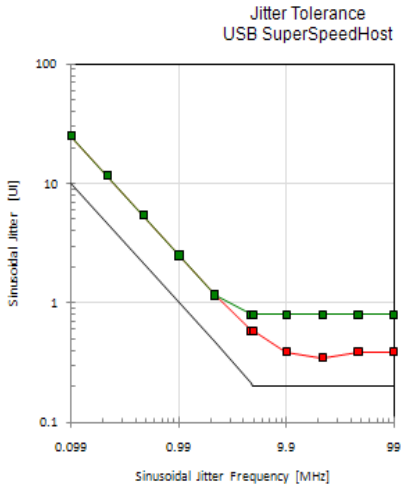


Figure 6-28. Jitter Tolerance Curve

SuperSpeed Receiver Tests
Rx Compliance and Jitter Tolerance Testing

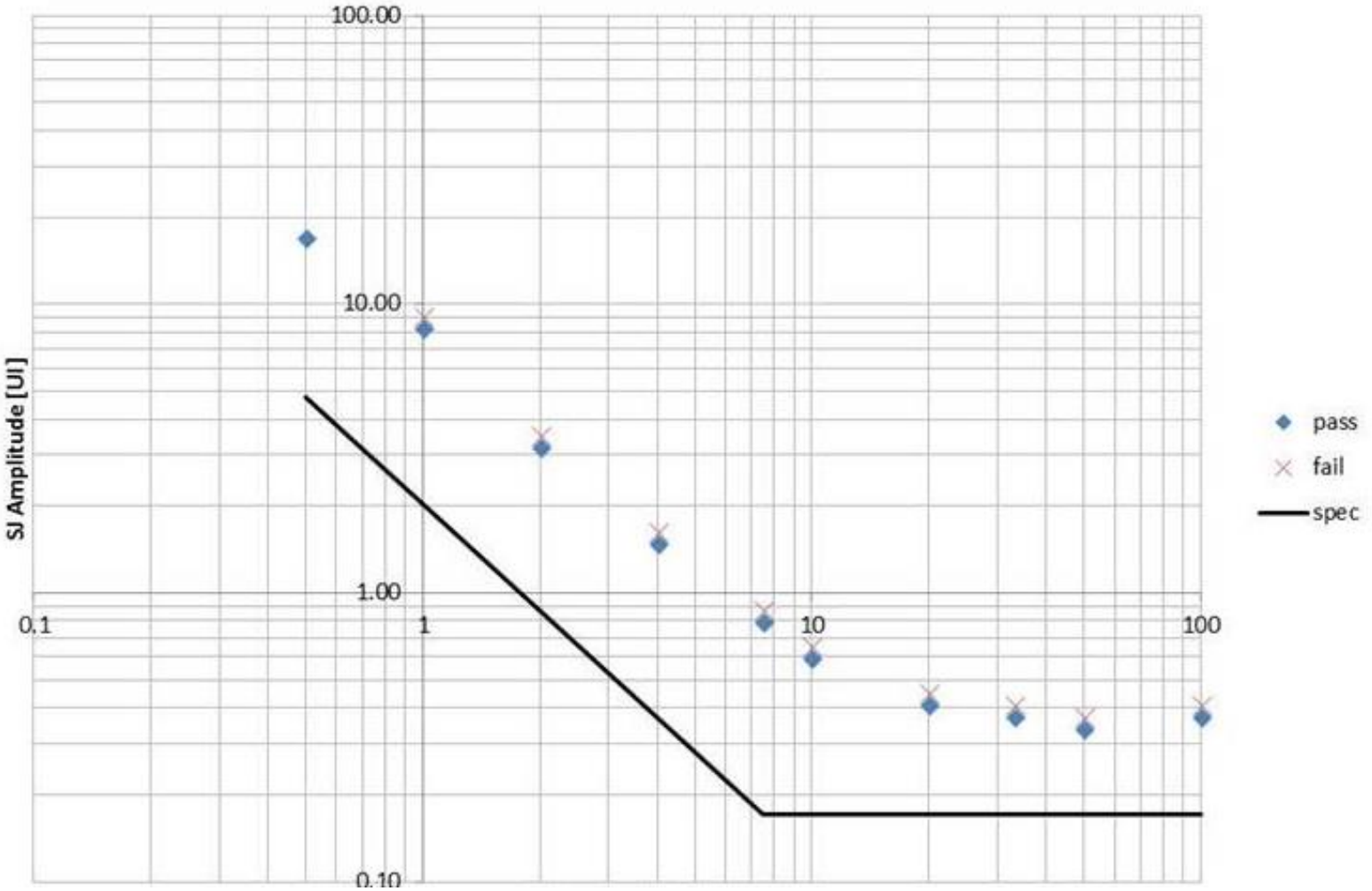
- Automated instrument control for:
  - Setup calibration
  - Compliance test
  - Characterization test
  - Support for debugging
- Operator guidance
- Sophisticated test reports
- Controls J-BERT, Oscilloscope.
- Supports full product characterization including transmitter measurements



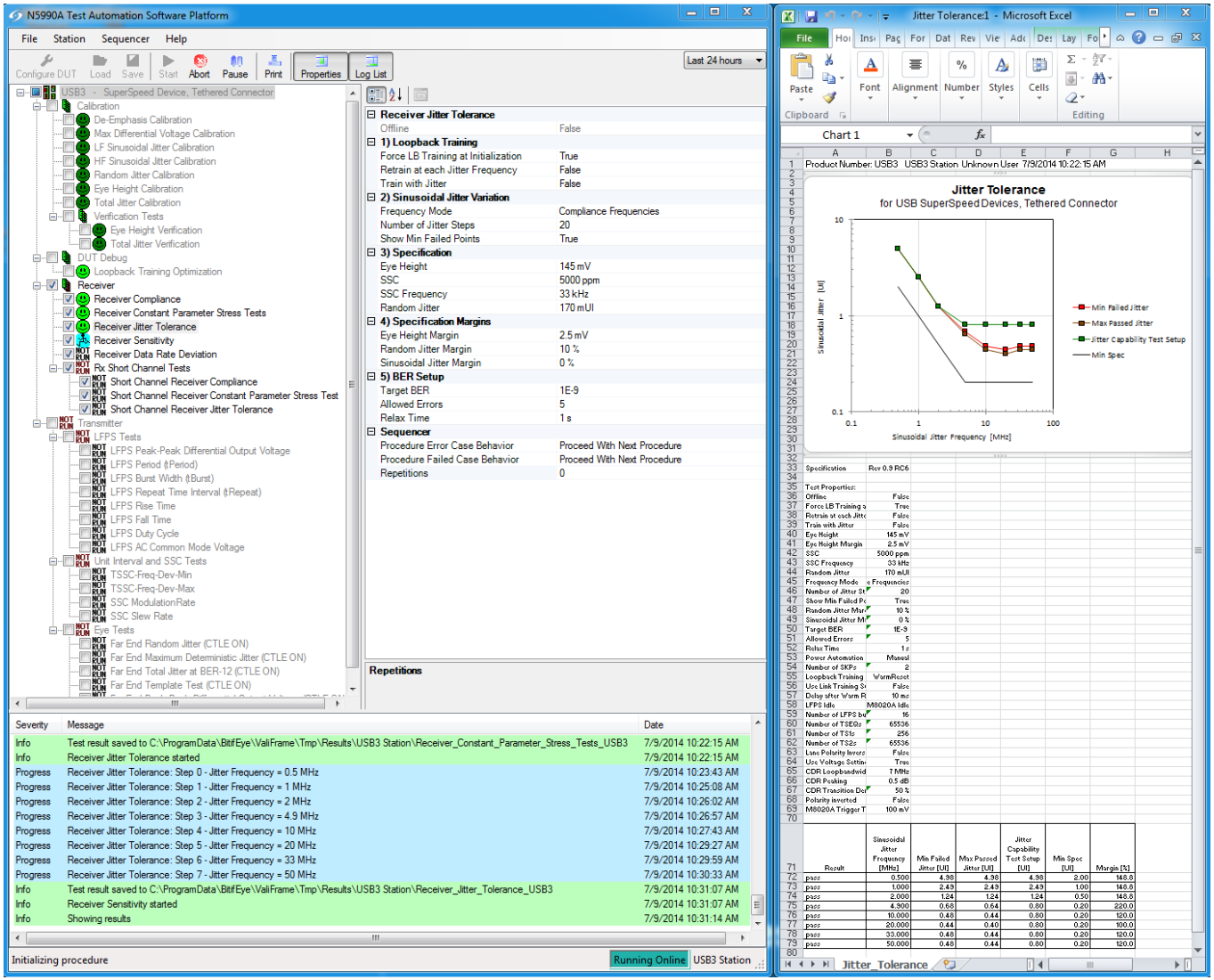


Result	SJ Frequency [MHz]	Failed Jitter [UI]	Passed Jitter [UI]	Min Spec [UI]	Symbol Errors
pass	0.500		2.00	2.000	0
pass	1.000		1.00	1.000	0
pass	2.000		0.50	0.500	0
pass	4.900		0.20	0.200	0
pass	10.000		0.20	0.200	0
pass	20.000		0.20	0.200	0
pass	33.000		0.20	0.200	0
pass	50.000		0.20	0.200	0

JTOL Margining Test Results

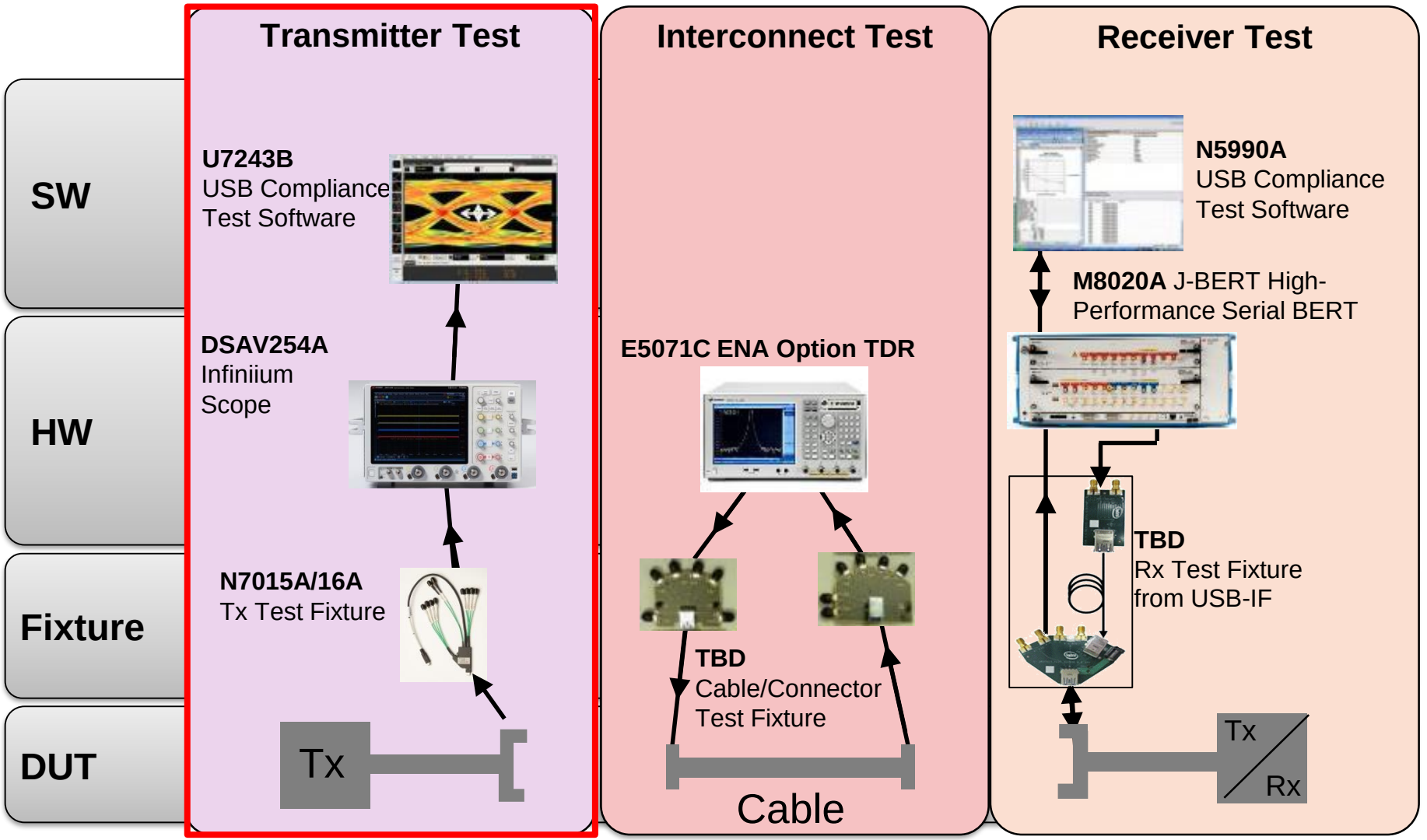


Receiver Characterization Example



- Automated instrument control for:
  - Setup calibration
  - Compliance test
  - Characterization test
  - Support for debugging
- Operator guidance
- Sophisticated test reports
- Controls J-BERT, Oscilloscope.
- Supports full product characterization including transmitter measurements

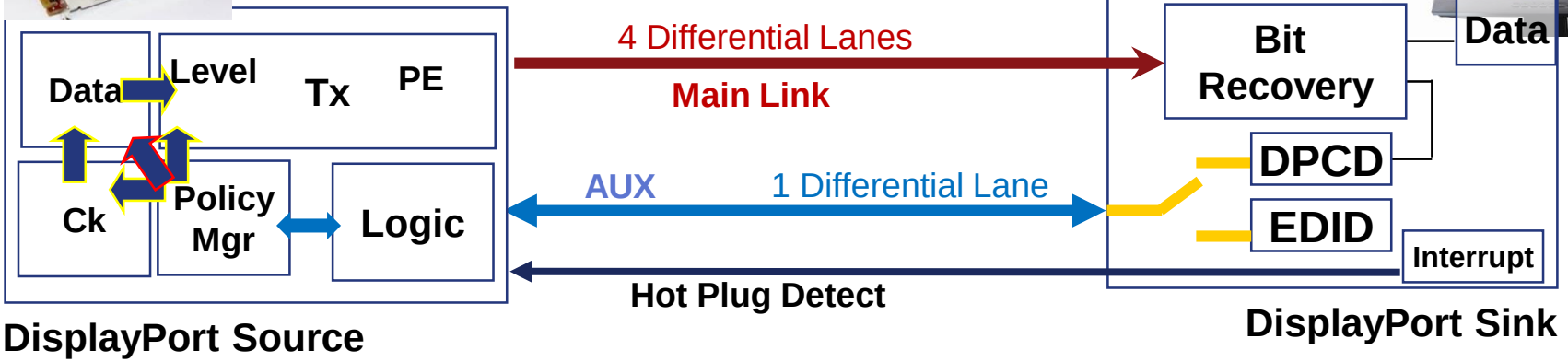
Keysight USB 3.1 Total Test Solution



USB Type-C Interface and DP Alt Mode Overview

KEYSIGHT TECHNOLOGIES

Review of DisplayPort Interface



Main Link

Up to 4 differential lanes: 4 possible bit rates

TX:

- 4 possible level settings
- 4 possible pre-emphasis settings
- Spread Spectrum Clocking (optional)
- Dual Mode optional

RX:

- Receiver individual clock recovery
- Receiver Tolerance curve specified.
- Receiver Sensitivity = 50mV

AUX Channel

Phy Layer

- Bit rate at 1Mbs
- Manchester II encoded

Purpose

- Link Management
- Test Mode control

USB Type C Port Function

Alternate Mode: DisplayPort

Downstream Facing Port (Video Output)

DP

STD Mux

Port Mux

USB 3.1

Supply

Provider/ Consumer

Power (V_{BUS}) Control

GND GND
TX2 TX3
TX2 TX3
V_{BUS} V_{BUS}
SBU2 CC1
D- D+
D+ D-
V_{CONN} CC2 SBU1
V_{BUS} V_{BUS}
TX1 TX0
TX1 TX0
GND GND

Cable

CC

GND GND
RX0 RX1
RX0 RX1
V_{BUS} V_{BUS}
SBU2 CC1
D- D+
D+ D-
CC2
V_{BUS} V_{BUS}
RX3 RX2
RX3 RX2
GND GND

Provider/ Consumer

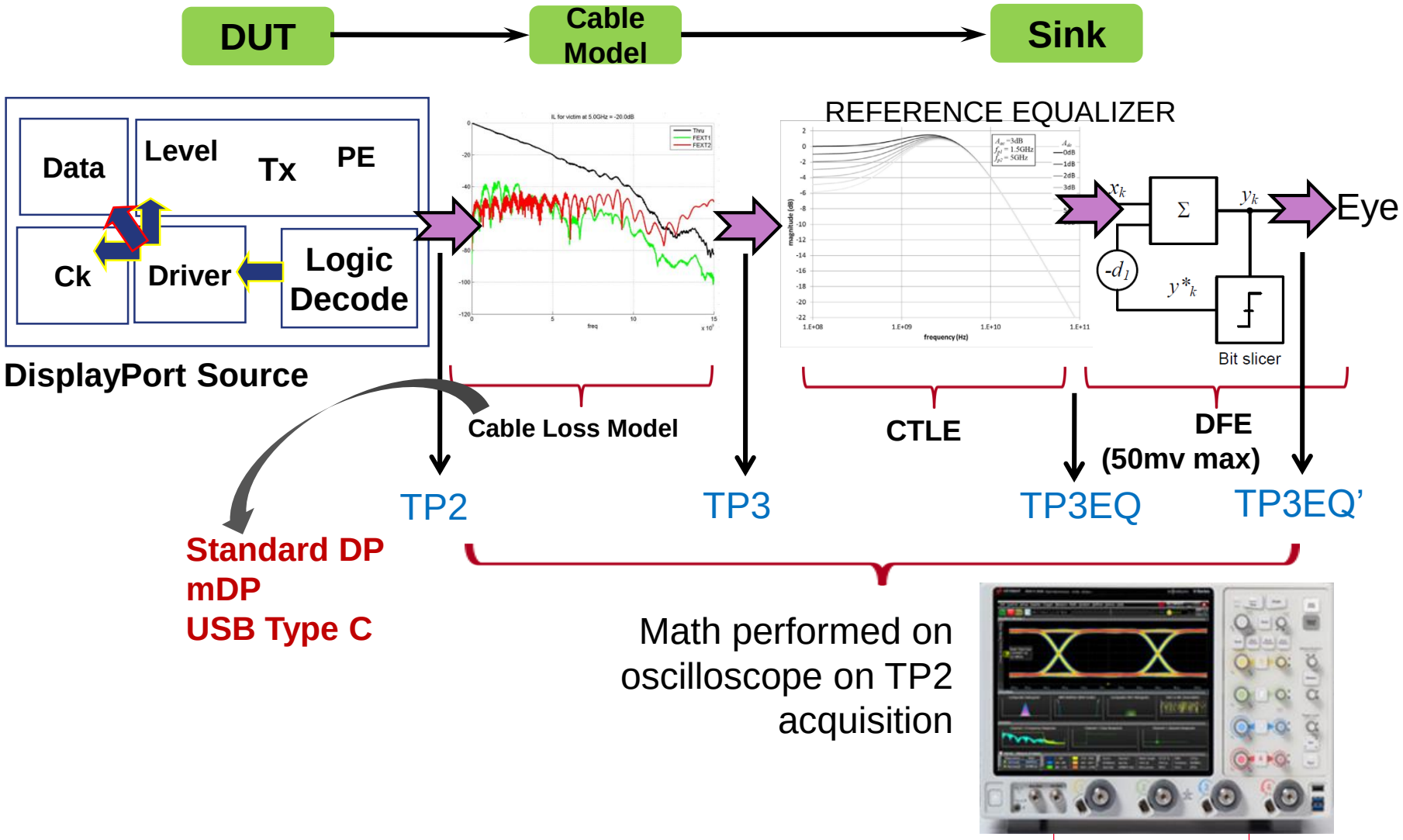
Supply

Power (V_{BUS}) Control

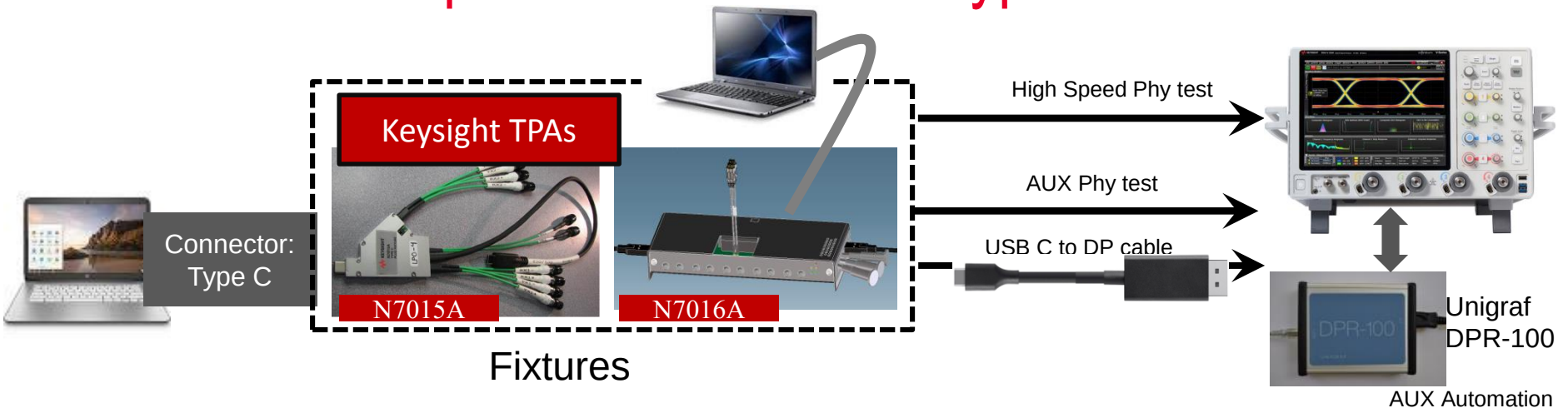
Port Mux

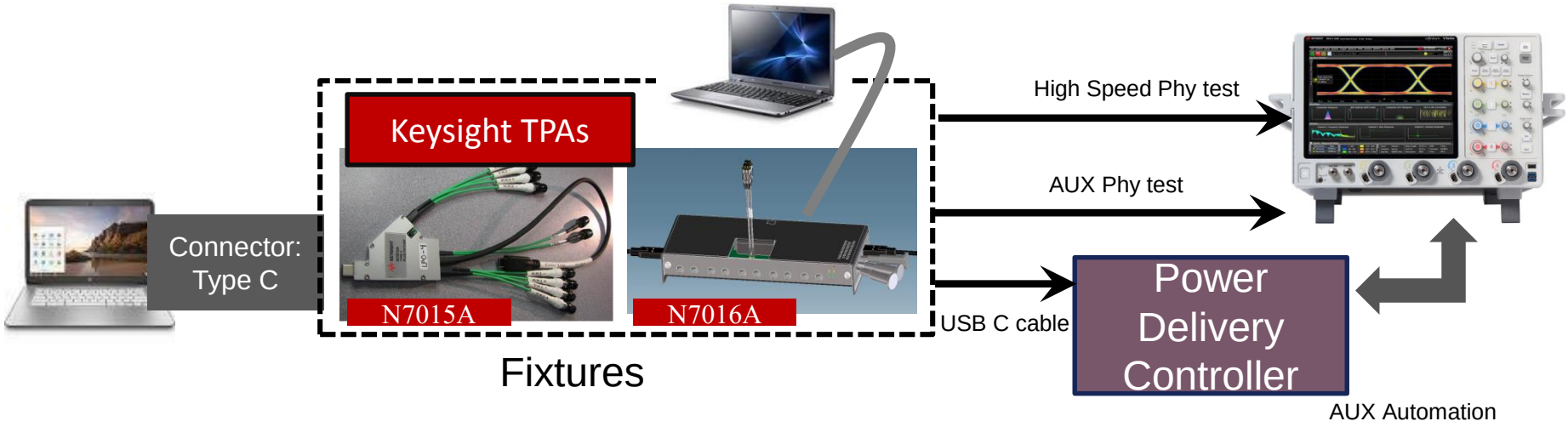
Upstream Facing Port (Display)

DP Transmitter Testing: Whole Channel



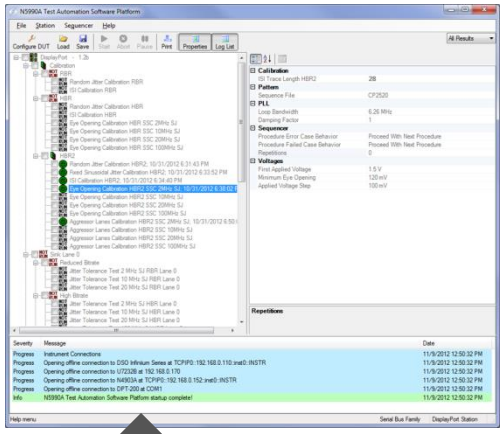
TX Test Setup for DP over USB Type-C



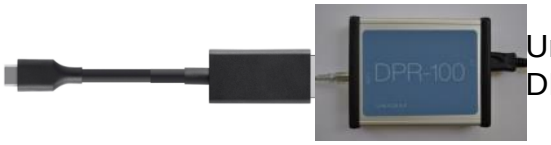


RX Test Setup for DP over USB Type-C

InterSymbol Interference



High Speed Phy test



Unigraf DPT-200

AUX Automation

USB C to DP cable

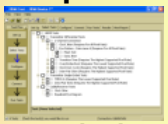
Keysight DisplayPort 1.3 Solutions and Solution Elements

Source Test Solution

Computer Motherboards, ICs, Graphic Cards

DSO V series Infiniium Real Time Oscilloscopes

Unigraf DPR-100 For automation



U7232D DisplayPort Compliance Test SW

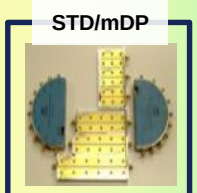
Wilder TPA

N7015A TPA

Media Testing

Cables, PC Boards, Connectors

E5071C VNA



BIT-DP-CBL-0002

Luxshare Rec

Sink Test Solution

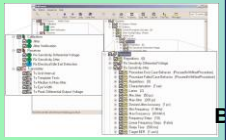
PC Monitors

Artek CLE1000

M8020A JBERT

N4915A-006 DP ISI Generation

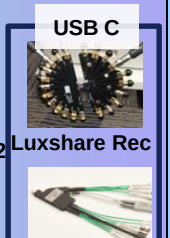
Unigraf DPT-200 for Automation



N5990A Rx Compliance Test SW

BIT-DP-RTF-0002

Wilder TPA



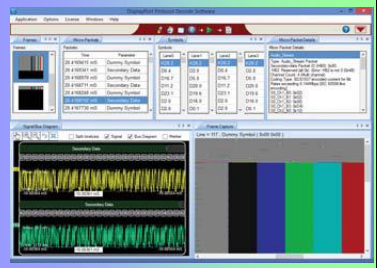
Luxshare Rec

N7015A TPA

Link Layer & General Solutions

Protocol Debug solution

Granite River Labs GRL-DP-DEC

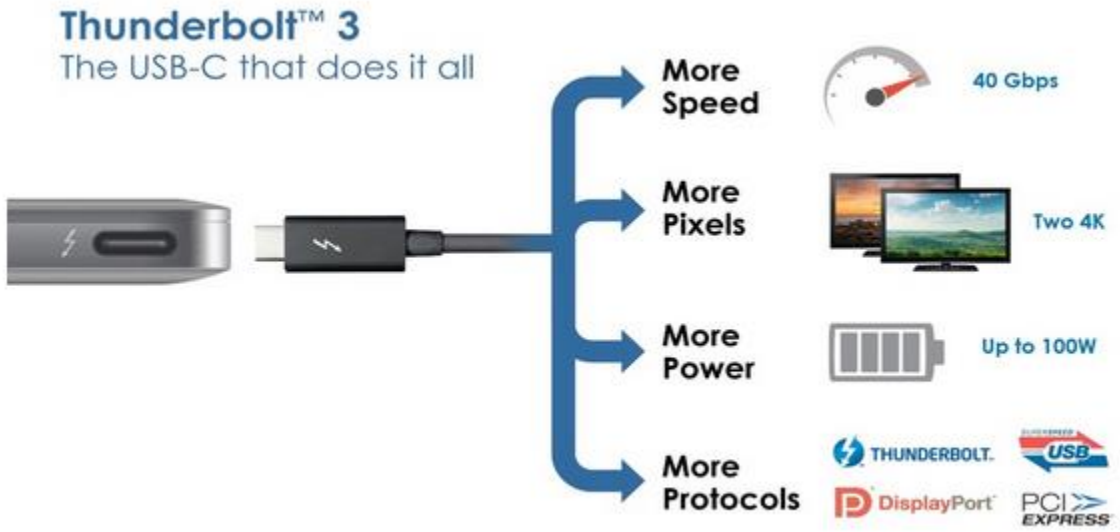


USB Type-C Interface and TBT Alt Mode Overview

KEYSIGHT TECHNOLOGIES

Thunderbolt 3 Overview

- Announced in Q2 2015
- Uses the Type-C connector
- Channel aggregation: two independent 20Gbps links into one logical 40Gbps link
- Supports other standards through ALT mode



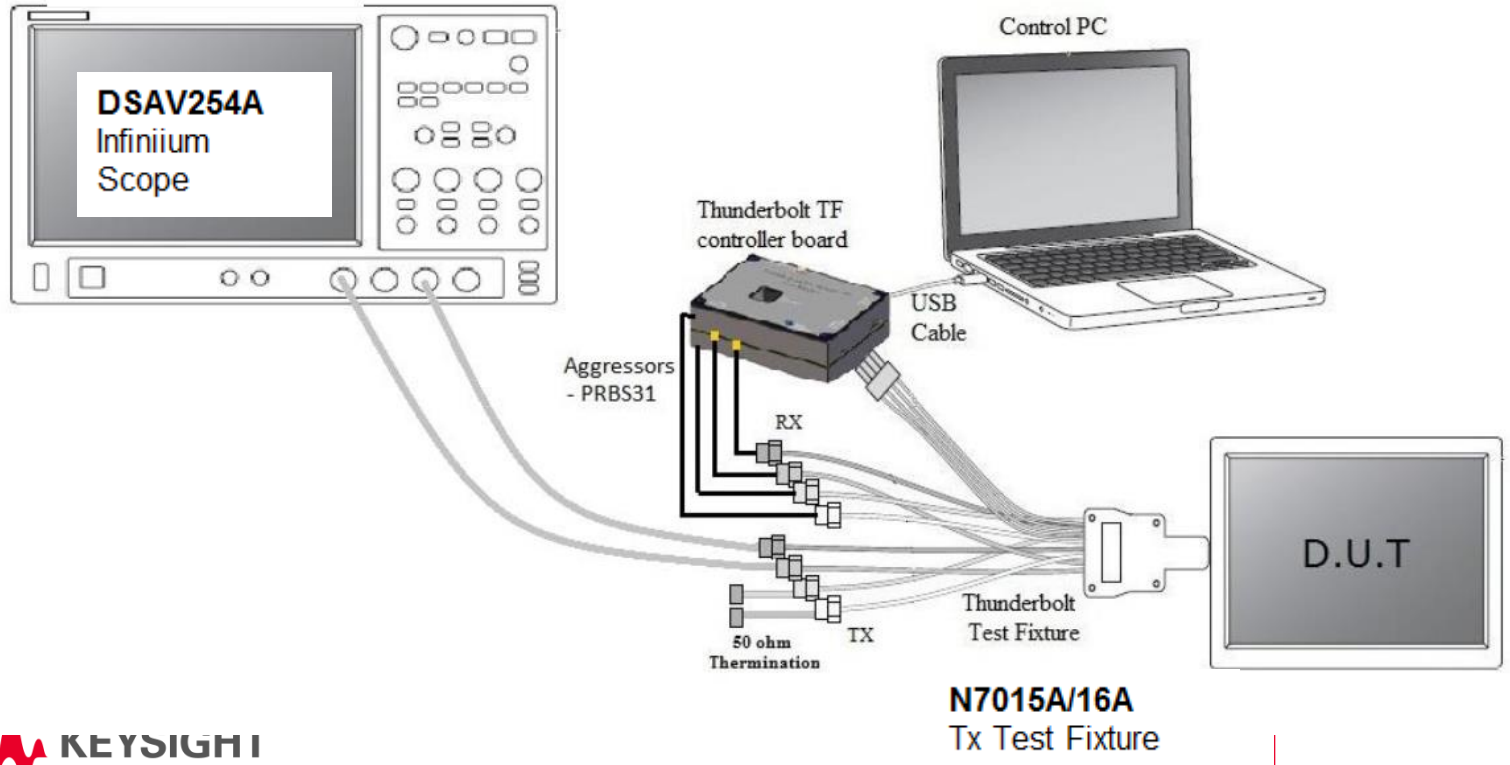
Testing Methodology

- Spec is at v0.7.
- CTS not yet released.
- Testing approach will be similar to Thunderbolt 2
  - Tx, Rx, and Return Loss
- Today, customers with Thunderbolt DUTs need to work with their Inte l PAE to meet the design guidelines and send their DUTs to Intel for t esting.
- Keysight can help with pre-compliance testing

- Tx testing
  - Initial analysis is that 33GHz minimum BW is required for compli ance testing.
  - Silicon characterization will need more BW since the 20/80 riseti me can be 10ps.

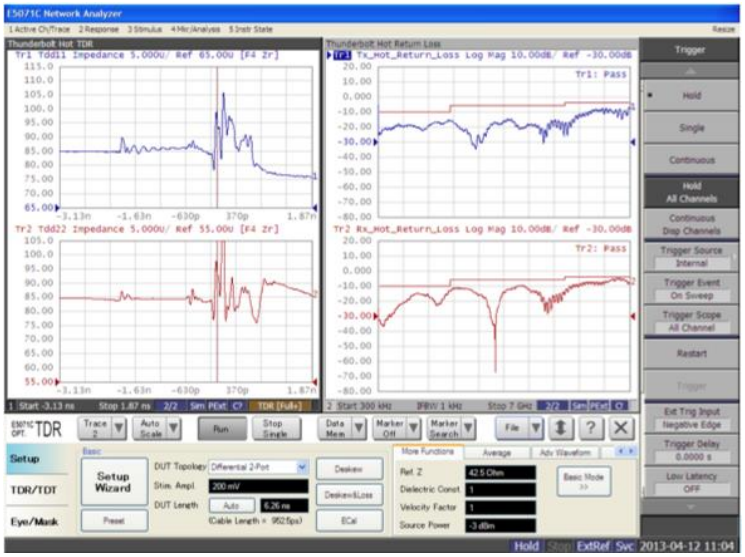
Thunderbolt 3 Transmitter Test Setup

- 25GHz BW required for compliance testing, more if closer to the silicon
- Thunderbolt-specific SW (Imaginarium, TenLira, TCL, scripts)
- Crosstalk generator
- Type-C test fixture
- UI, SSC, Rise/Fall, Jitter, Eye Diagram Near End/Far End
- New Preset testing and optimization for 10.3G and 20.6G



Thunderbolt 3 Return Loss Test

- DUT output PRBS31 on all lanes with SSC turned on
- Setup the Network Analyzer with automated measurements specific to Thunderbolt 3



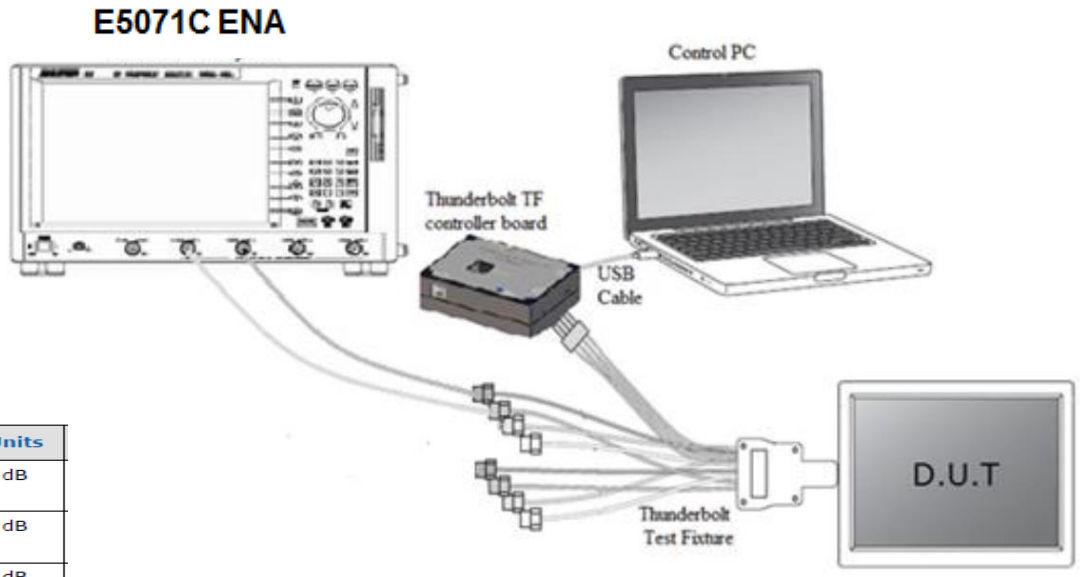
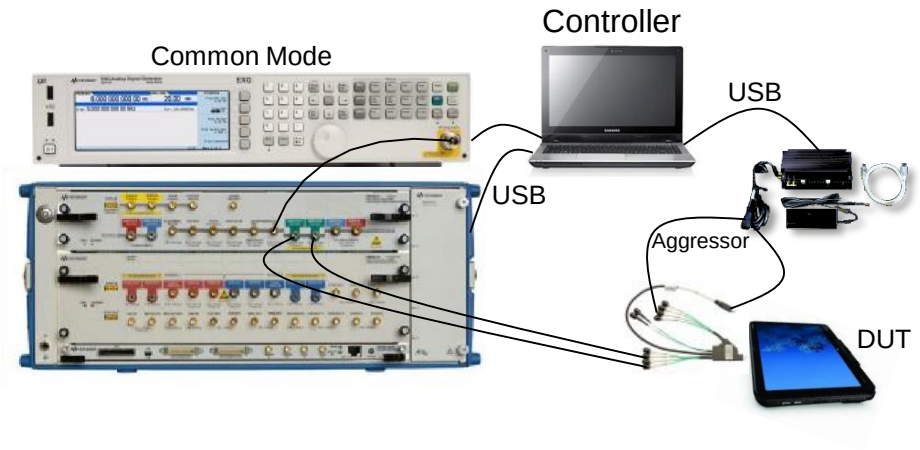
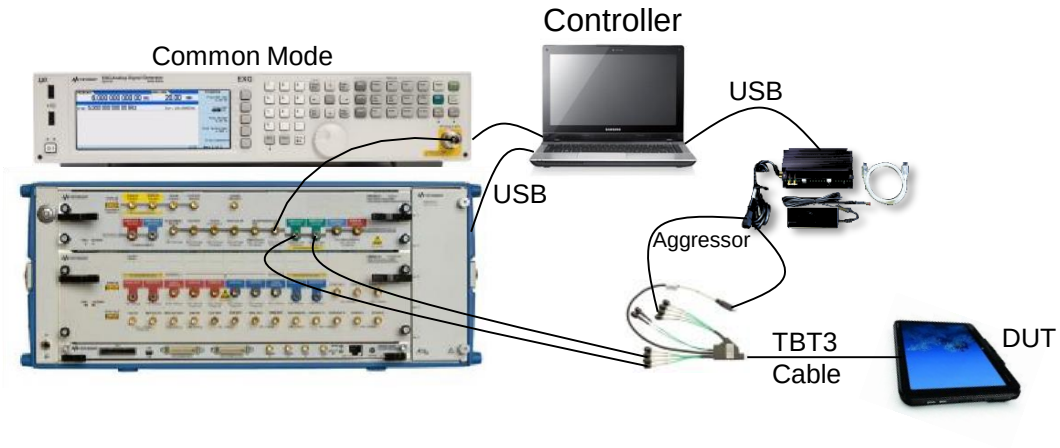


Table 4-6. Host/Device Transmitter Specifications at TP1

Symbol	Description	Min	Max	Units
RL_LF	Return loss, 0.05 – 2 GHz	10		dB
RL_MF	Return loss, 2 – 5.2 GHz	6		dB
RL_HF	Return loss, 5.2 – 7 GHz	4		dB

Test Setup: Case 1 and Case 2 Execution





Thunderbolt 3 – Total Solution