STM32

32-bit ARM® Cortex™ MCUs

STM32F030 Series

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BSI SEMICONDUCTOR (KOREA) Co., Ltd.

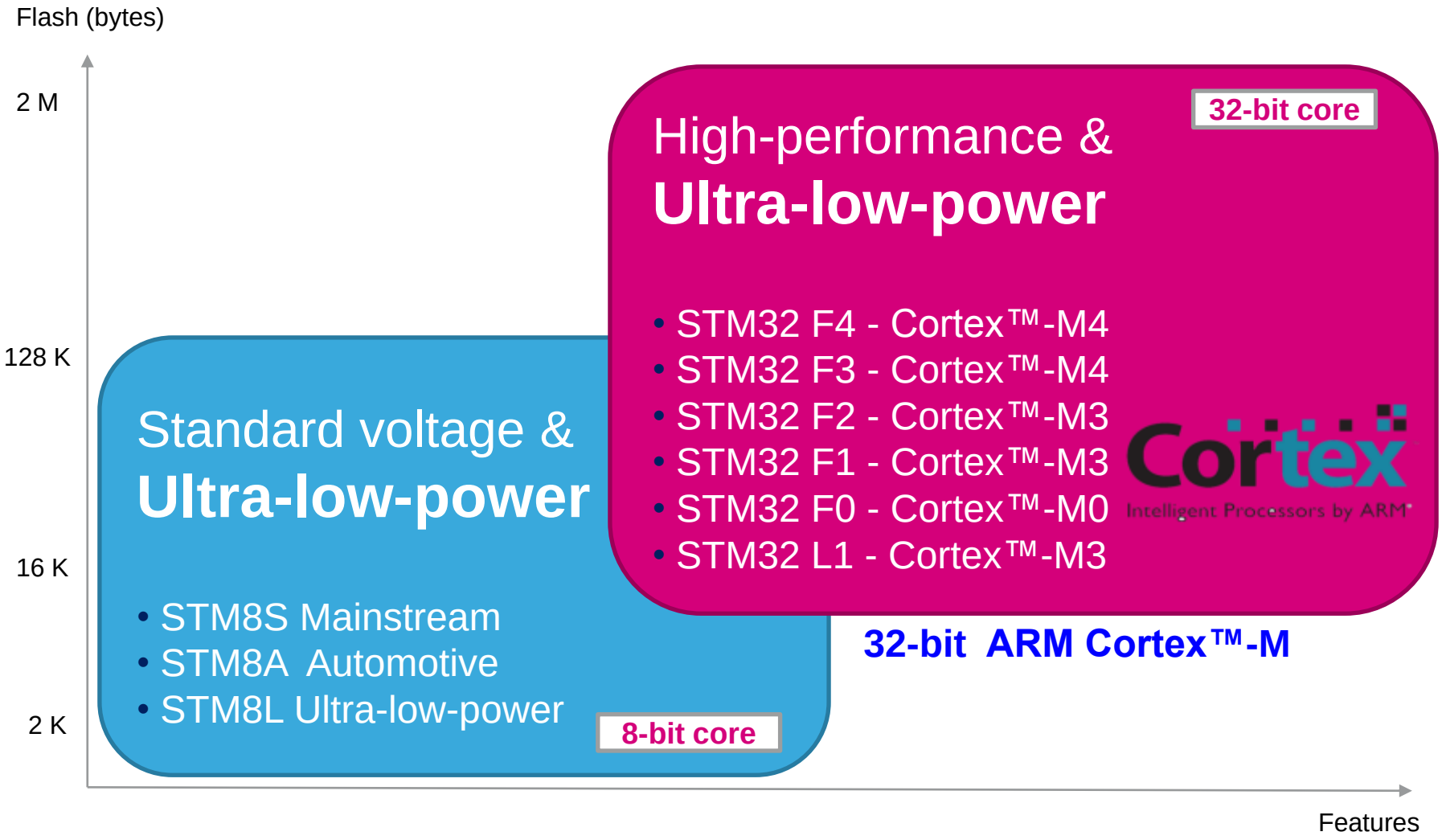
ST has licensed Cortex-M processors

- **Forget traditional 8/16/32-bit classifications and get**
  - Seamless architecture across all applications
  - Every product optimized for ultra-low power and ease of use

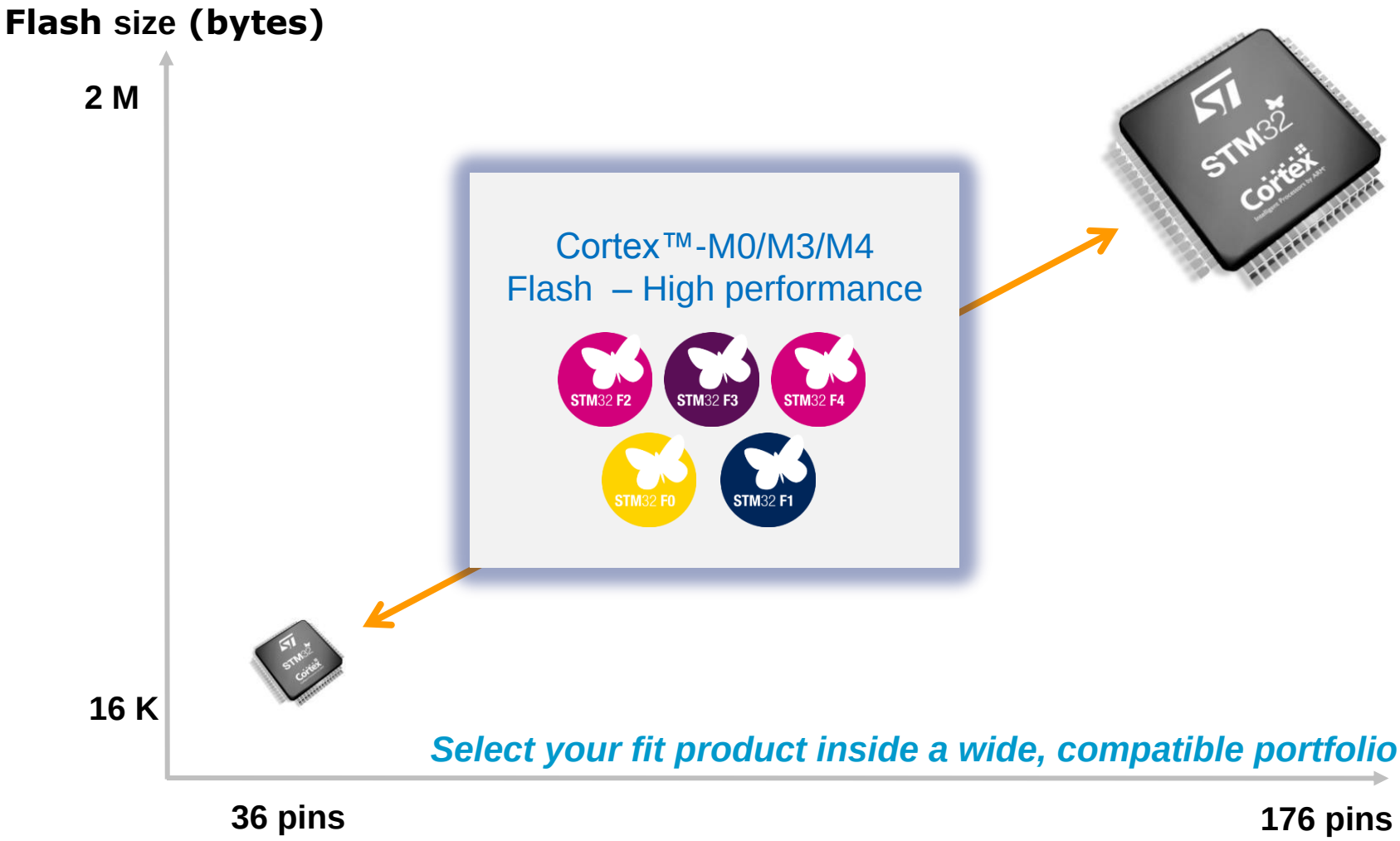
Cortex-M0	Cortex-M3	Cortex-M4
8/16-bit applications	16/32-bit applications	32-bit/DSC applications

Binary and tool compatible

MCUs – new families development focus



MCUs – new families development focus

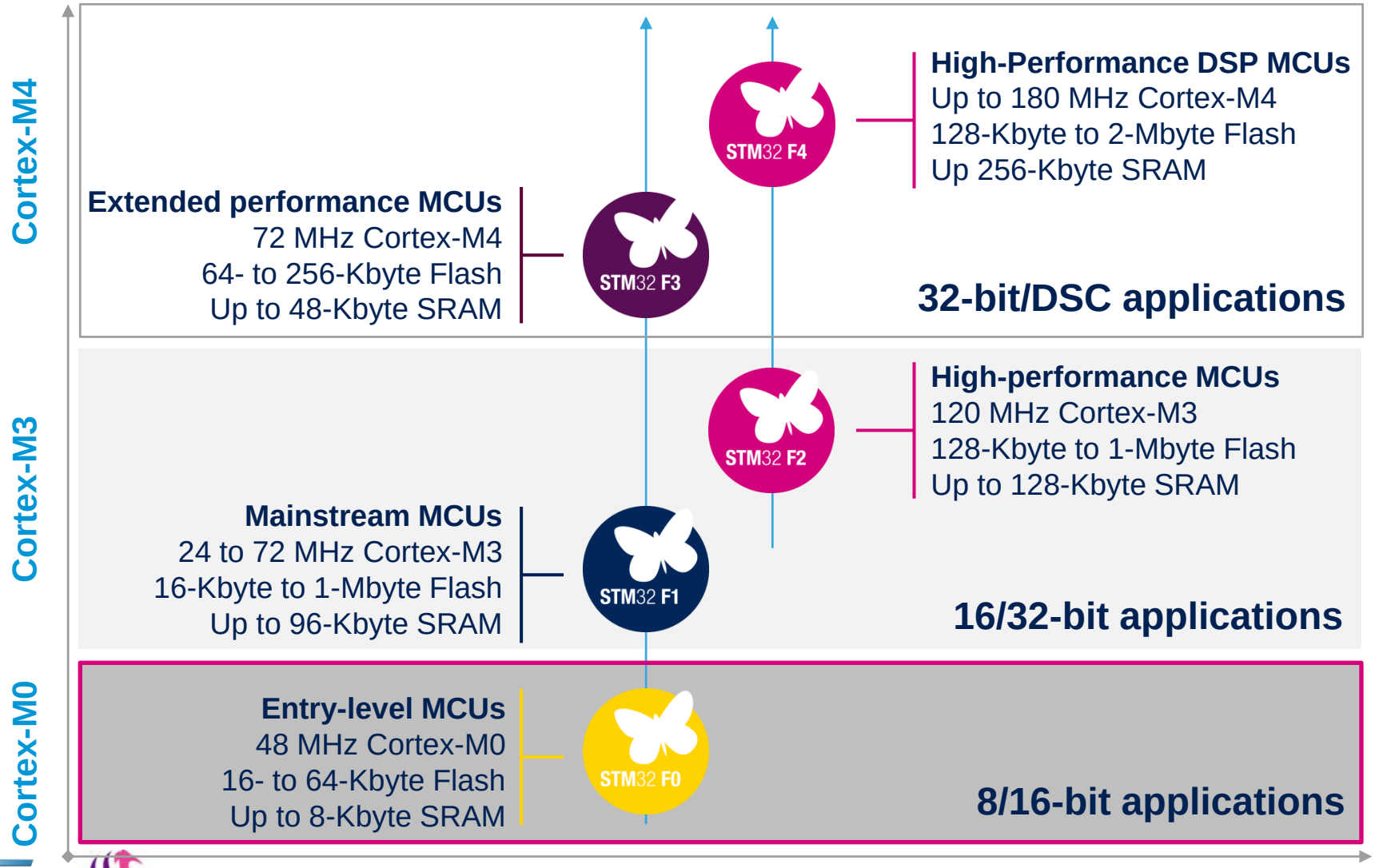


Cortex-M – firmware compatibility

- Cortex-M processors are F/W and binary compatible 
  - Migrating path M0->M3->M4 is straight forward
    - Instruction set of Cortex-Mx is strictly included in the instruction set of Cortex-My (for x<y), allowing direct migration, while taking advantage of higher MCU clock speed and von Neumann to Harvard performance increase
    - Re-compilation of the code is recommended
      - When moving from M0/M3 to M4, some part of the code might be re-coded using intrinsics, taking advantage of the advanced DSP/SIMD instructions
      - When moving backwards M3/M4 -> M0, the code needs to be recompiled in order to use only M0 instruction codes

STM32 – 6 product series

STM32F – Family by core



No compromise on robustness

Meets industry safety specifications

- Hardware **RAM** parity check
- **Clock Security System** (CSS) for switching to back-up internal RC in case of external clock failure
- **2x Watchdogs (2x WDG)** capable of real-time code execution monitoring and ensuring the application integrity independently from system clock
- **Cyclic Redundancy Check** (CRC) with DMA support for embedded Flash-memory content-integrity checking

STM32F0 Series

Entry-level MCUs for cost-sensitive applications

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Cortex-M feature set comparison

Cortex Low-Power Leadership from ARM	Cortex-M0	Cortex-M3	Cortex-M4
Architecture Version	V6M	v7M	v7ME
Instruction set architecture	Thumb, Thumb-2 System Instructions	Thumb + Thumb-2	Thumb + Thumb-2, DSP, SIMD, FP
DMIPS/MHz	0.9	1.25	1.25
Bus interfaces	1	3	3
Integrated NVIC	Yes	Yes	Yes
Number interrupts	1-32 + NMI	1-240 + NMI	1-240 + NMI
Interrupt priorities	4	8-256	8-256
Breakpoints, Watchpoints	4/2/0, 2/1/0	8/4/0, 2/1/0	8/4/0, 2/1/0
Memory Protection Unit (MPU)	No	Yes (Option)	Yes (Option)
Integrated trace option (ETM)	No	Yes (Option)	Yes (Option)
Fault Robust Interface	No	Yes (Option)	No
Single Cycle Multiply	**Yes** (Option)	Yes	Yes
Hardware Divide	No	Yes	Yes
WIC Support	Yes	Yes	Yes
Bit banding support	No	Yes	Yes
Single cycle DSP/SIMD	No	No	Yes
Floating point hardware	No	No	Yes
Bus protocol	AHB Lite	AHB Lite, APB	AHB Lite, APB
CMSIS Support	Yes	Yes	Yes

STM32F0 : 8-, 32- and 64-Kbyte fact sheet

- **ARM 32-bit Cortex-M0 core**
  - 48 MHz max CPU frequency
- **2.4 to 3.6V power supply**
- **5 x channels DMA**
- **Safety features**
  - RAM Hardware parity check, CRC, 2x watchdogs, clock security system..
- **Communication peripherals**
  - 1x USART, 1x SPI, 1x I^2C
    - I^2C fast mode + (20 mA drive capability)
    - SPI (18 Mbit/s) with 4-16 bit programmable bit frame
    - USART auto baud rate detection
  - Additional USART, SPI and I2C on 64KB versions
- **Timers**
  - 1x 16-bit PWM motor control AC timer
  - Up to 5 x 16-bit timer with up to 8xIC/OC/PWM
- **Real Time Clock**
  - H/W calendar, alarm functions and two tamper inputs
- **I/O ports**
- **Analog features**
  - 1x 12-bit ADC 1.0µS with separate analog supply and independent clock.
  - 1x Temperature Sensor
  - 1x voltage reference 1.2V
- **Debug mode**
  - Serial wire debug (SWD)

STM32F0 Product lines

Main common features

Cortex™-M0 @ 48 MHz

- PLL
- Reset + BOR
- Low and high speed oscillators
- RTC
- 2x Watchdogs
- Hardware CRC
- Reset circuitry POR/PDR
- Multiple Channel DMA
- USART, SPI and I²C
- Single Wire Debug
- Temp. sensor

STM32F051 – 2.0 to 3.6V

16- to 64-KB Flash 8-KB SRAM (parity check) 20-byte backup data	2x Comp. VBat	12-bit ADC 1 MSPS SAR	16-bit MC timer	1x 12-bit DAC	CEC I²S (I²C,USART wake-up)	Up to 18 Cap. Touch-sensing

STM32F050 – 2.0 to 3.6V

16- to 32-KB Flash 4-KB SRAM (parity check) 20-byte backup data	VBat	12-bit ADC 1 MSPS SAR	16-bit MC timer	I²S (I²C,USART wake-up)

STM32F030 Value line – 2.4 to 3.6V

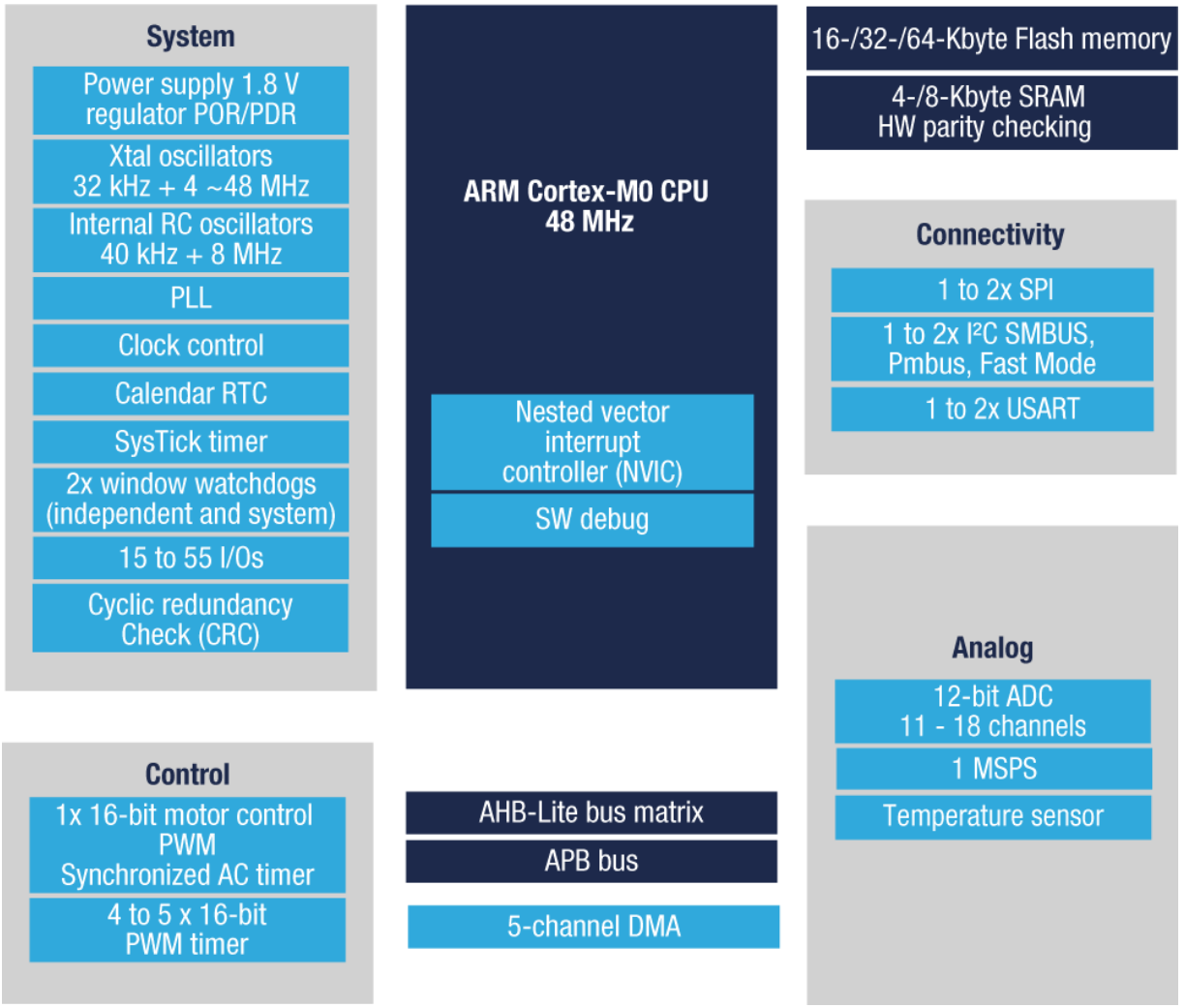
16- to 64-KB Flash Up to 8-KB SRAM (parity check)	12-bit ADC 1 MSPS SAR	16-bit MC timer

STM32 F0

New

STM32F030 block diagram

- Description
  - 2.4 to 3.6V
  - 48 MHz/38 DMIPS
  - Int. RC 8 MHz + PLL
  - Trim-able 1% RC
  - 5 channels DMA
  - Up 55 I/Os
- Packages
  - TSSOP20
  - LQFP32,48 and 64



STM32F030 Series

Entry-level MCUs for cost-sensitive applications

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Flash Features

- Flash general features:
  - Up to 64KBytes
  - 64 pages of 1KBytes size and 16 Sectors of 4KBytes size (4 pages)
  - Endurance: **1k cycles**
  - Access time: 35ns
  - Half word (16-bit) program time: 52.5µs (Typ)
  - Page erase time and Mass erase time: 30ms (Typ)

- Flash interface features:
  - Read Interface with pre-fetch buffer
  - Option Bytes loader
  - Flash program/erase operations
  - Types of Protection:
    - **Readout Protection: Level 0, Level 1 and Level 2 (No debug)**
    - Write Protection

- Memory organization:
  - Main Program memory block (or Main Flash memory)
  - Information block : 3KBytes of System memory + 6 Option Bytes (12 with complements)
    - 2 option bytes for write protection and 1 for Readout protection
    - 1 option byte for device configuration : VDDA supervisor, BOOT1, Reset w/ STDBY/STOP, IWWG HW
    - 2 option bytes reserved for user data

Low Power Modes(1/2)

- **SLEEP Mode**: Core stopped, peripherals kept running
  - Entered by executing special instructions
    - WFI (Wait For Interrupt)
    - WFE (Wait For Event)
- **STOP Mode**: all periph clocks, PLL, HSI and HSE are disabled, SRAM and registers contents are preserved.
  - If the RTC and IWWDG are running they are not stopped in STOP (either as their clock sources)
  - To further reduce power consumption the Voltage Regulator can be put in Low Power mode
- **STANDBY Mode**: Voltage Regulator off, the entire V18 domain is powered off.
  - SRAM and register contents are lost except registers in the Backup domain and STANDBY circuitry
  - PLL, the HSI RC and the HSE crystal oscillators are also switched off.
  - RTC and IWWDG are kept running in STANDBY (if enabled)
  - In STANDBY mode all IO pins are high impedance and non-active except

Low Power Modes(2/2)

Parameter	Condition	f_{HCLK}	Typ		Unit
			Peripherals enabled	Peripherals disabled	
Supply current in Run mode, code executing from Flash	HSE crystal clock 8MHz	48 MHz	23.3	11.5	mA
		8MHz	4.5	3.0	

Parameter	Condition	Typ @V_{DD}	Max	Unit
		3.6V	T_A = 85℃	
Supply current in stop mode	Regulator in run mode, all oscillators OFF	19	48	uA
	Regulator in low-power mode, all oscillators OFF	5	32	
Supply current in Standby mode	LSI ON and IWDG ON	2	-	

Clock Features

- System Clock (SYSCLK) sources:
  - **HSE** (High Speed External osc) 4MHz to 32MHz, can be bypassed by user clock
  - **HSI** (High Speed Internal RC): factory trimmed internal RC oscillator 8MHz +/- 1%
  - **PLL** x2, x3, .. x16 (16MHz min. output freq.)
- Additional clock sources:
  - **LSI** (Low Speed Internal RC): 30kHz ~ 50kHz internal RC
  - **LSE** (Low Speed External oscillator): 32.768kHz, can be bypassed by user clock
  - **HSI14** (High Speed Internal RC 14MHz): dedicated oscillator for ADC
- Clock-out capability on the MCO (HSI14, LSI, LSE, SYSCLK, HSI, HSE, PLL/2)
- Clock Security System (**CSS**) to switch to backup clock in case of HSE clock failure
  - Enabled by SW w/ interrupt capability linked to Cortex NMI
- RTC Clock sources: LSE, LSI and HSE clock divided by 32
- USART, I2C & CEC have multiple possible clock sources

Timers overview

Timer type	Timer	Counter resolution	Counter Type	DMA request generation	Capture/ compare channels	Complementary outputs
Advanced Control	TIM1	16 bit	Up, down, up/down	Yes	4	Yes
General purpose	TIM3		Up, down, up/down	Yes	4	No
	TIM14		Up	No	1	No
	TIM15		Up	Yes	2	Yes
	TIM16, TIM17		Up	Yes	1	Yes
Basic	TIM6		Up	Yes	0	No

USART Features (1/2)

- Fully-programmable serial interface characteristics:
  - Configurable oversampling method by 16 or by 8
  - Up to 6Mbps when the clock frequency is 48MHz and oversampling by 8 is selected.
- Programmable data order with MSB or LSB first.
- Swappable Tx/Rx pin configuration
- Dual clock domain allowing
  - UART functionality and wakeup from Stop mode
  - Convenient baud rate programming independent from the PCLK reprogramming
- Support for DMA
- LIN Master/Slave compatible
- Synchronous Mode: Master mode only

USART Features (2/2)

- IrDA SIR Encoder Decoder
- Smartcard Capability T = 0(character mode), T = 1(block mode) (using the Address/character match, End of block, receiver timeout etc…)
- Single wire Half Duplex Communication
- Multi-Processor communication
  - USART can enter Mute mode
  - Mute mode: disable receive interrupts
  - Wake up from mute mode (by idle line detection or address mark detection)
- Auto-baudrate detection using various character patterns.
- Driver enable (for RS485) signal sharing the same pin as nRTS.

USART Implementation

USART features	USART1	USART2
Hardware Flow Control	YES	YES
Continous communication using DMA	YES	YES
Multiprocessor communication	YES	YES
Synchronous mode	YES	YES
Smartcard mode	YES	NO
Single wire half duplex mode	YES	YES
IrDA	YES	NO
LIN	YES	NO
Dual clock domain and wake up from STOP mode	YES	NO
Receiver timeout	YES	NO
Modbus Communication	YES	NO
Autobaudrate detection	YES	NO
Driver enable	YES	YES

RTC Features(1/2)

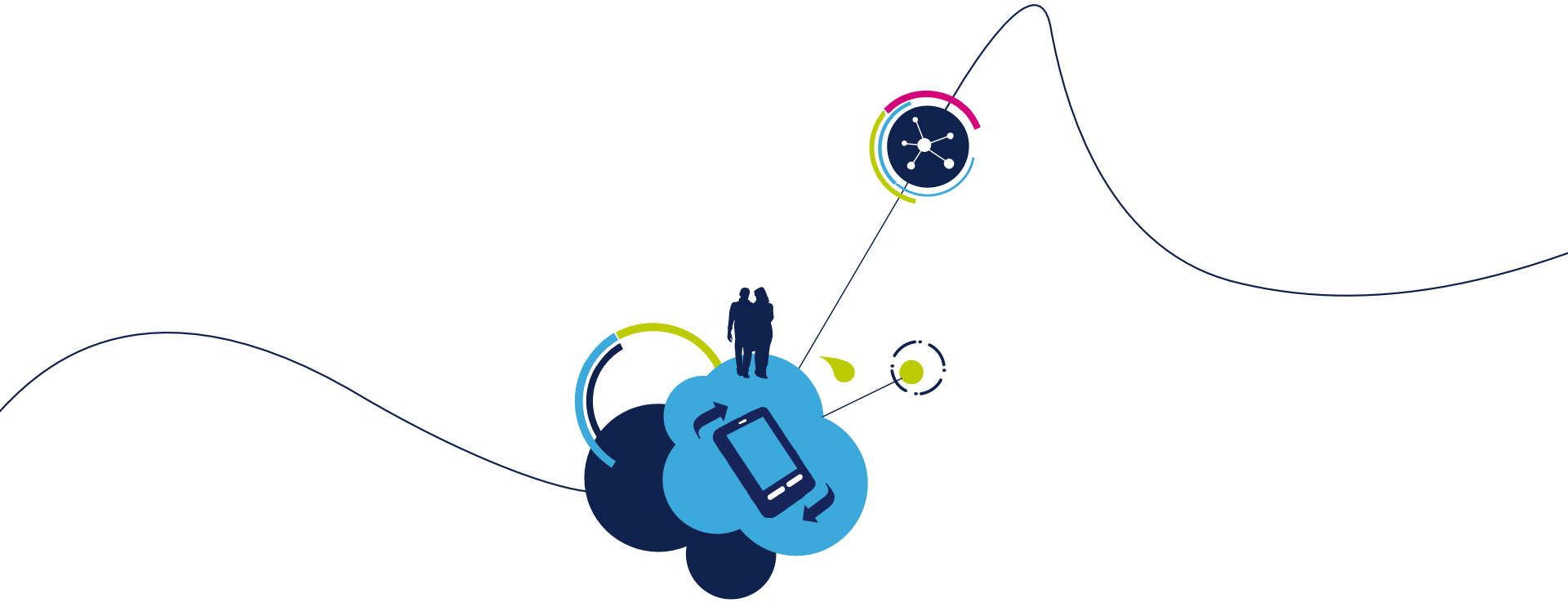
- Calendar with subseconds, seconds, minutes, hours(12 or 24), week day, date, month, and year. In BCD(binary-coded decimal) format
- Automatically correction for 28, 29, 30 and 31 day of the month
- Programmable alarm with wake up from Stop and Standby mode capability
- Digital calibration circuit with 1ppm resolution, to compensate for quartz crystal inaccuracy
- 2 anti-tamper detection pins with programmable filter
- Timestamp feature which can be used to save the calendar content.
- Periodic wakeup from Stop/Standby
- Reference clock detection : a more precise second source clock(50 or 60 Hz) can be used to enhance the calendar precision.

RTC Features(2/2)

- The RTC clock sources can be :
  - A 32.768kHz external crystal
  - A resonator or oscillator
  - The internal low-power RC Oscillator
  - The High-speed external clock divided by 32

ADC Features

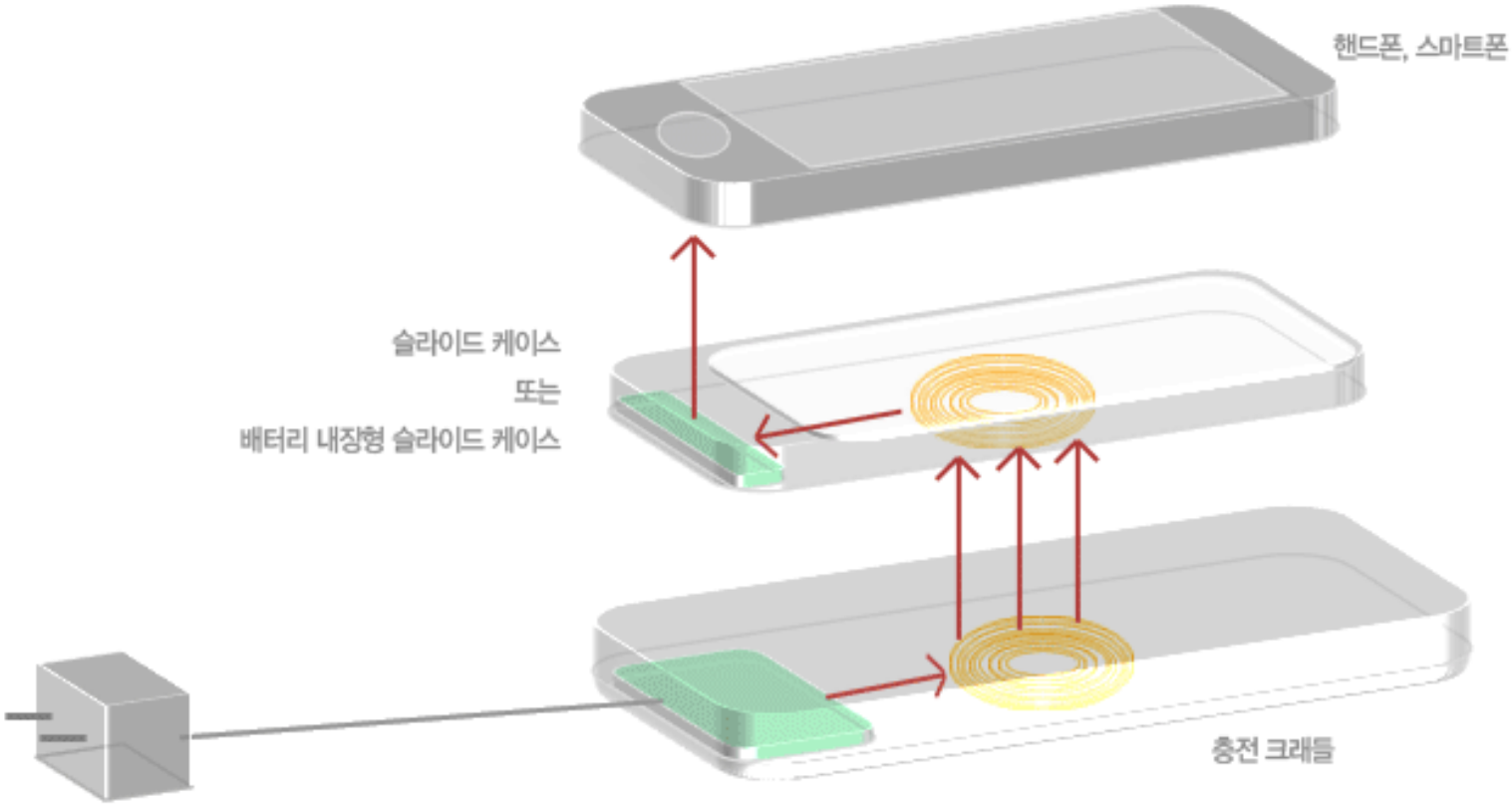
- ADC conversion rate 1 MHz and 12-bit resolution
- Conversion range: 0 to 3.6 V
- ADC supply requirement: 2.4 V to 3.6 V
- ADC input range: $V_{SSA} \leq V_{IN} \leq V_{DDA}$
- Up to 16 external channels
  - 16 external channels
  - 2 internal channels connected to :
    - Temperature sensor V_{SENSE}
    - Internal voltage reference V_{REFINT}



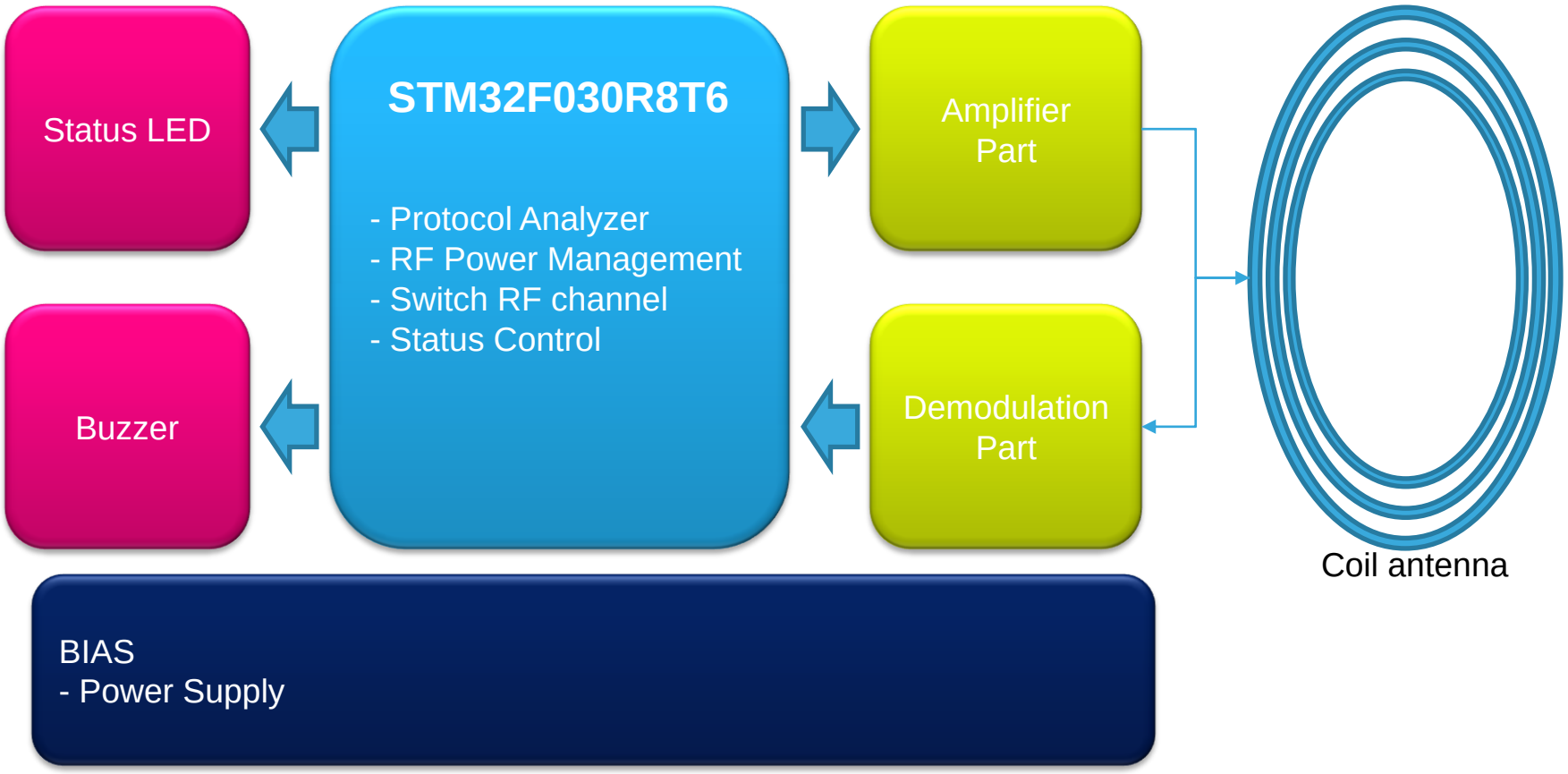
Demostration

- WPC(Wireless Power Charger)
- BLDC Motor Control

WPC(Wireless Power Charger)



WPC(Wireless Power Charger)



WPC(Wireless Power Charger) Demostration

BLDC Motor Driving

1. MCU (STM32F030R8T6)
2. Sensor(Hall, Encoder, OPAMP)

MCU VDD

CONTROL BLOCK

VDC BUS

POWER SUPPLY BLOCK

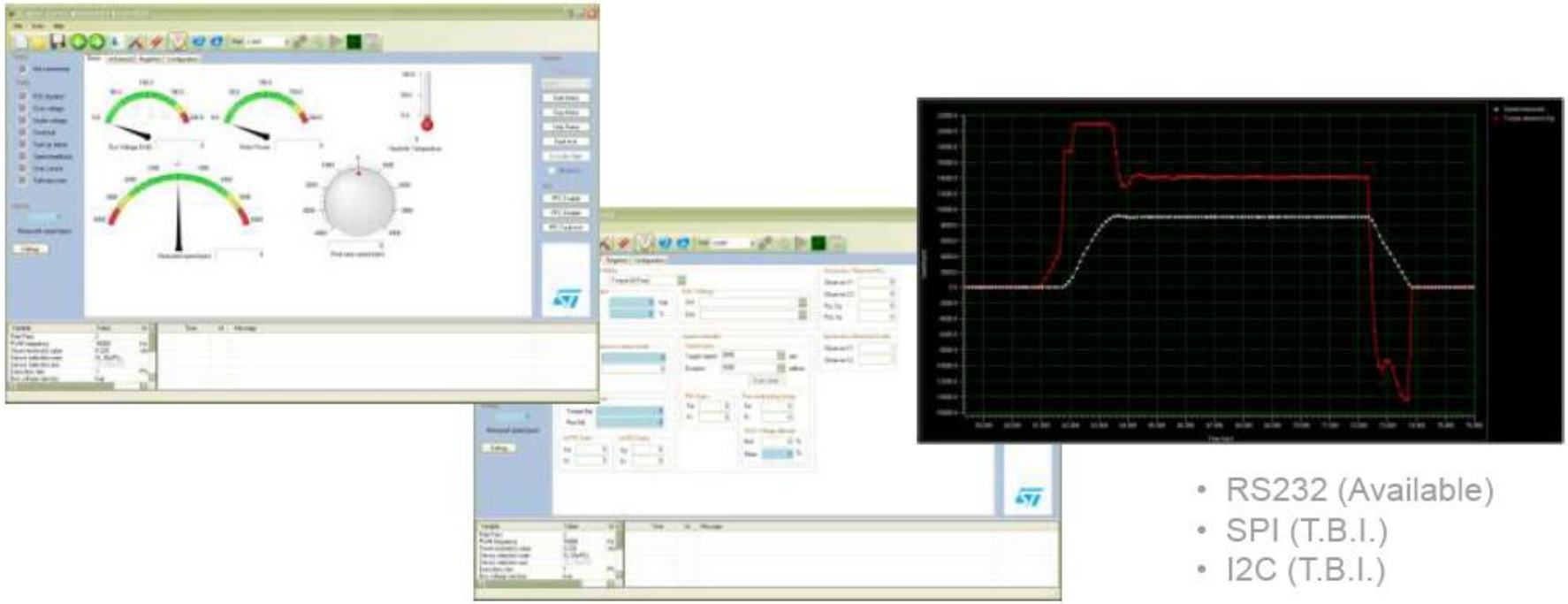
POWER BLOCK

1. Rectifier
2. High voltage converter
3. Voltage regulator : Step down

1. Gate driver
2. Half bridge(FET or IGBT)

BLDC Motor Driving

- Serial communication
  - Start / Stop commands
  - Set speed ramp.
  - Fine tuning motor control variables
  - Real time communication



- RS232 (Available)
- SPI (T.B.I.)
- I2C (T.B.I.)

BLDC Motor Control Demostration

Thank you

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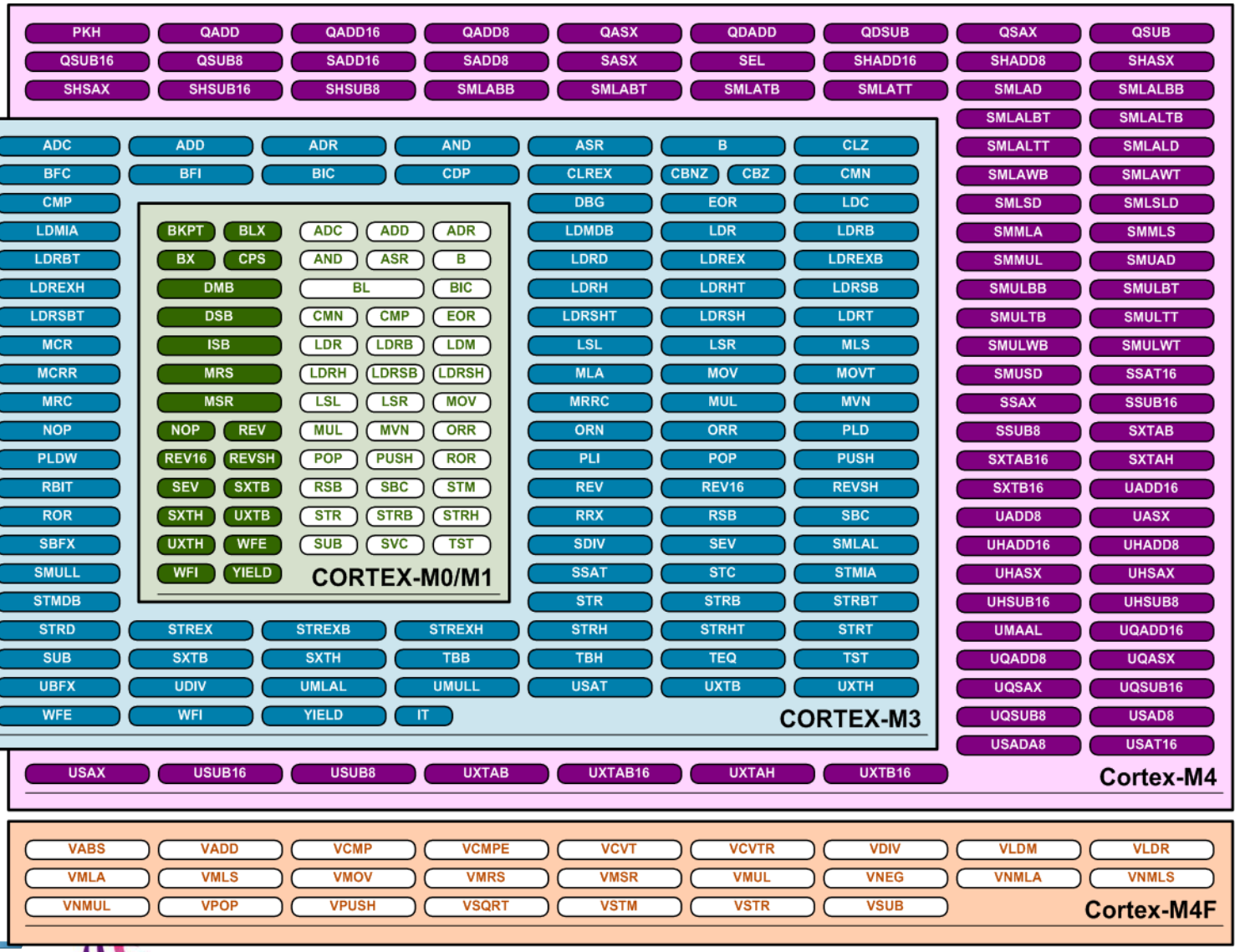
Cortex-M processors binary compatible



USART register map

27.6.8 USART register map

The table below gives the USART register map and reset values.

Table 198. USART register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	USART_SR	Reserved																						CTS	LBD	TXE	TC	RXNE	IDLE	ORE	NE	FE	PE
	Reset value																							0	0	1	1	0	0	0	0	0	0
0x04	USART_DR	Reserved																						DR[8:0]									
	Reset value																							0	0	0	0	0	0	0	0	0	0
0x08	USART_BRR	Reserved																DIV_Mantissa[15:4]														DIV_Fraction [3:0]	
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

24.7.12 USART register map

The table below gives the USART register map and reset values.

Table 96. USART register map and reset values

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0x00	USART_CR1	Res.	Res.	Res.	Res.	EOBIE	RTOIE	DEAT4	DEAT3	DEAT2	DEAT1	DEAT0	DEDT4	DEDT3	DEDT2	DEDT1	DEDT0	OVER8	CMIE	MME	M	WAKE	PCE	PS	PEIE	TXEIE	TCIE	RXNEIE	IDLEIE	TE	RE	LESM	UE
	Reset value					0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	USART_RDR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	RDR[8:0]								
	Reset value																								0	0	0	0	0	0	0	0	0
0x28	USART_TDR	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	TDR[8:0]								
	Reset value																								0	0	0	0	0	0	0	0	0