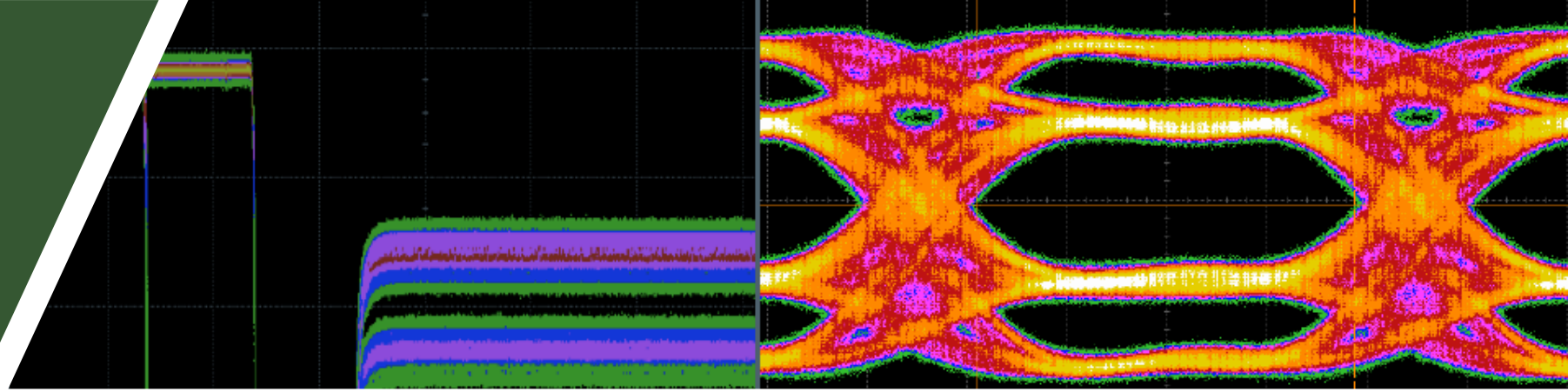


MIPI 개발 및 최적화를 위한 측정기술과 ADAS 적용사례

2018. 3. 15.

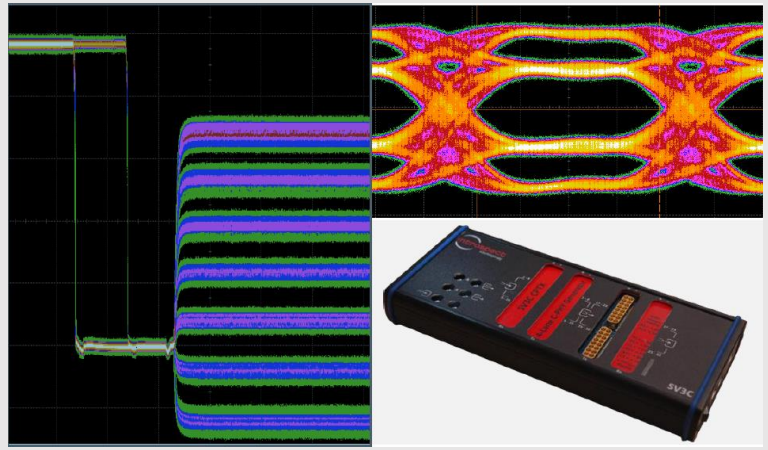
제이윌테크놀로지 대표 지충선

JWILL TECHNOLOGY 제이윌테크놀로지
Innovating Test Automation

introspect technology

내용

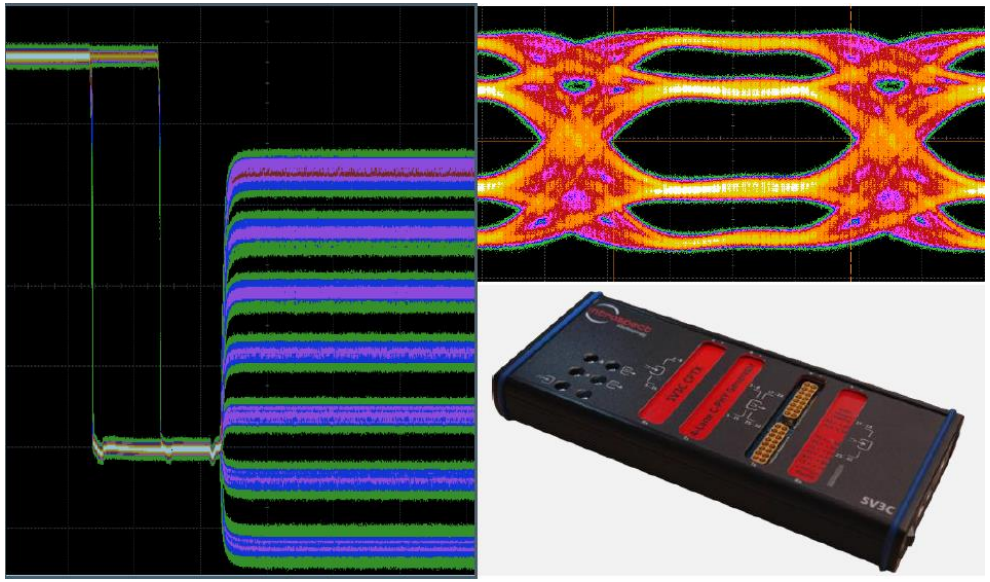
- 웨비나 목적과 대상
- MIPI 개요
- MIPI 인터페이스 기술들
- 설계와 최적화 과제
- 응용사례 연구 - MIPI Testing in ADAS
- Introspect Technology MIPI 측정 솔루션
- 결론



제이윌테크놀로지
JWILL TECHNOLOGY
Innovating Test Automation

<MIPI 개발 및 최적화를 위한 측정기술과 ADAS 적용사례>

웨비나 목적과 대상



웨비나 목적과 대상

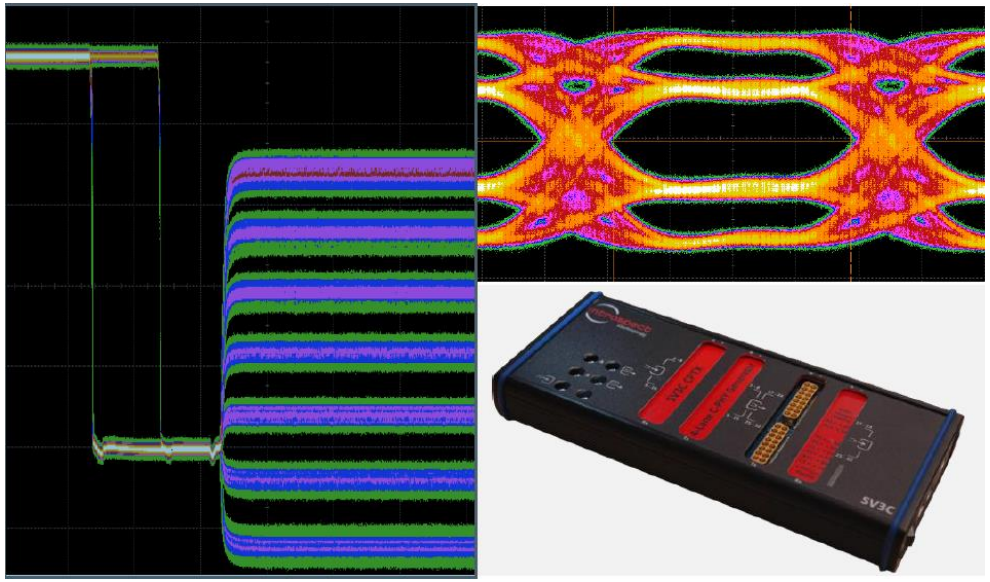
목적

- MIPI 관련 인터페이스 개발 및 최적화 작업에 보다 효율적인 솔루션을 제공해 드리기 위함.

대상

- 모바일 카메라 혹은 디스플레이 인터페이스 설계, 개발, 시험/측정 실무자
- 모바일 시스템 설계/통합 기술자
- 모바일 프로젝트 관리자
- 자동차, IoT, 의료기기등 응용분야에 MIPI 적용을 검토중이신 분
- 기타 MIPI Test Solution에 대해 관심있으신 분

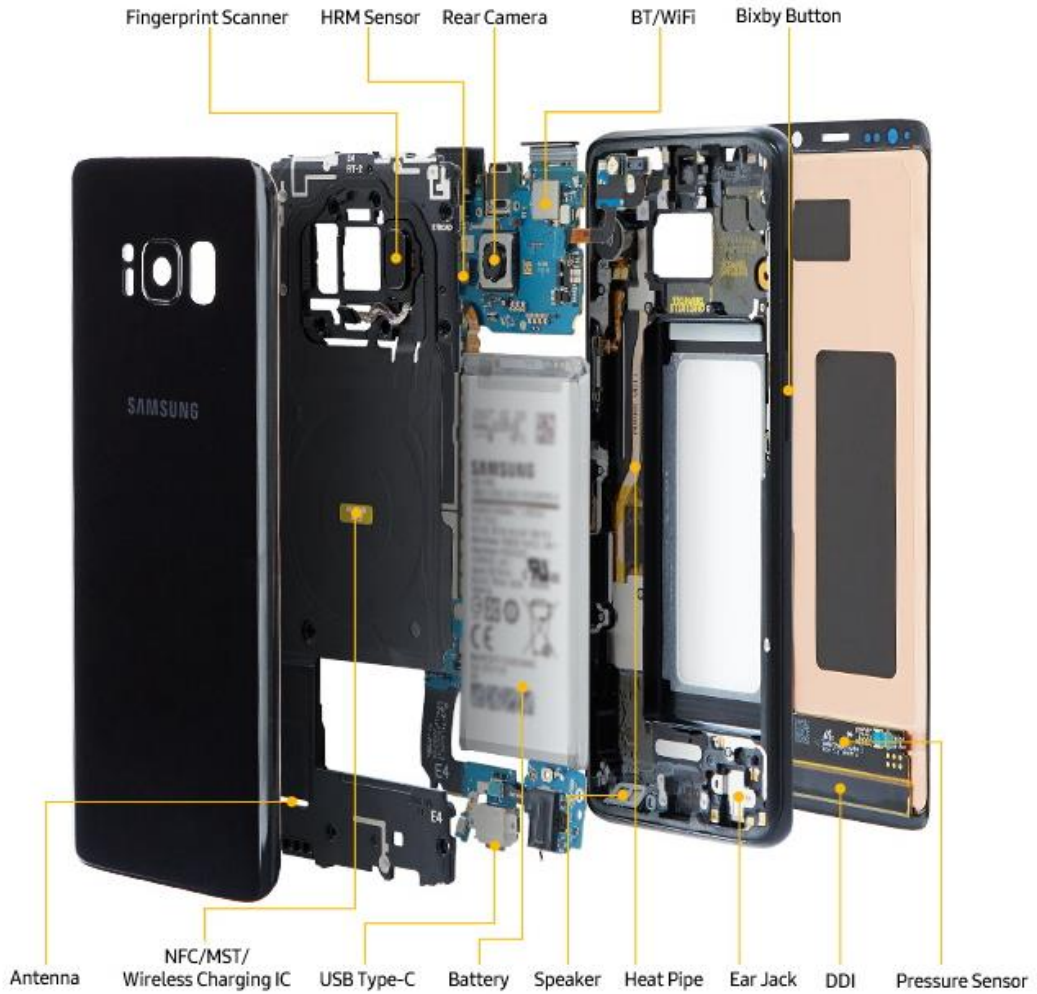
MIPI 개요



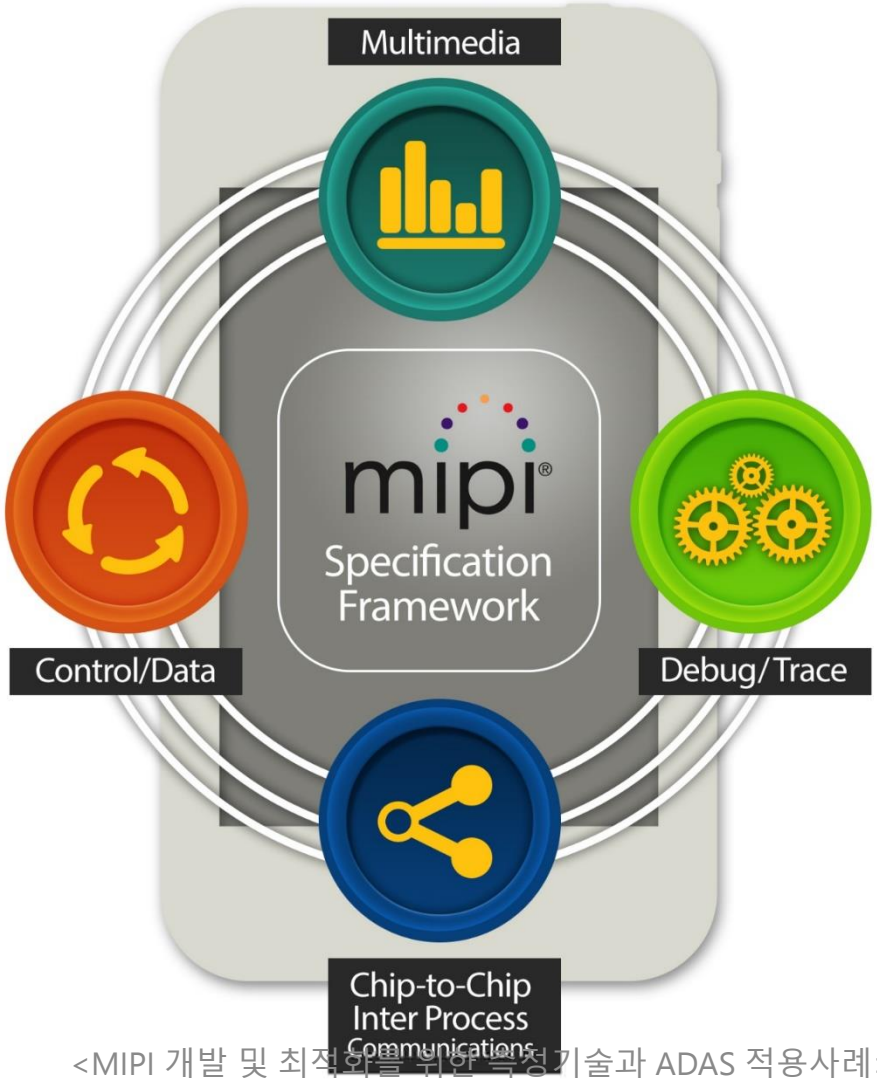
MIPI

~~Mobile Industry Processor Interface~~

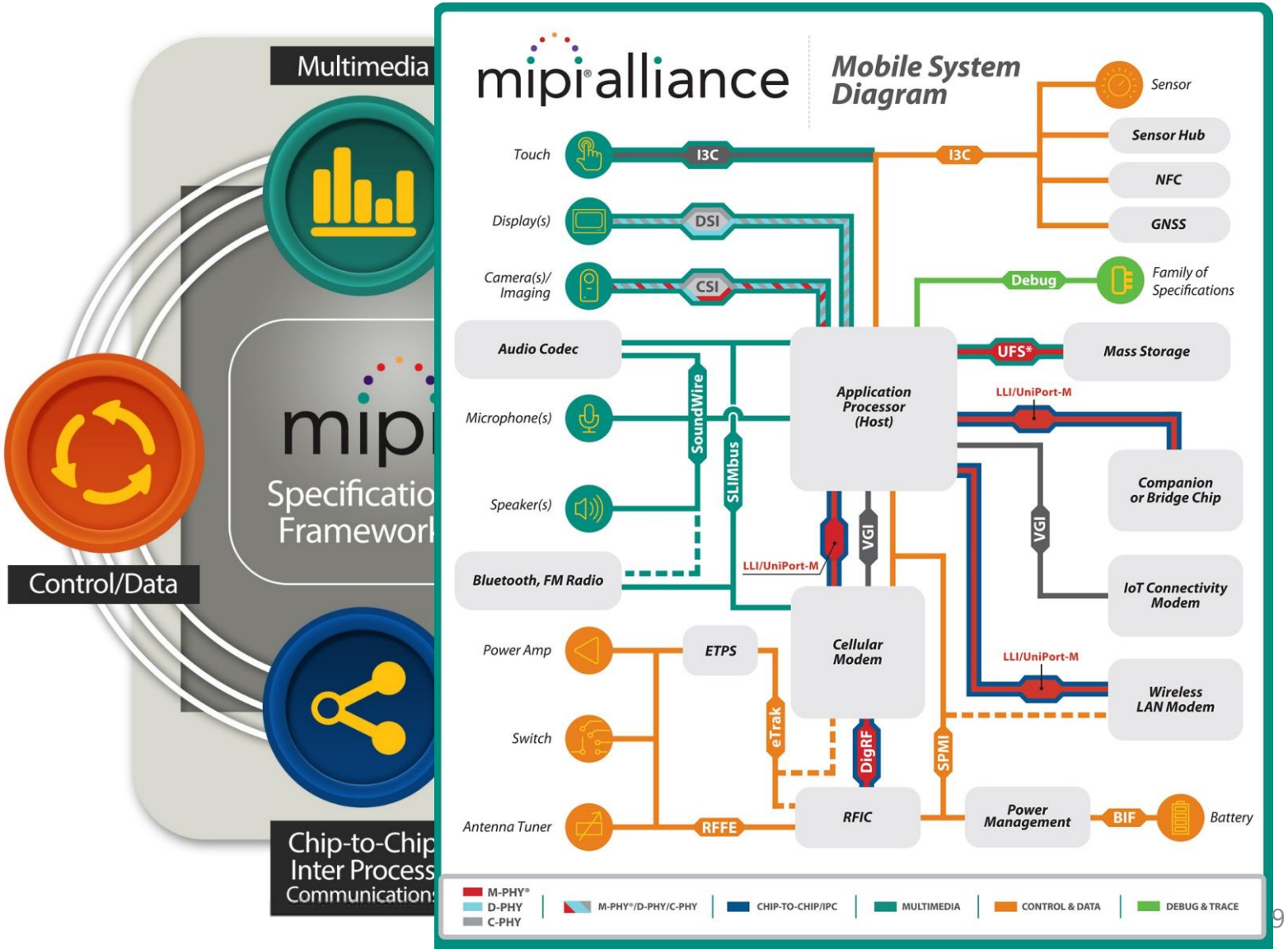
Inside Mobile Phones



The Standard for Mobile



The Standard for Mobile & Mobile Influenced Industry



Influenced by… Highly Accomplished Ecosystem

Automotive

Internet Appliances

Medical

intel
NVIDIA
Texas Instruments
LG
HUAWEI
SK hynix
SAMSUNG
PIXELPLUS

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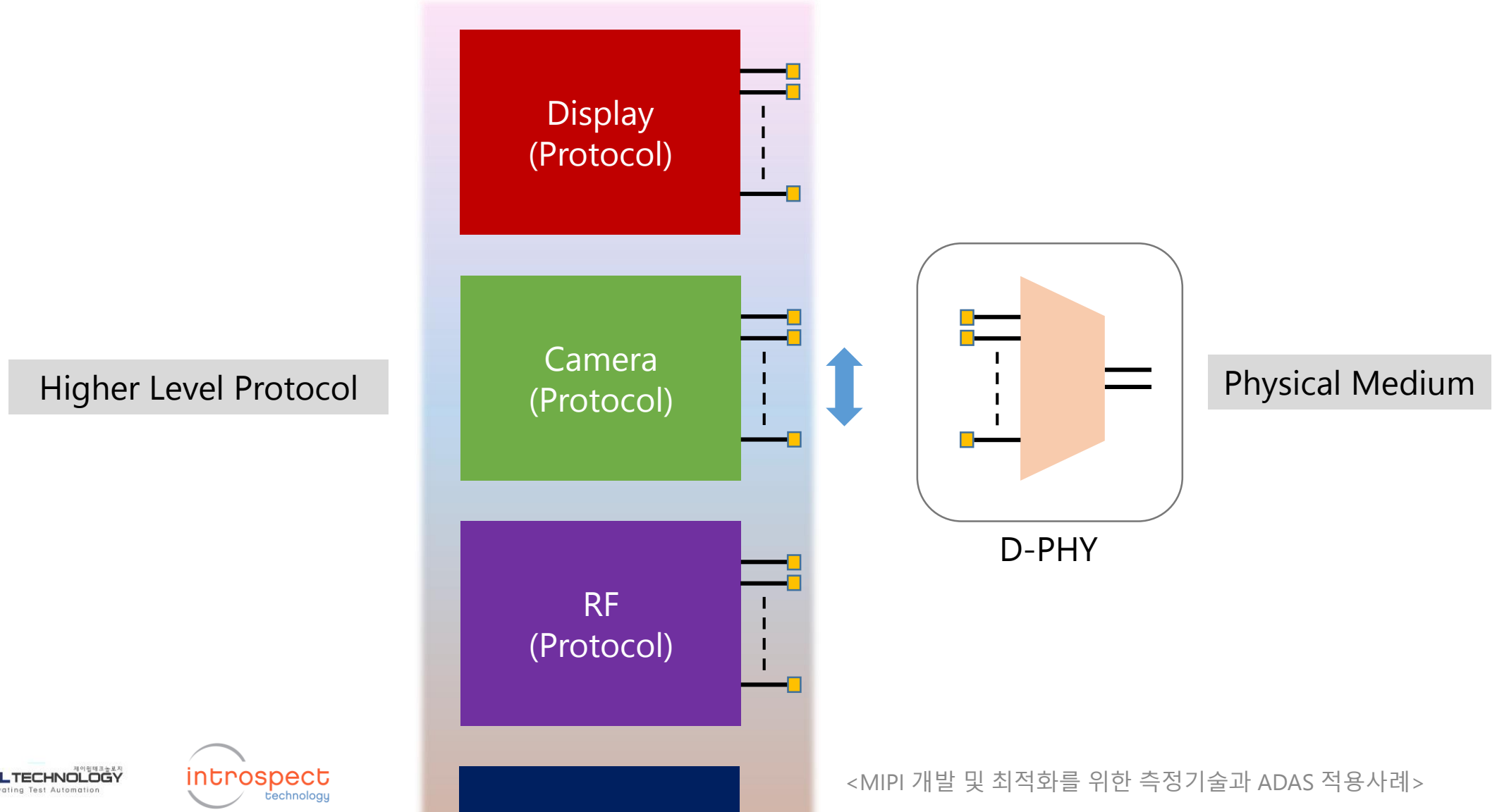
introspect technology

Origins: Modular PHY and Protocol Implementations



Flexibility: Variable Data Rate Unlike Other Standards

Low Resolution

Source: Flir

Low MIPI Data Rate

Medium Resolution

Source: PixelPlus

Medium MIPI Data Rate

High Resolution

Source: Telsa

High MIPI Data Rate

Standard does not specify data rate!

Key Takeaways

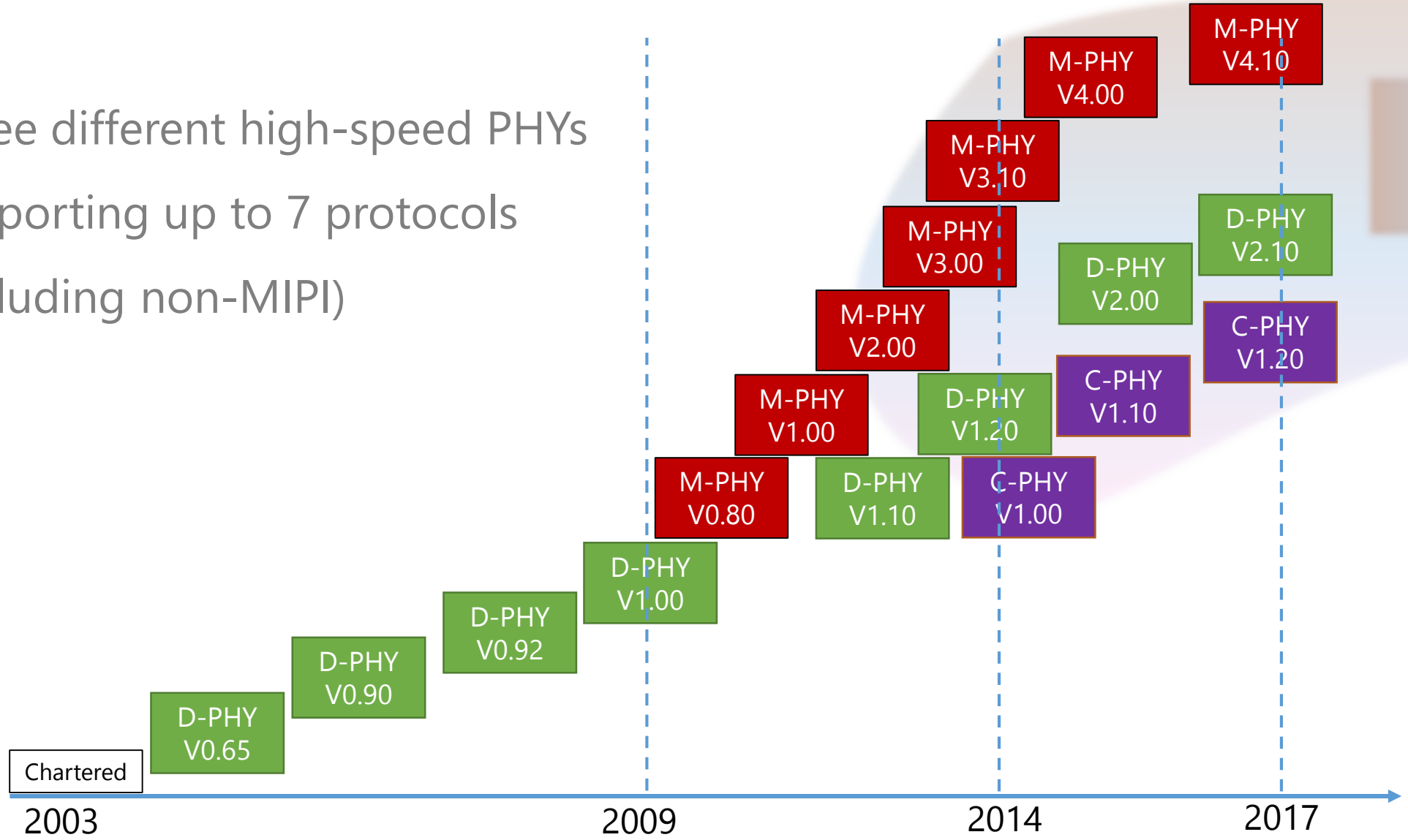
Modular construction of protocol and physical layers

Any rate operation

Challenge and Opportunity!

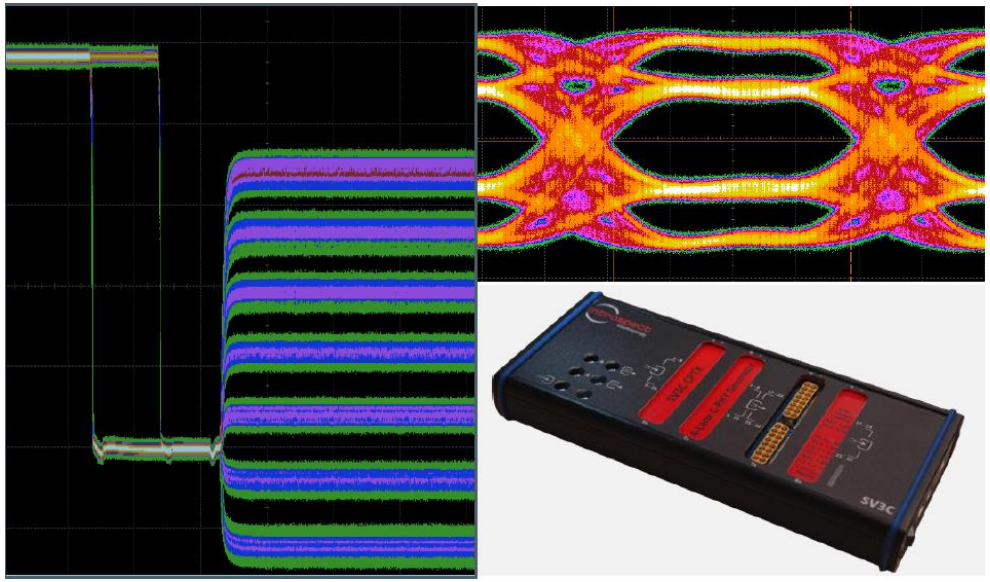
Rapid PHY Evolution (High Speed Links)

Three different high-speed PHYs supporting up to 7 protocols (including non-MIPI)

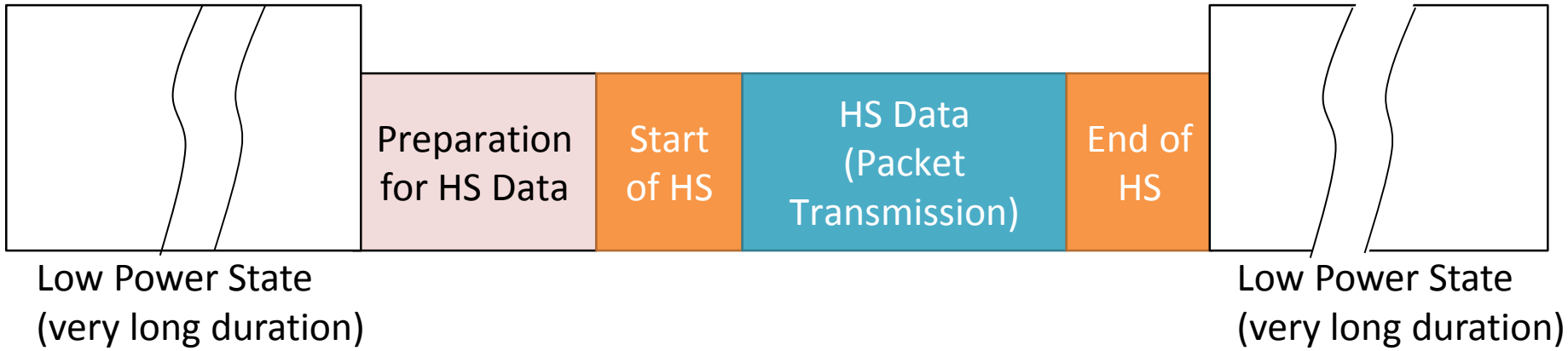


MIPI 인터페이스 기술들

- D-PHY, C-PHY 중심으로 -



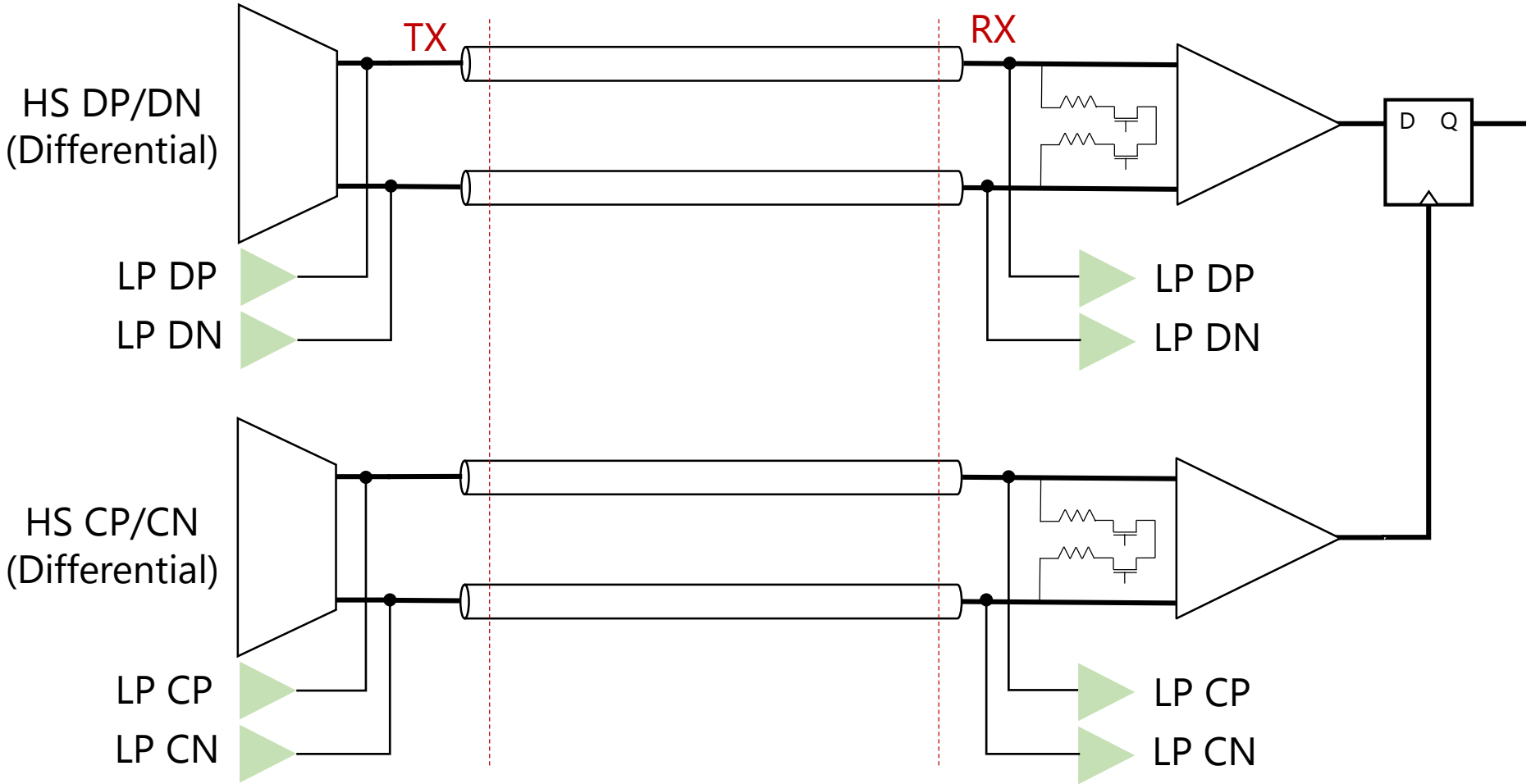
Unified Theme: Low Power, Burst-Mode Operation



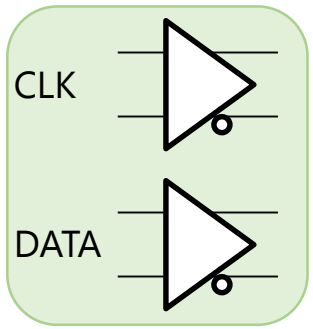
LP state is included to conserve power

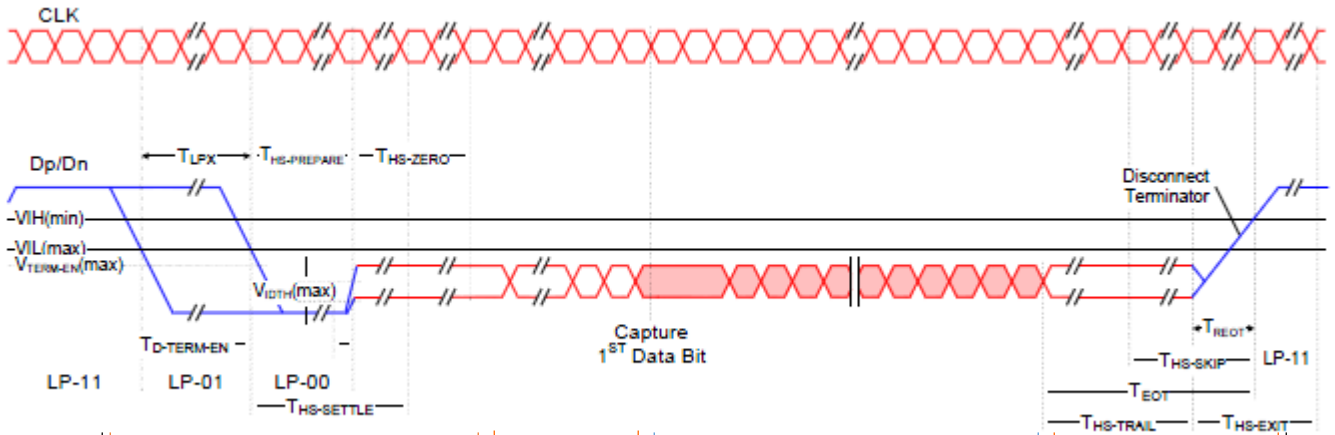
Different PHY layers define the transmission states differently

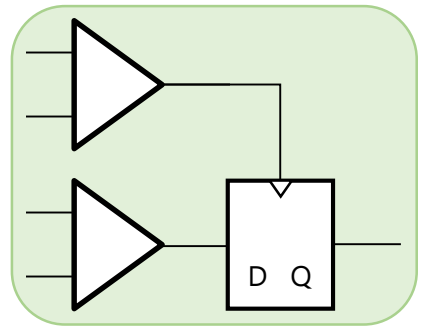
D-PHY is Source Synchronous



D-PHY is Source Synchronous







LP consists of LVCMOS single-ended signals

HS prep. consists of LP11-LP01-LP00 transition followed by differential zero signal

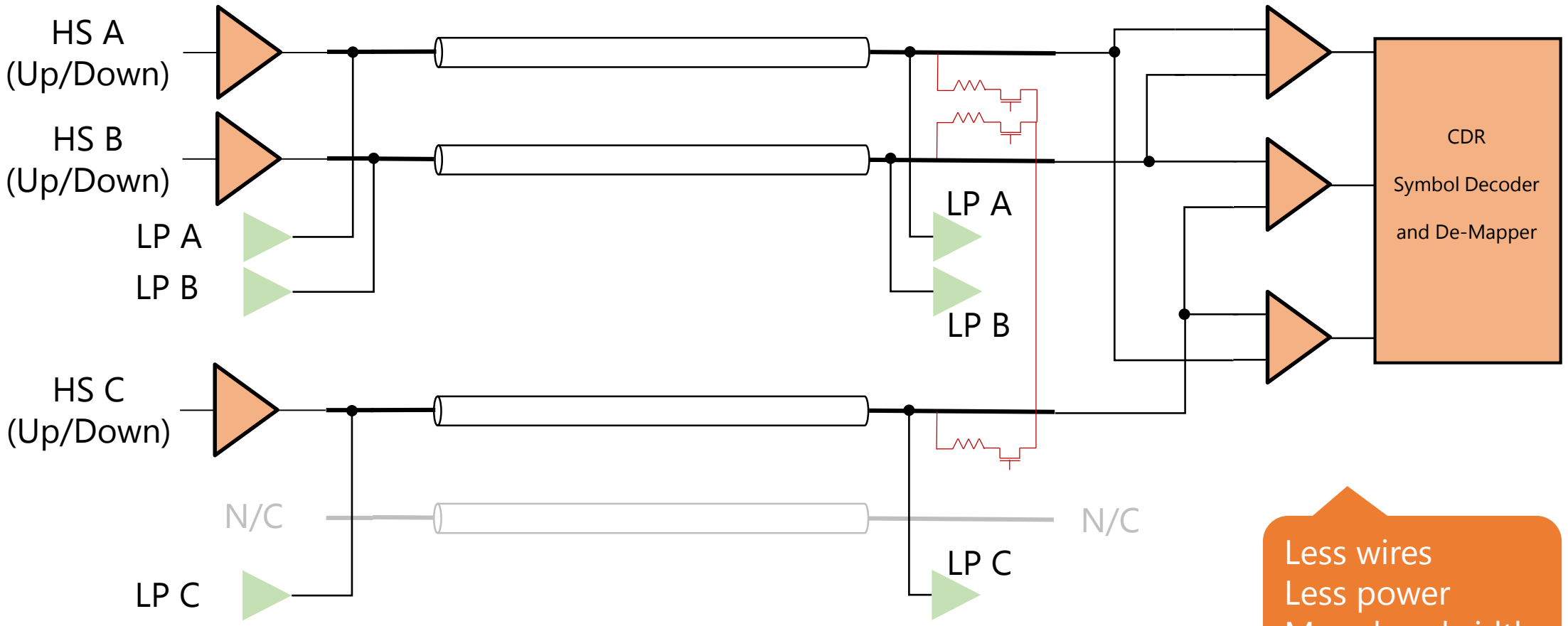
Start of HS data is signified by SOT word

HS data is source synchronous with CLK

End of HS data is signified by constant value followed by LP11

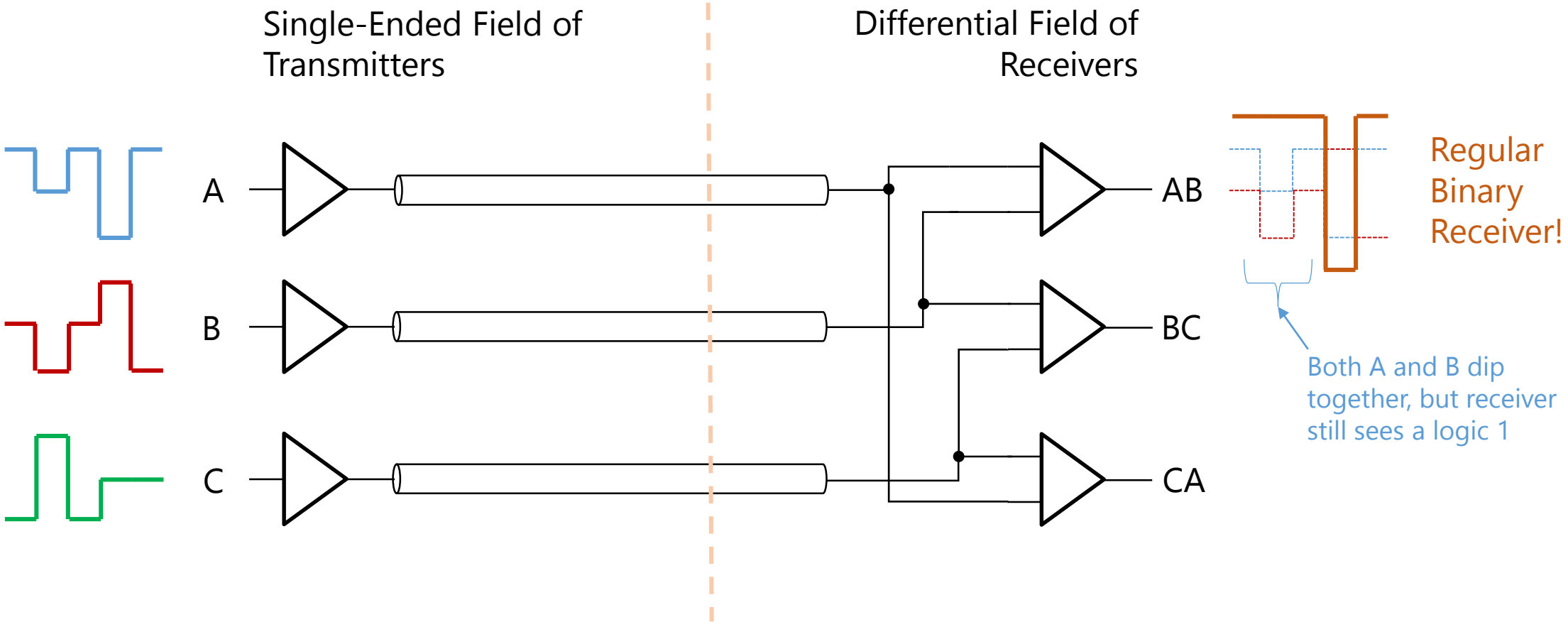
LP is single-ended again

C-PHY is Three Phase Encoding – One Trio, Embedded Clock

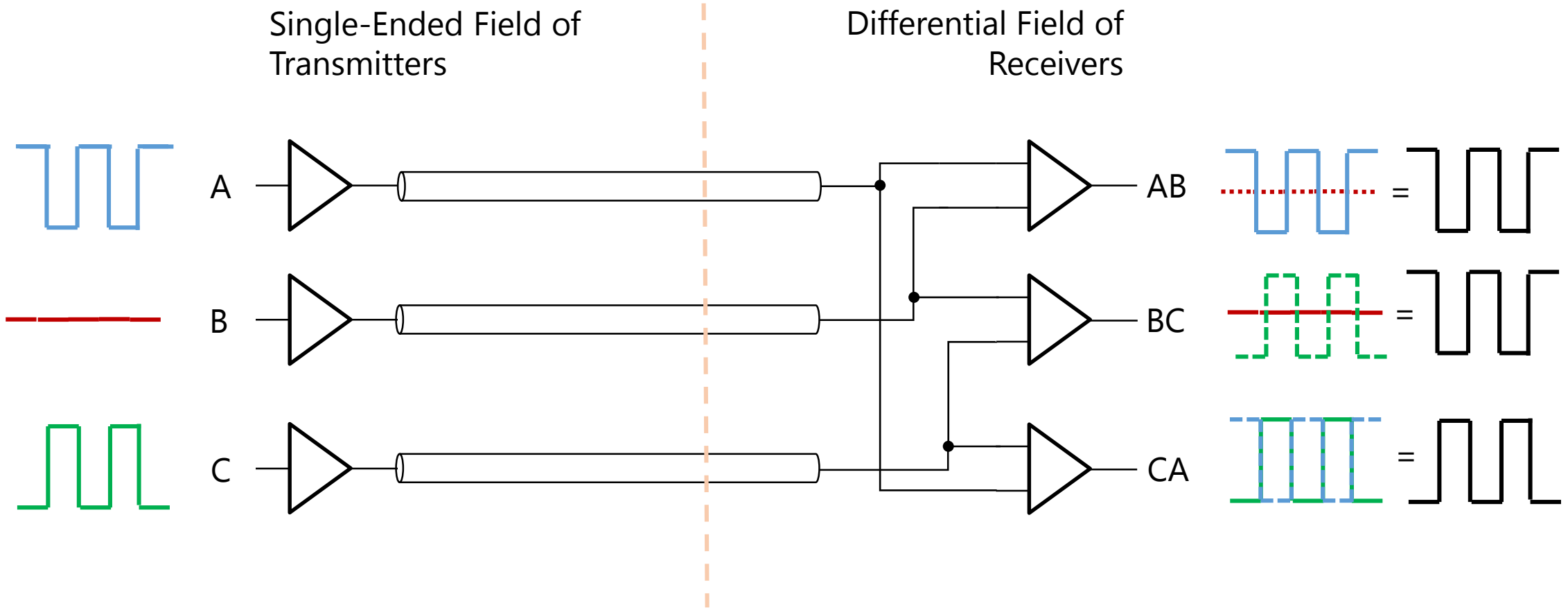


Less wires
Less power
More bandwidth

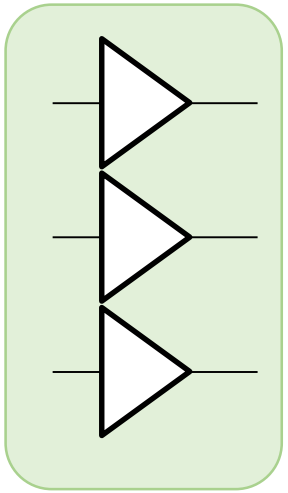
Three Voltage Levels Per Wire Ensure Proper Differential Reception

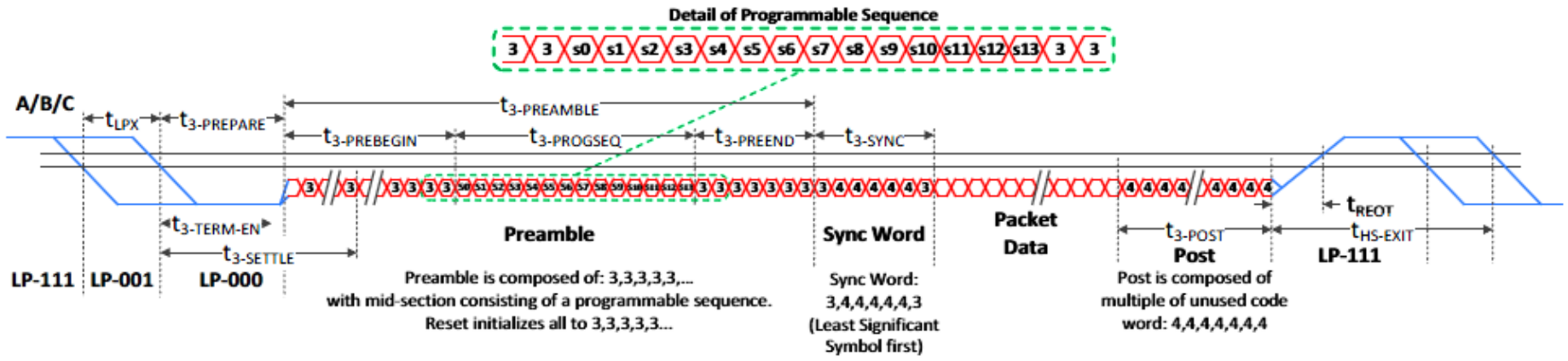


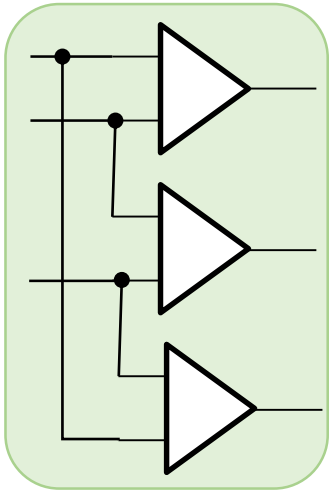
Always-Toggle Design Allows for Simple Clock Recovery (100% Aggregate Transition Density)



C-PHY is Three-Phase Encoded (Embedded Clock)







LP consists of LVCMOS single-ended signals

HS prep. consists of LP111-LP011-LP000 transition followed by constant 3,3,3,.. sequence

Start of HS data is signified by SYNC word

HS data is "three-phase" specially encoded (no clock)

End of HS data is signified by constant 4,4,4... sequence

LP is single-ended again

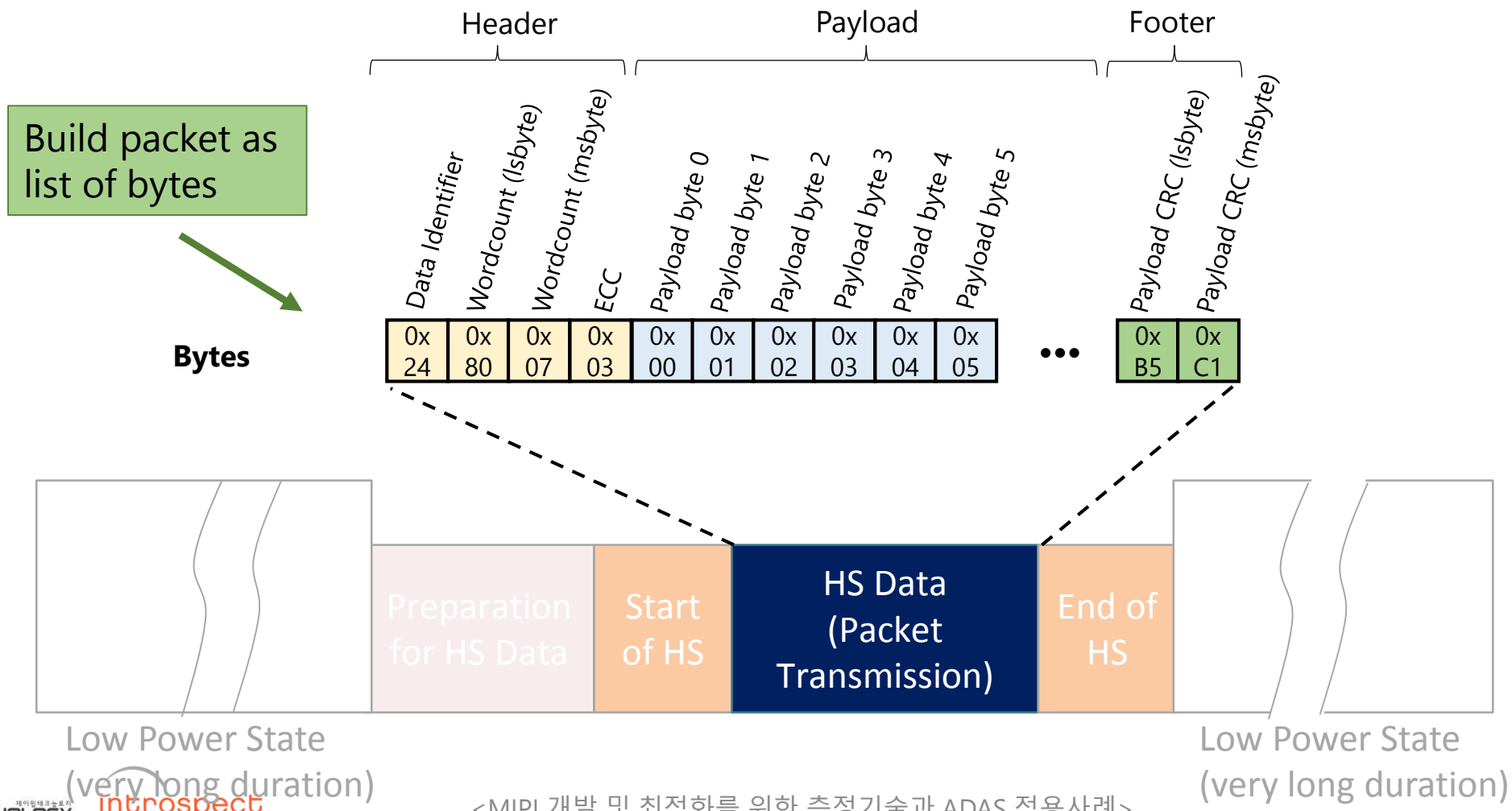
See Our Pres at

mipi DEVCON

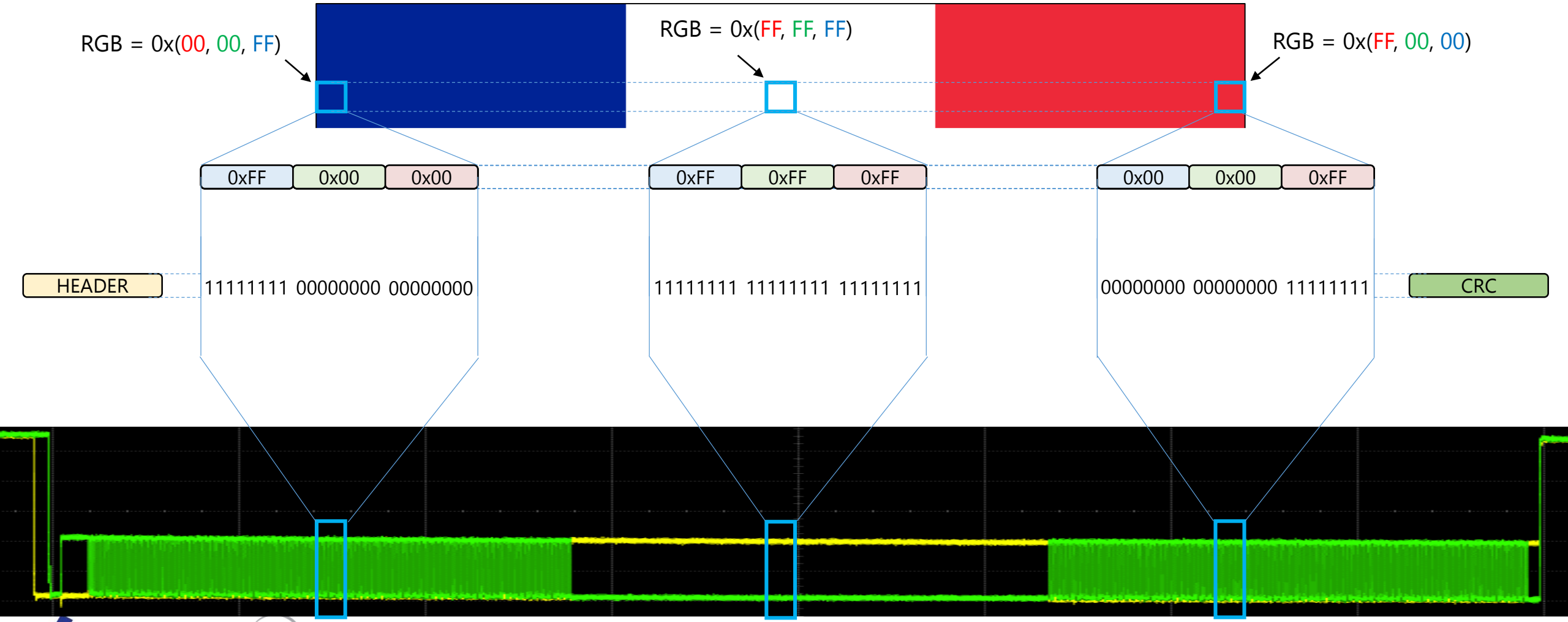
27 October 2017
BANGALORE, INDIA

MIPI.ORG/DEVCON

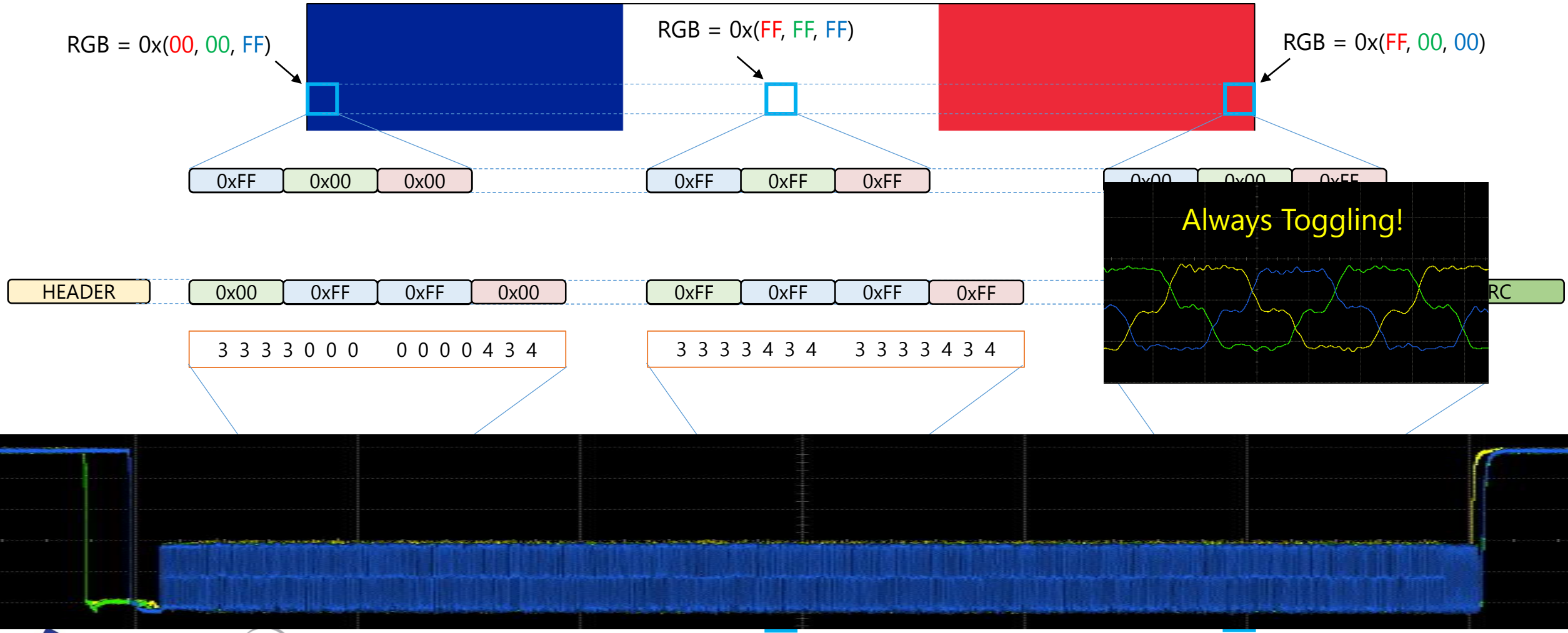
HS Data: Packet Based Transmissions



Visualizing Transmissions – Camera & Display (D-PHY)

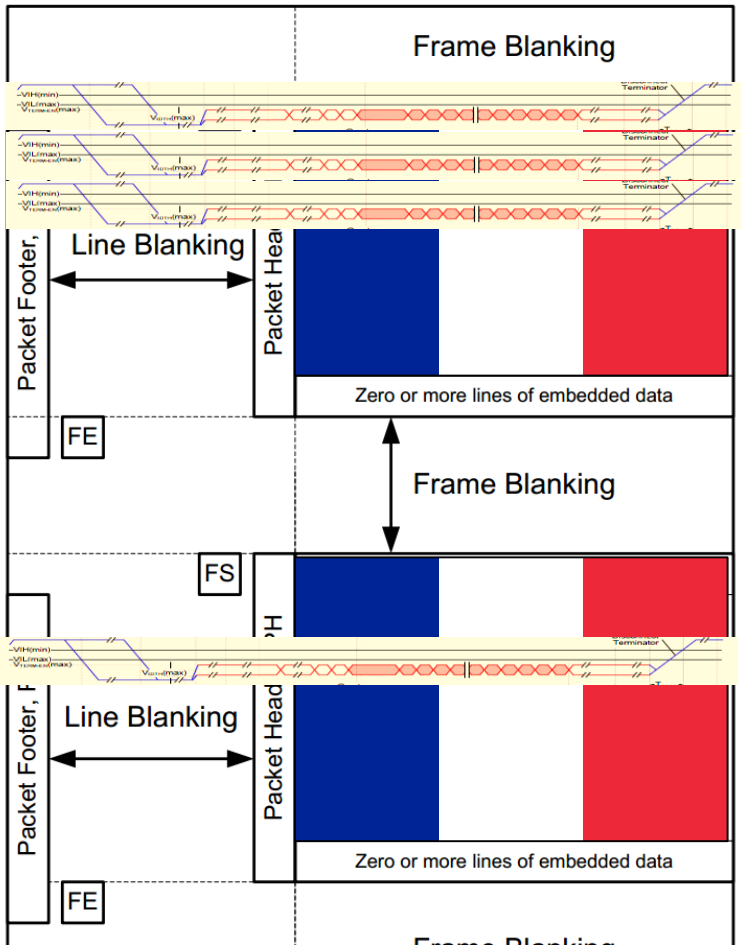


Visualizing Transmissions – Camera & Display (C-PHY)

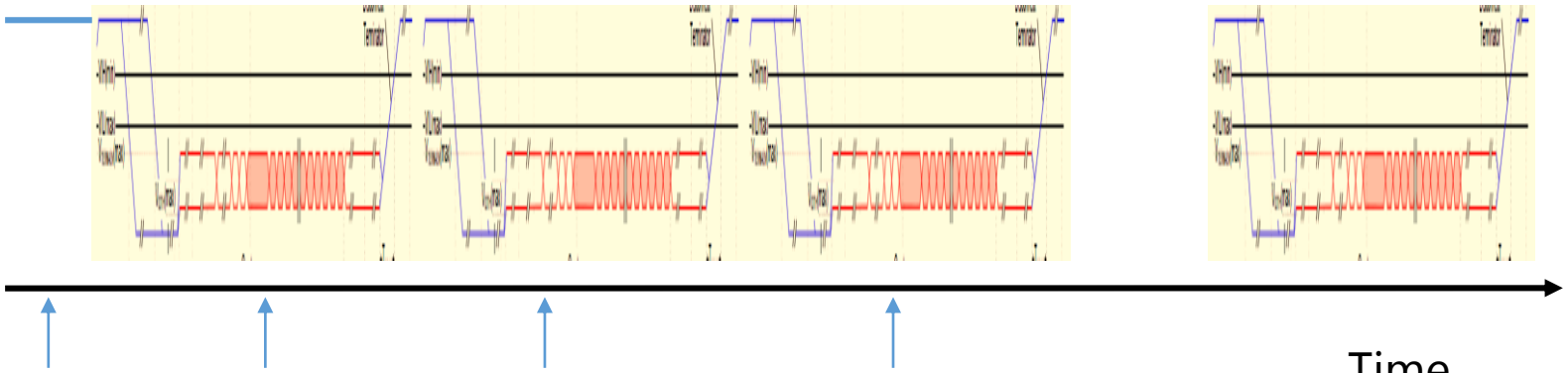


Video Streaming

CSI-2 On D-PHY / C-PHY



LP11 Stop State



D-PHY Held in LP11 During Frame Blanking

One Packet for One Line (after FS)

One Packet for One Line

One Packet for One Line

Key Takeaways

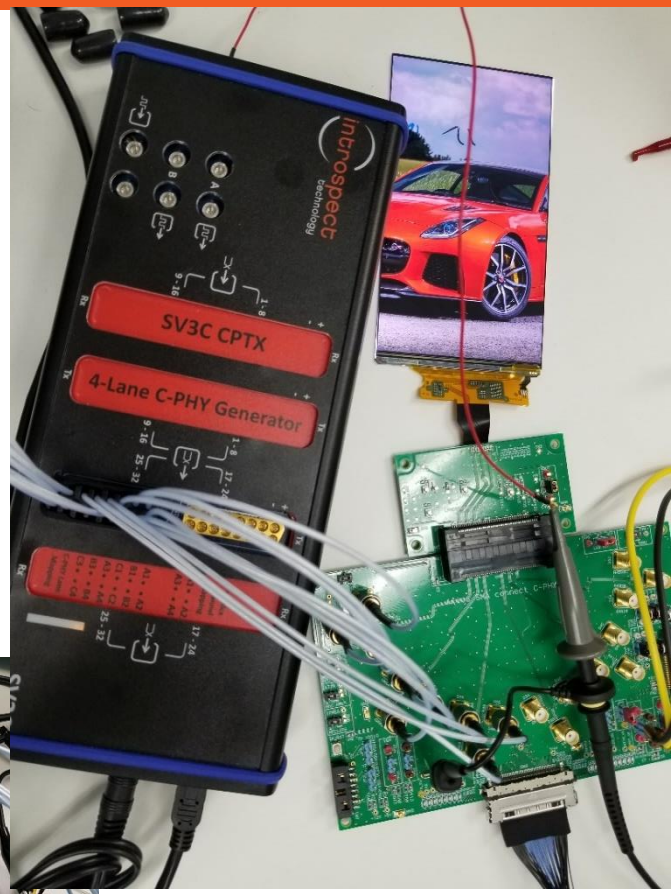
Display and camera systems leverage packet-based transmission technology through MIPI standards

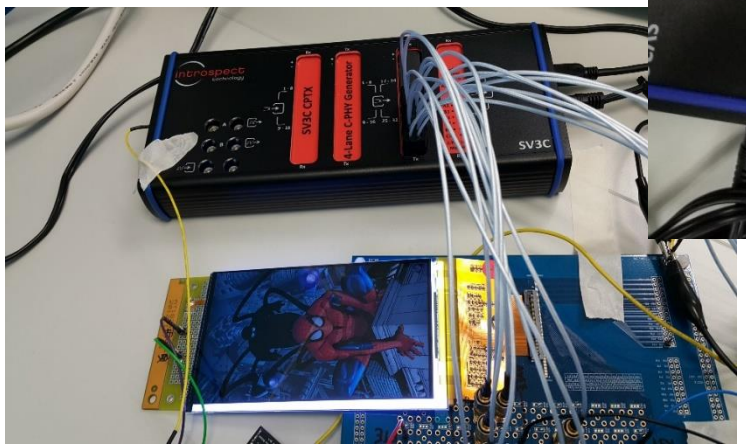
Signal transmission mechanisms vary slightly at the physical layer, but they always strive for low power dissipation

Practical Implementations – Display

- Display ecosystem is heavily invested in MIPI DSI/DSI-2 protocol
- Pervasive presence of D-PHY 1.1, 1.2
- Strong growth in C-PHY 1.1 due to reduction in number of wires

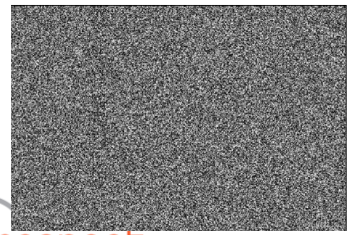
- Trends:
  - Higher speeds!
  - Scrambling
  - 30 bpp color depth
  - VESA v1.2 compression





Original image: 24 BPP

On the wire: 8 BPP



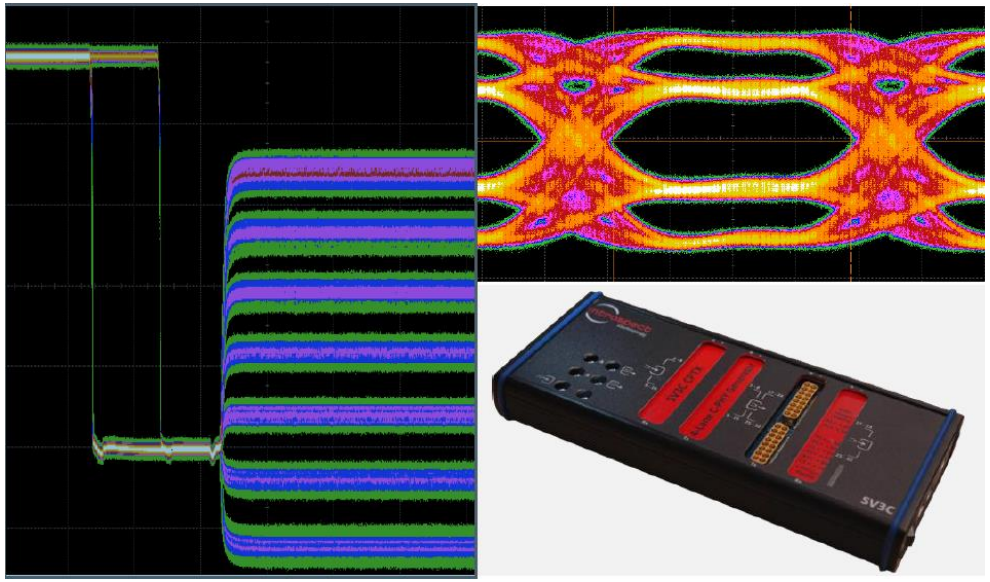
Received image: 24 BPP

Practical Implementations – Camera

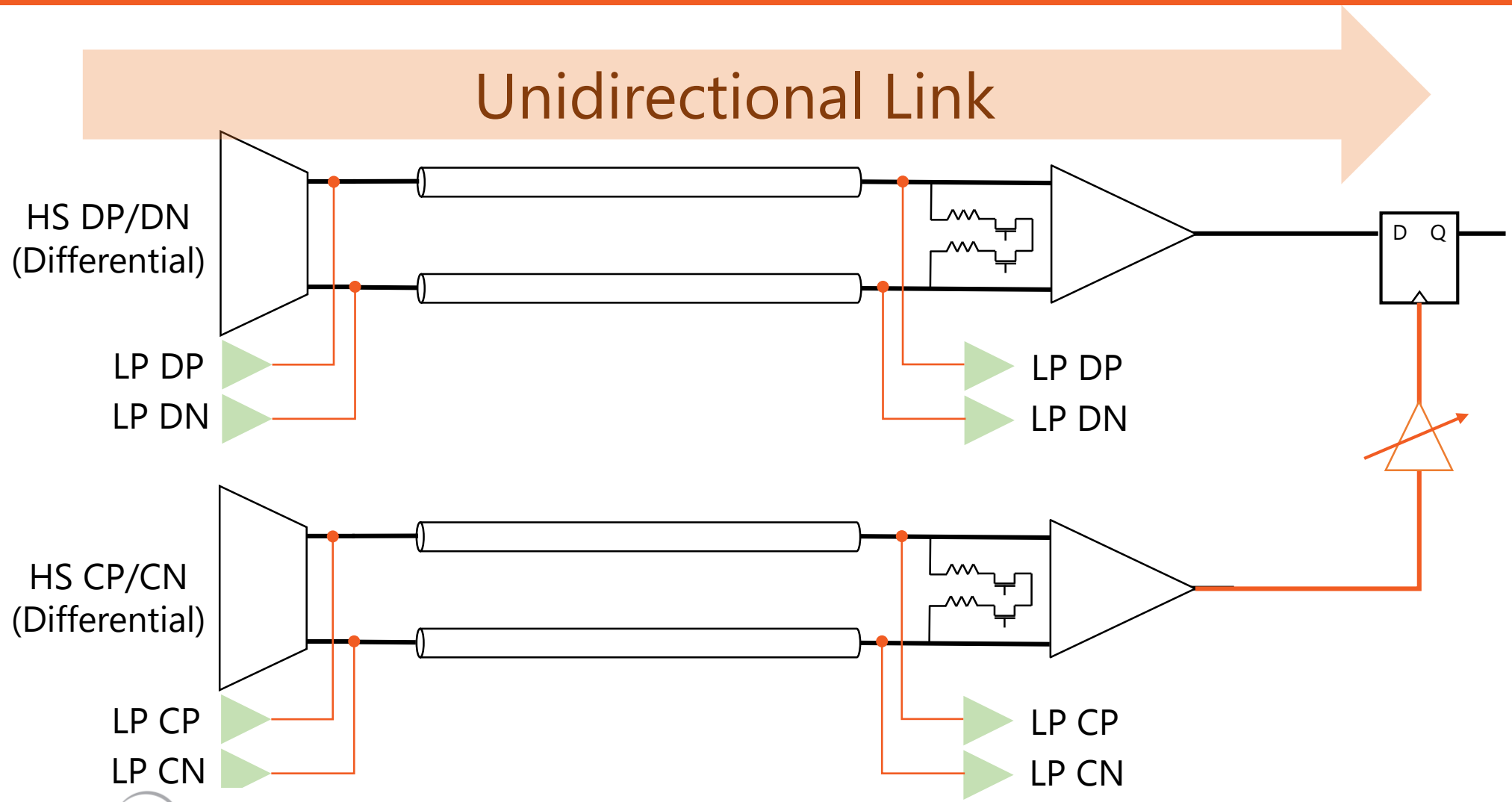
Result of the test can be a photo!

- D-PHY protocol is simple, and it is here to stay for image sensors:
  - User-facing camera
  - Medical imaging
  - Infrared
- C-PHY addresses new trends:
  - High performance imaging (SLR quality)
  - Amenable to vision technologies (LRTE, ROI, fast BTA)

설계와 최적화 과제



Unidirectional Links

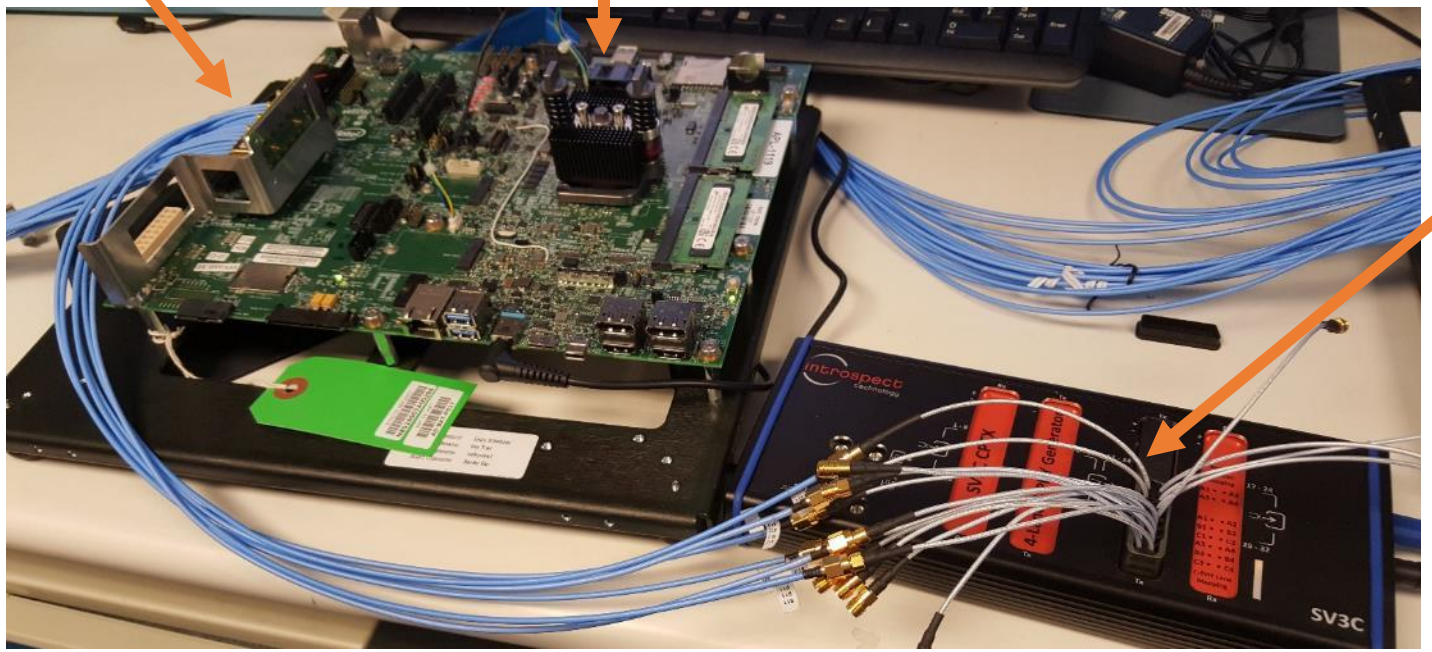


Feedback Through Software (No Loopback)

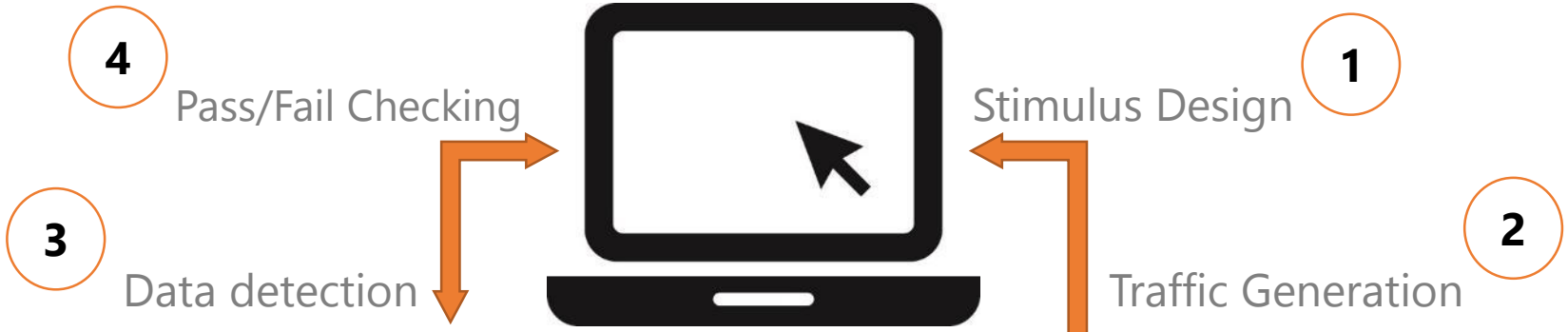
MIPI Input Port

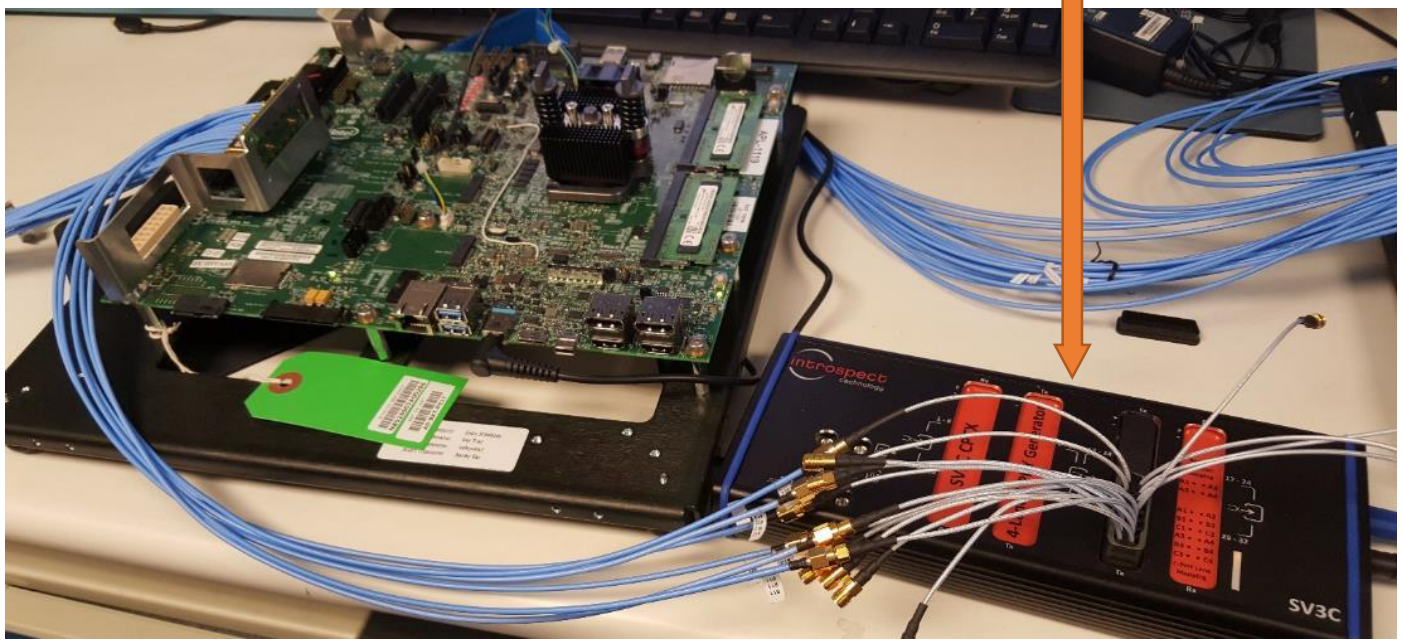
Device Under Test

Only HW connection to APU Under Test is through MIPI Pattern Generator



Feedback Through Software (No Loopback)



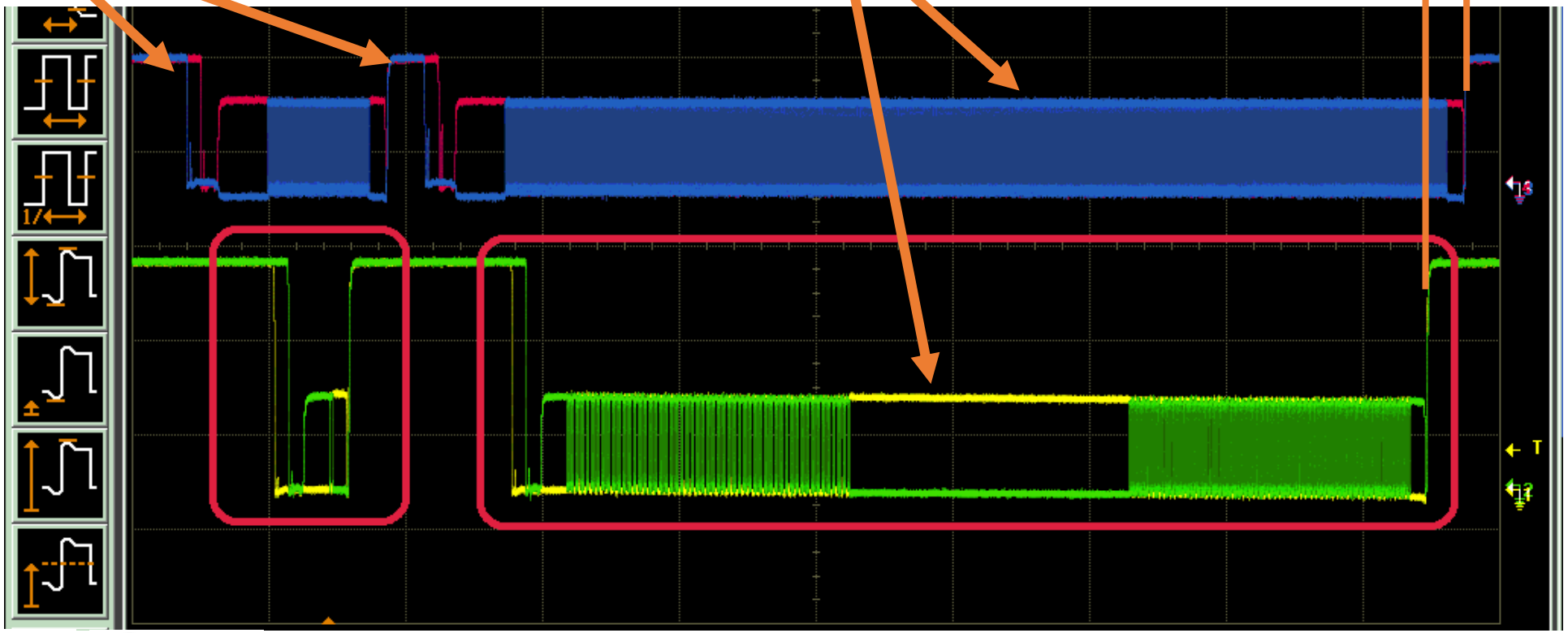


Pattern Generator Waveforms

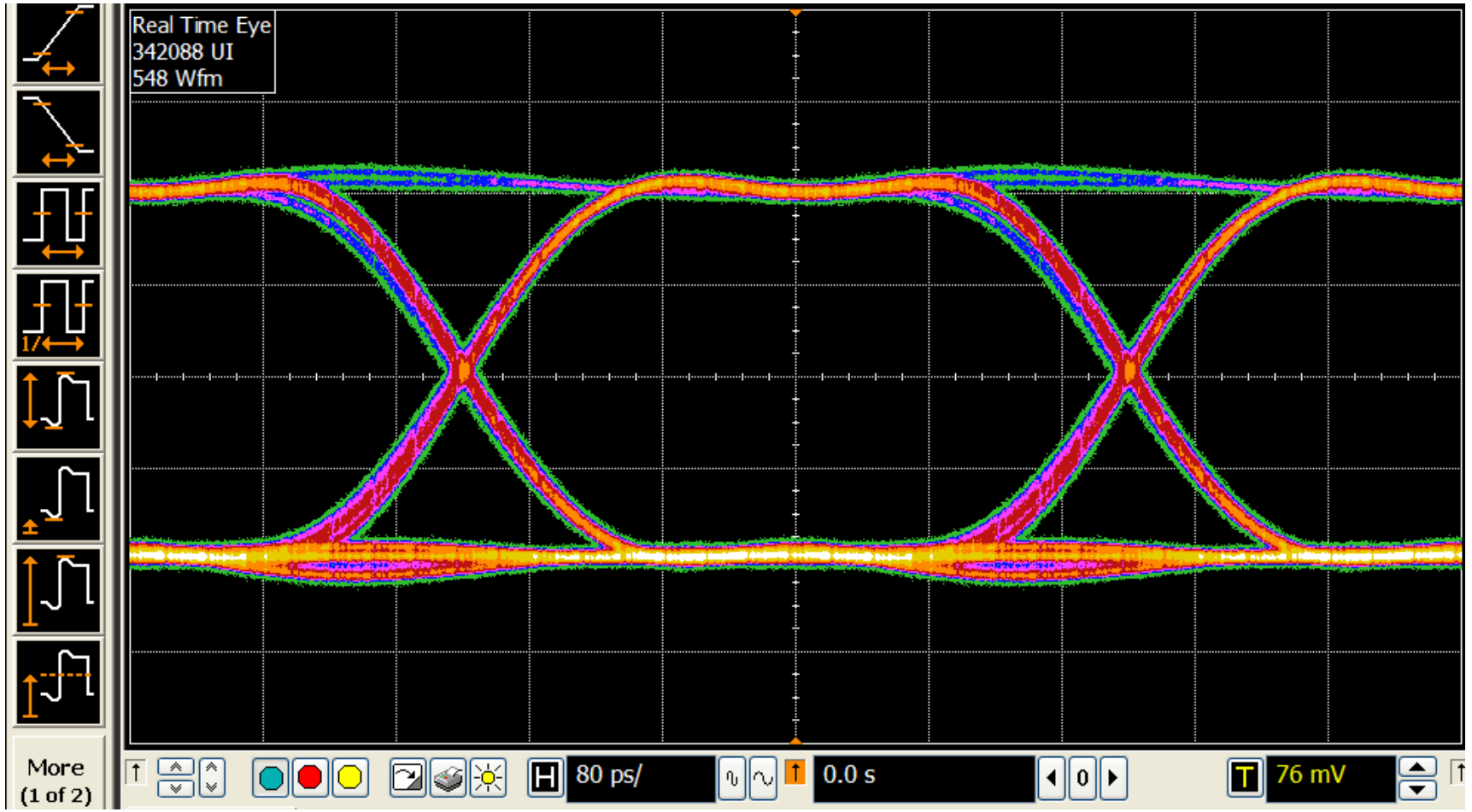
Single-Ended LP Waveforms

High-Fidelity Differential Waveforms

Deterministic Alignment



HS Signal Calibrated Using Conventional Methods



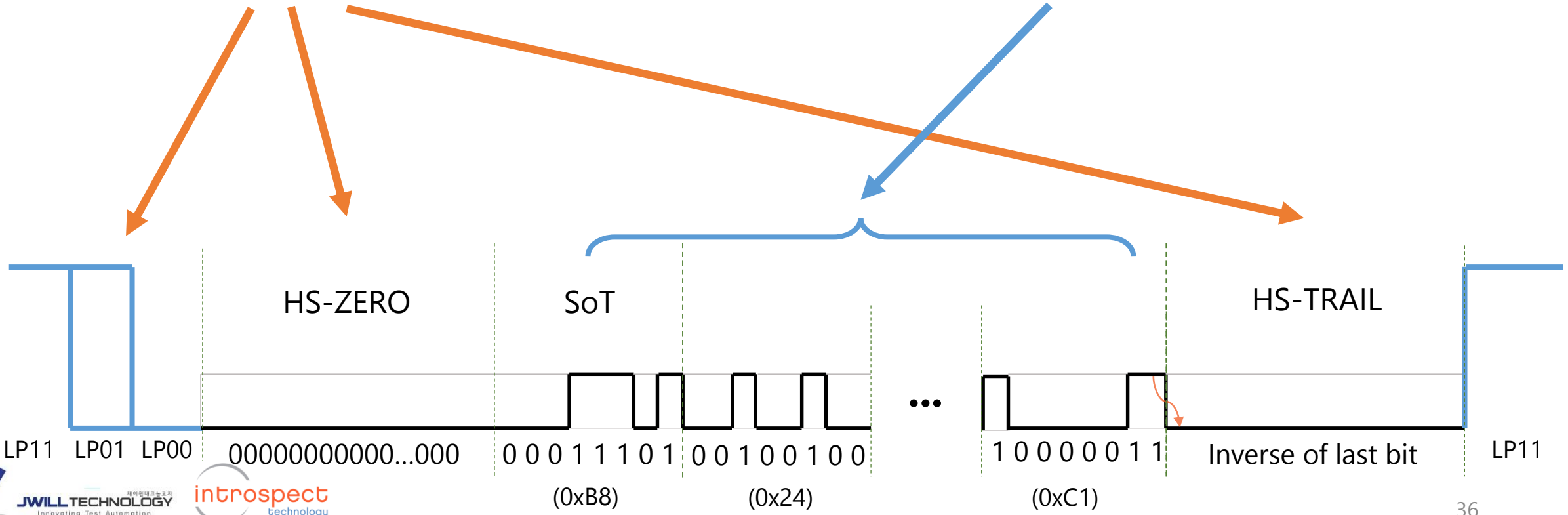
Two Categories of Test Requirements

Global Timers Test

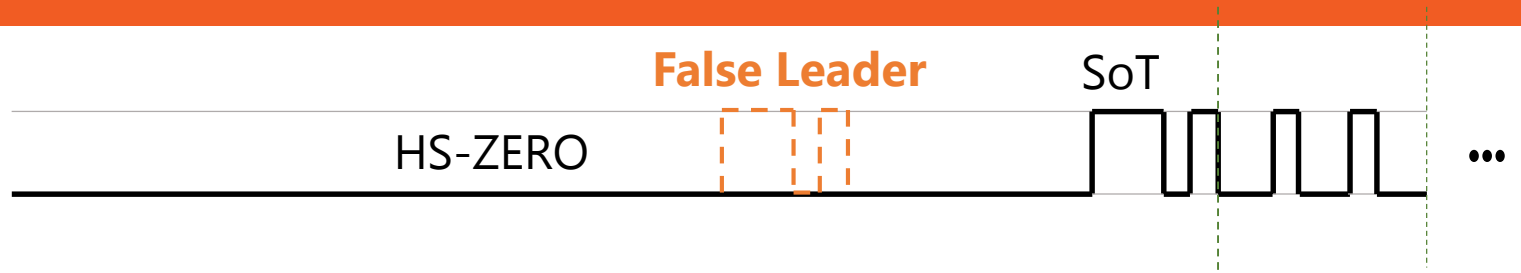
- Stress components related to state transitions from Low Power to High Speed

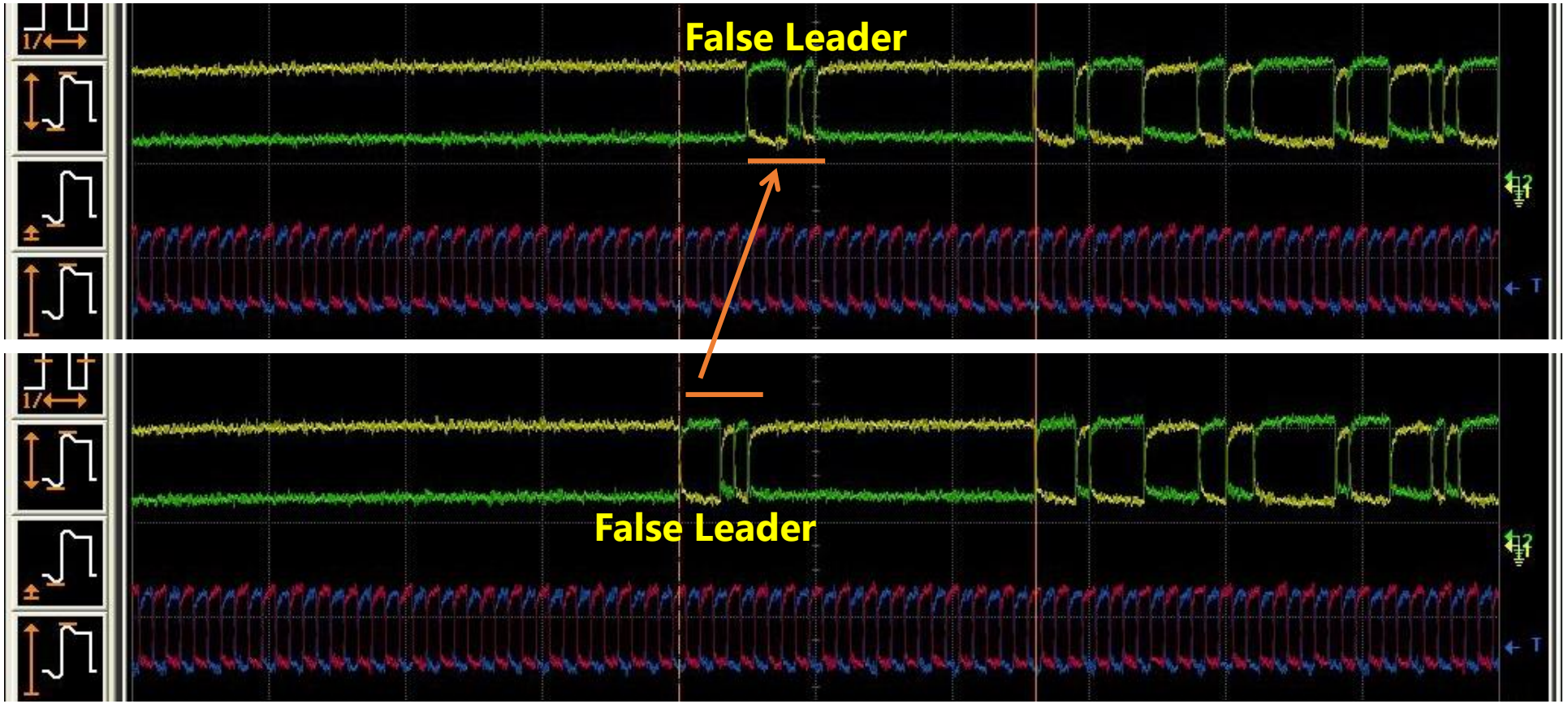
Receiver Eye Test

- Stress components related to the High Speed receiver itself

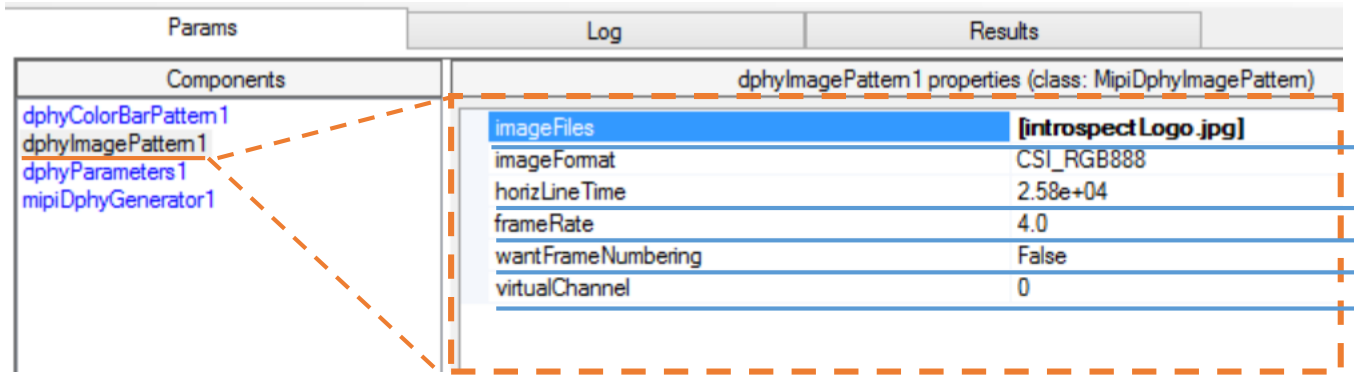


Example CTS Test 2.4.3





Results in Need for Protocol Level Patterns!



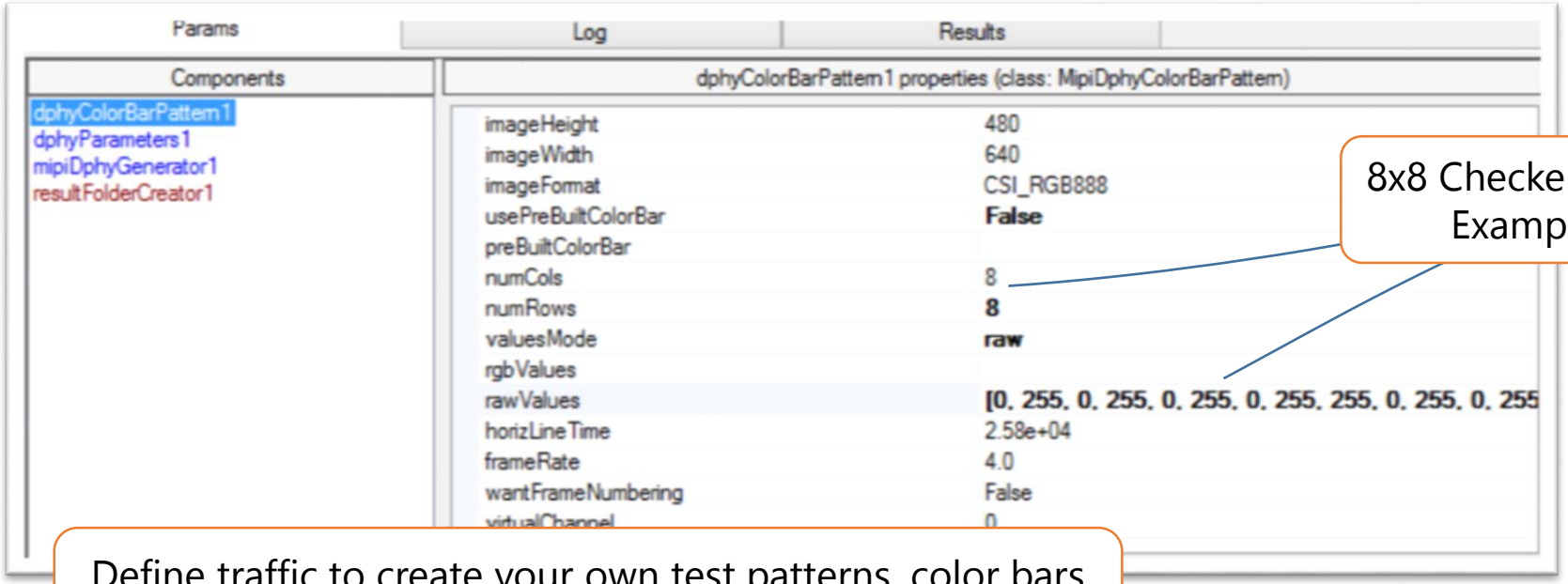
Input picture file from Windows File System

Regardless of test pattern, all frame parameters are configurable

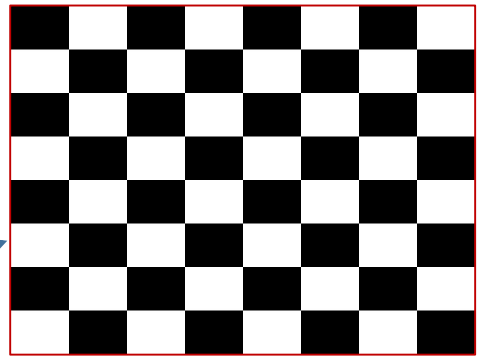
Sample photo being transmitted

Practical Tip: Use Color Bar Pattern Generator!

A color bar is an algorithmic pattern generator that allows you to very quickly generate MIPI D-PHY or C-PHY traffic

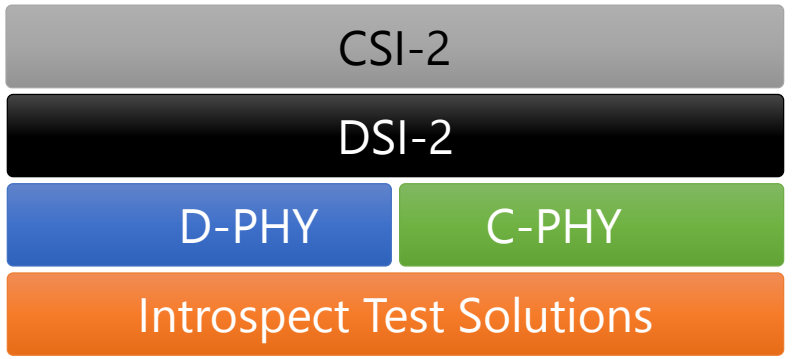


8x8 Checkerboard Example



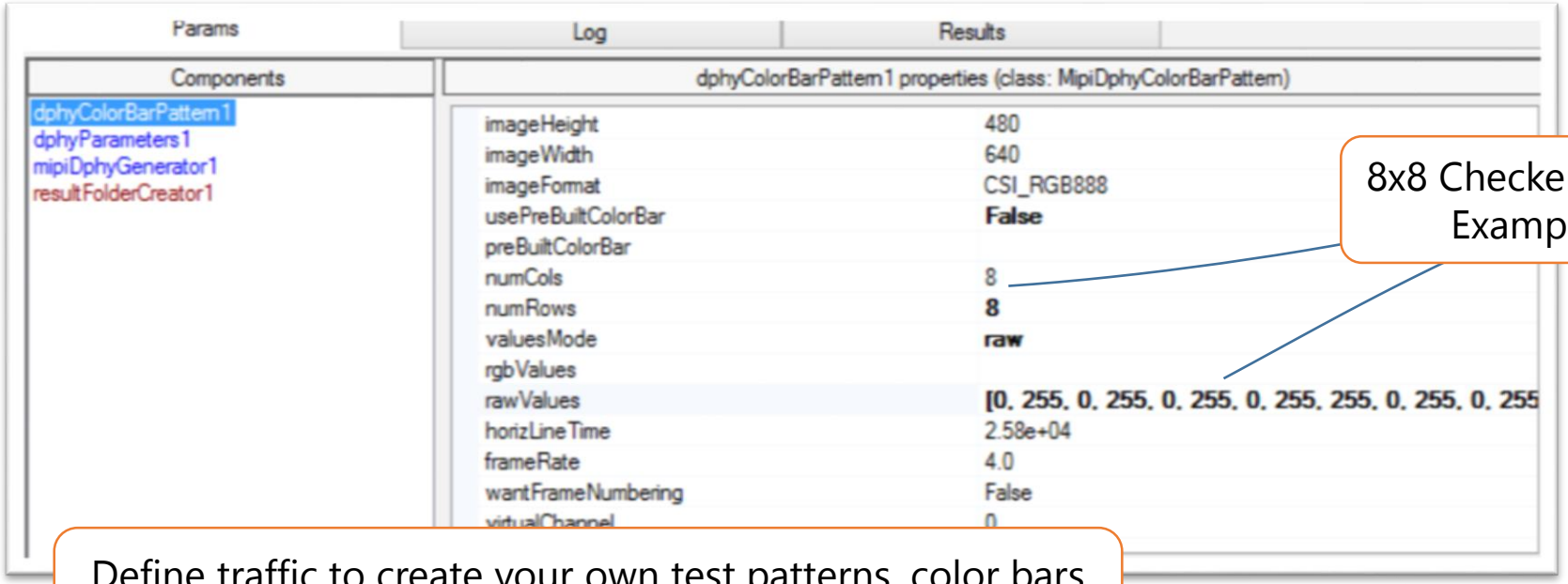
Software-generated preview

Define traffic to create your own test patterns, color bars or your even own protocol layer

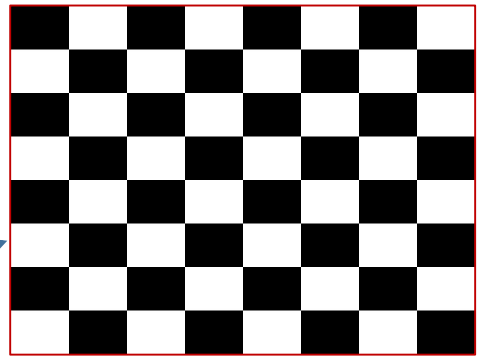


Practical Tip: Use Color Bar Pattern Generator!

The Introspect tool allows you to also define your own protocol, controlling every bit that is transmitted over the wires

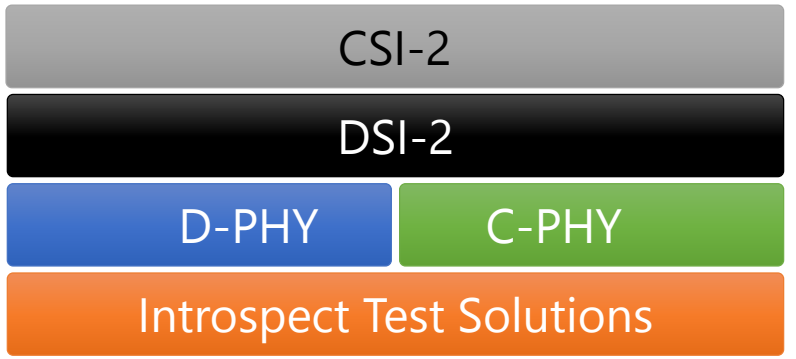


8x8 Checkerboard Example



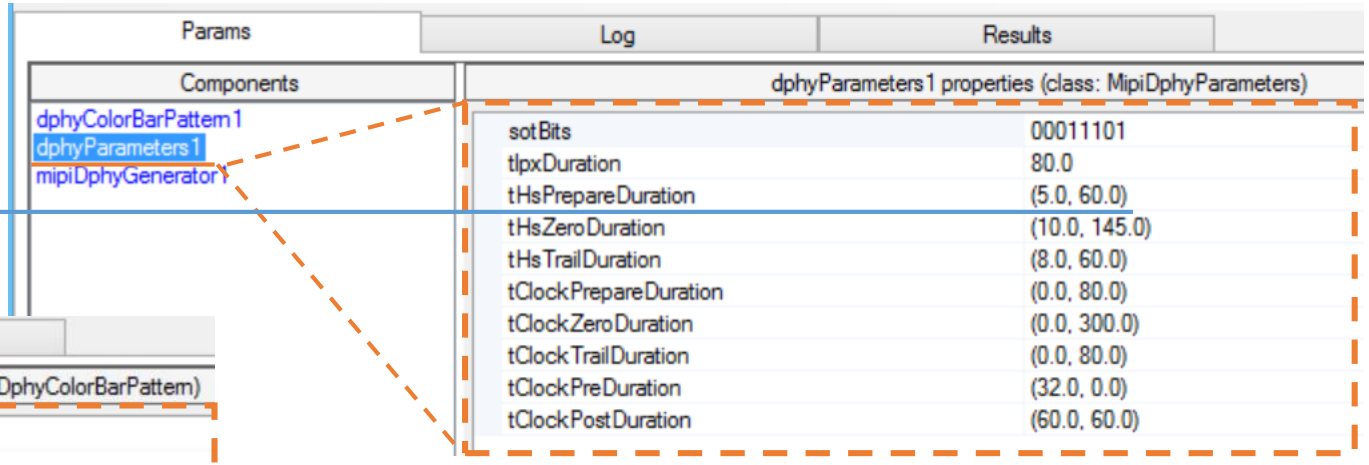
Software-generated preview

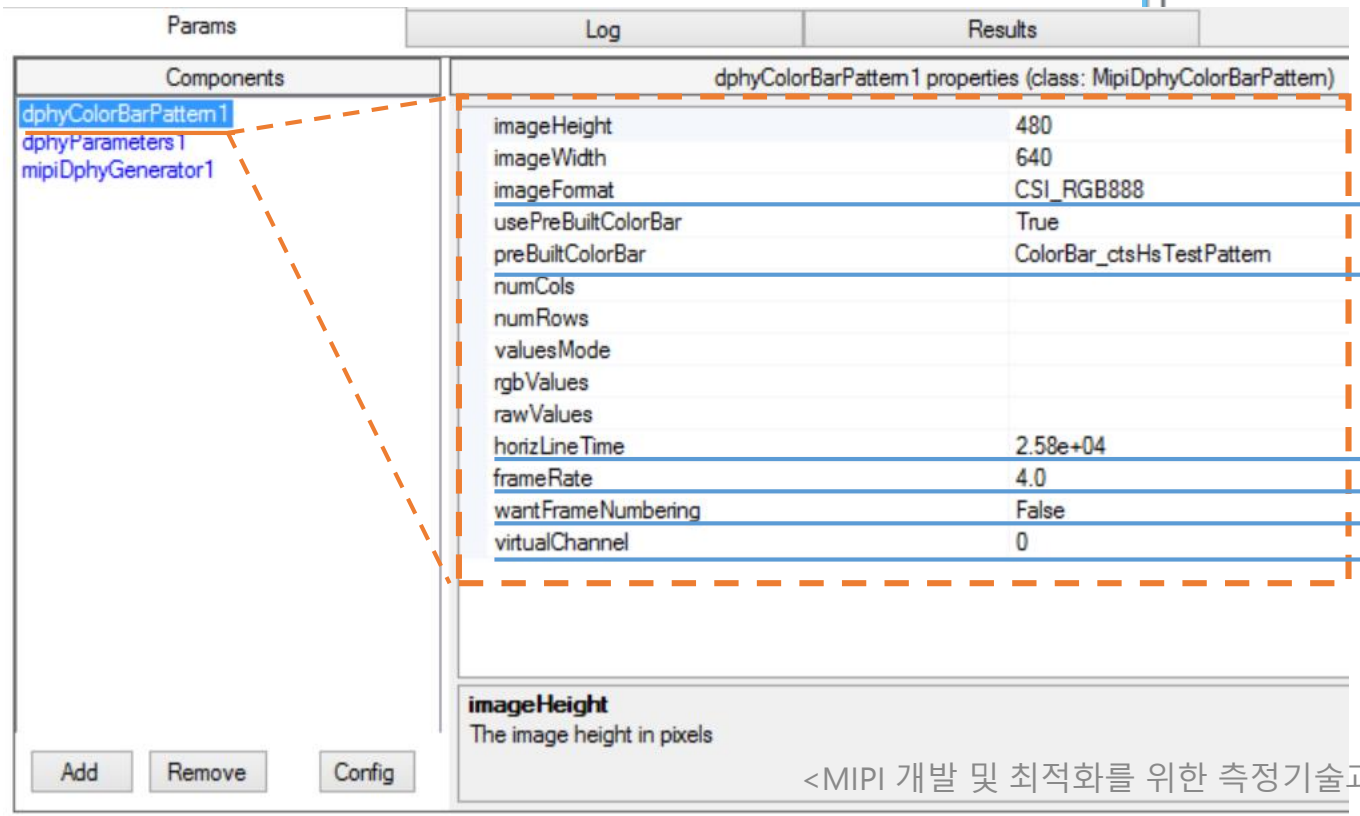
Define traffic to create your own test patterns, color bars or your even own protocol layer



While Controlling Analog Parameters

Global timing parameters are included in units of UI and nanoseconds. SOT bits need to be configurable





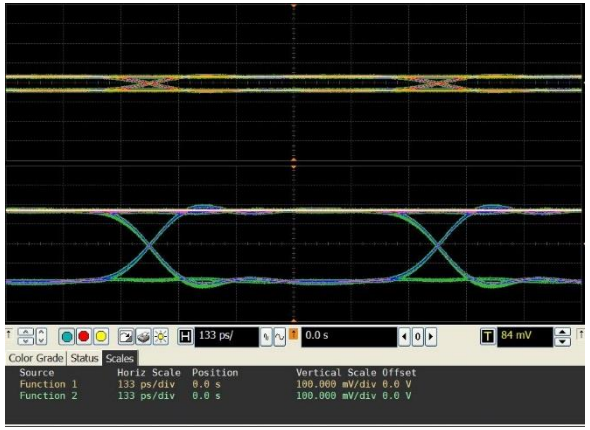
dphyPattern component shown here as a color bar generator. Frame height & width are included as well as selection of Pixel format (CSI-RGB888 shown)

Standard test color bar included by default

Regardless of test pattern, all frame parameters need to be configurable

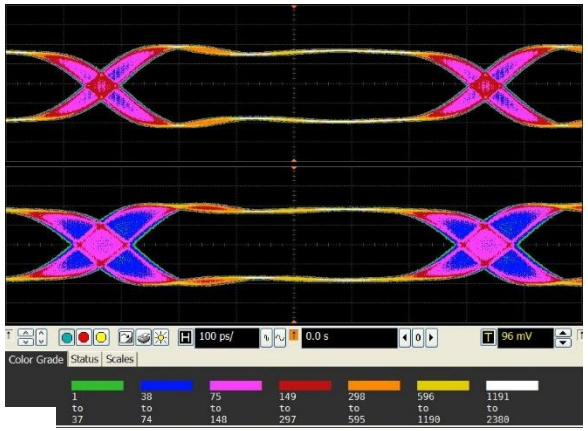
Signal Calibration Very Similar to Other SerDes

Voltage Amplitude

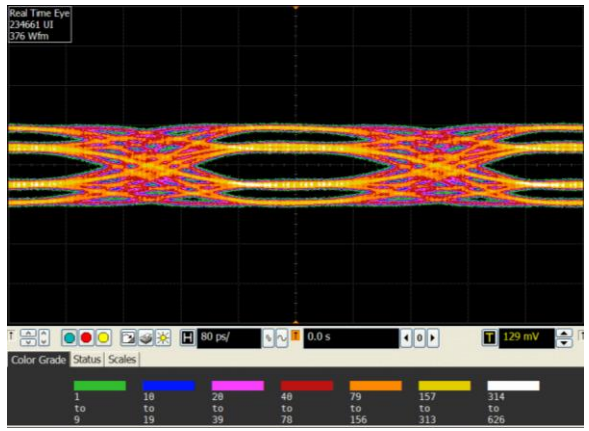


Common Voltage

Jitter Injection



Timing Stress



Real World Tips

When things really need to get done…

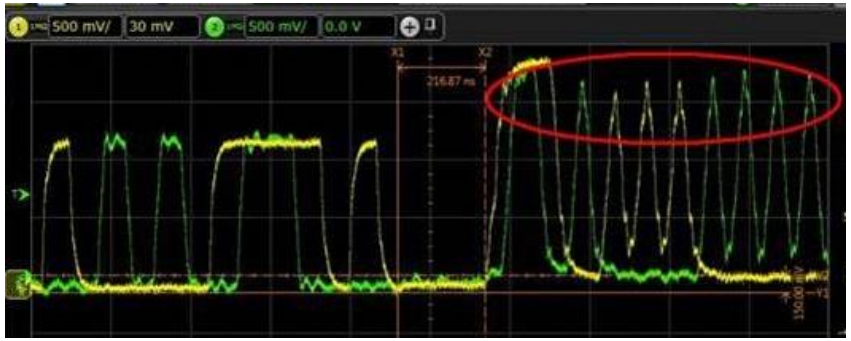
Avoid Long Cables

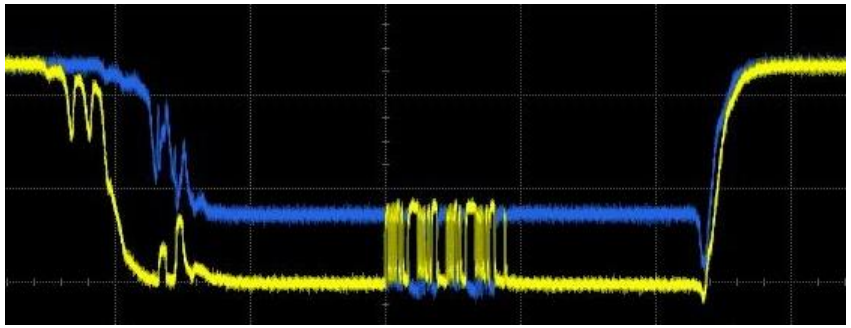
LP signals are unterminated

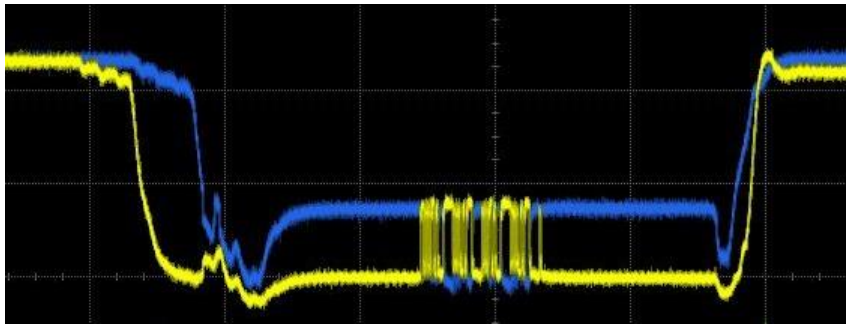
Reflections

LP to HS transition includes switching termination

Charge injection, ringing

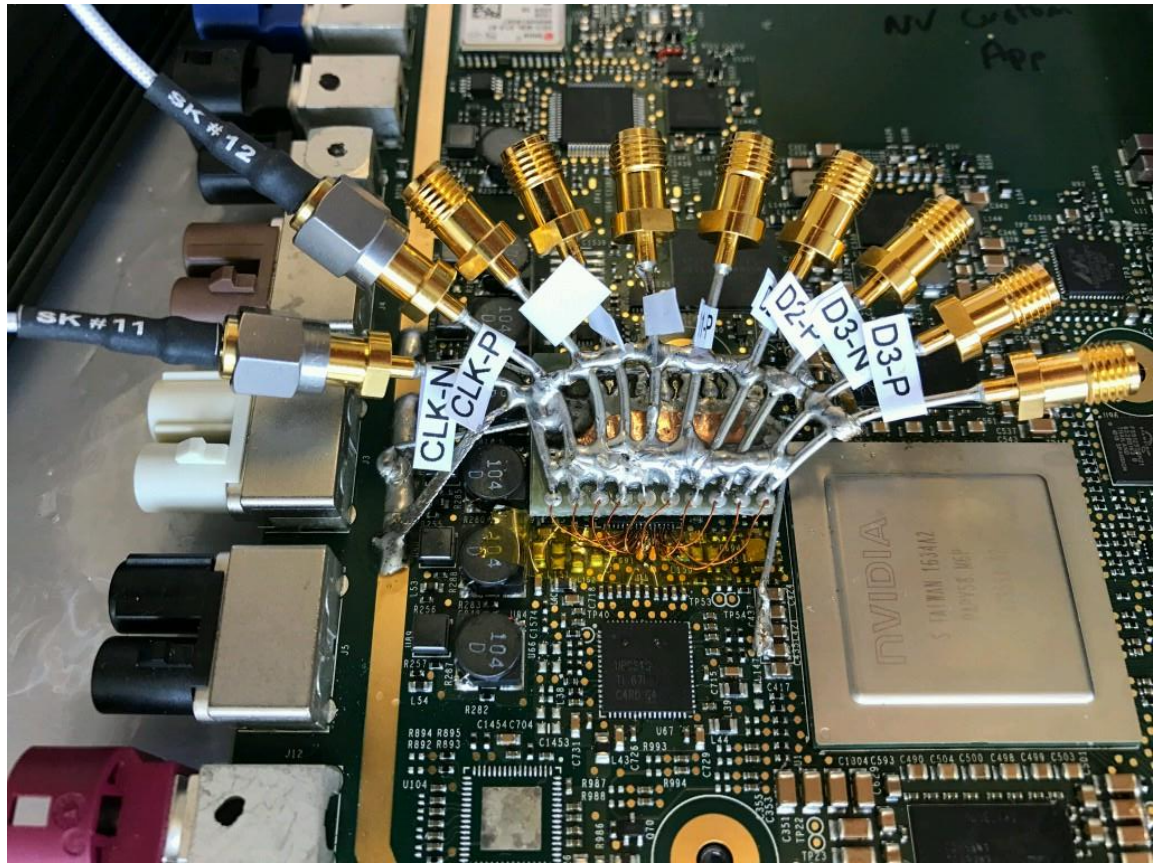






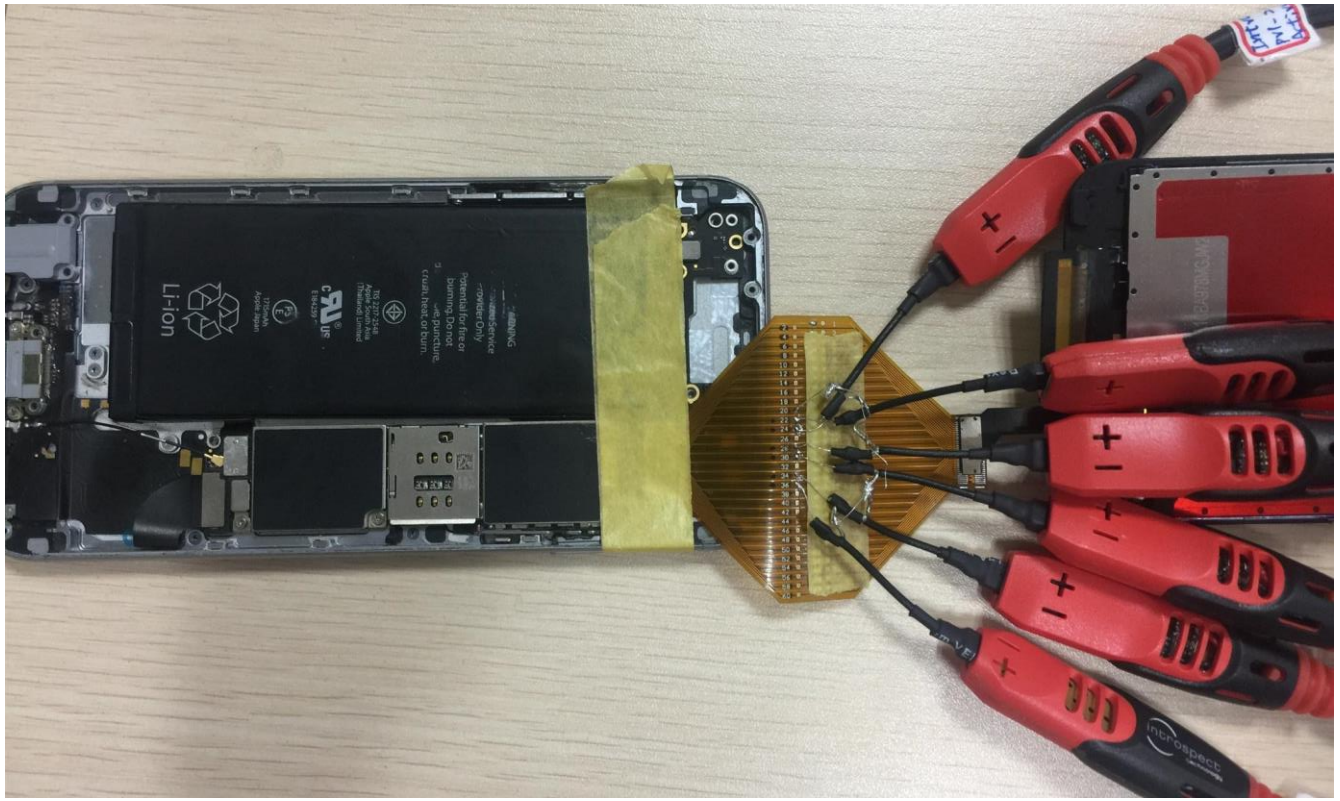
Passive Probes Do not Always Work Well!

Loading the HS lines means that load seen by Tx is no longer 50 Ohm

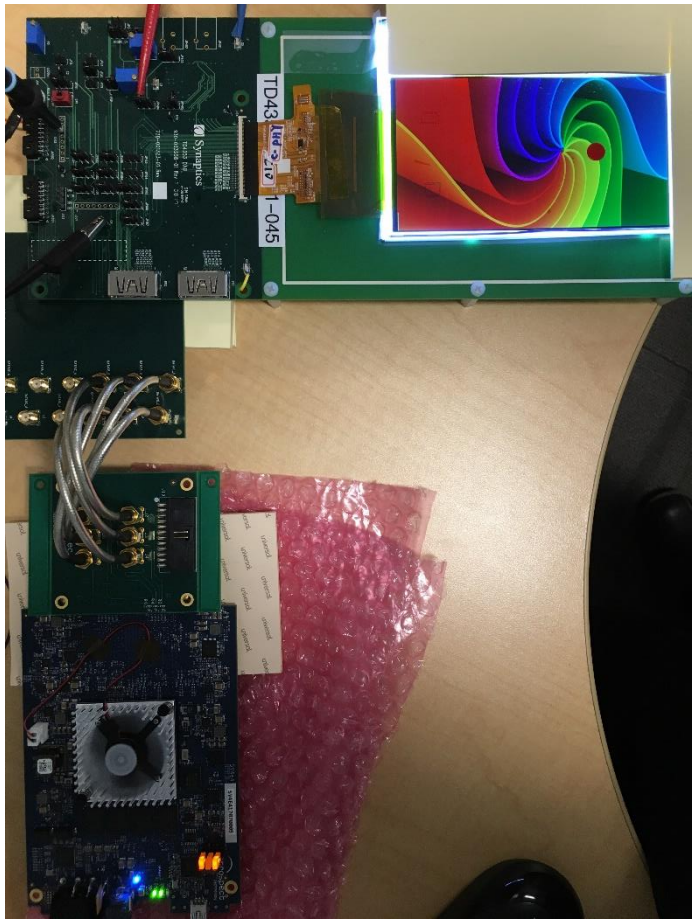


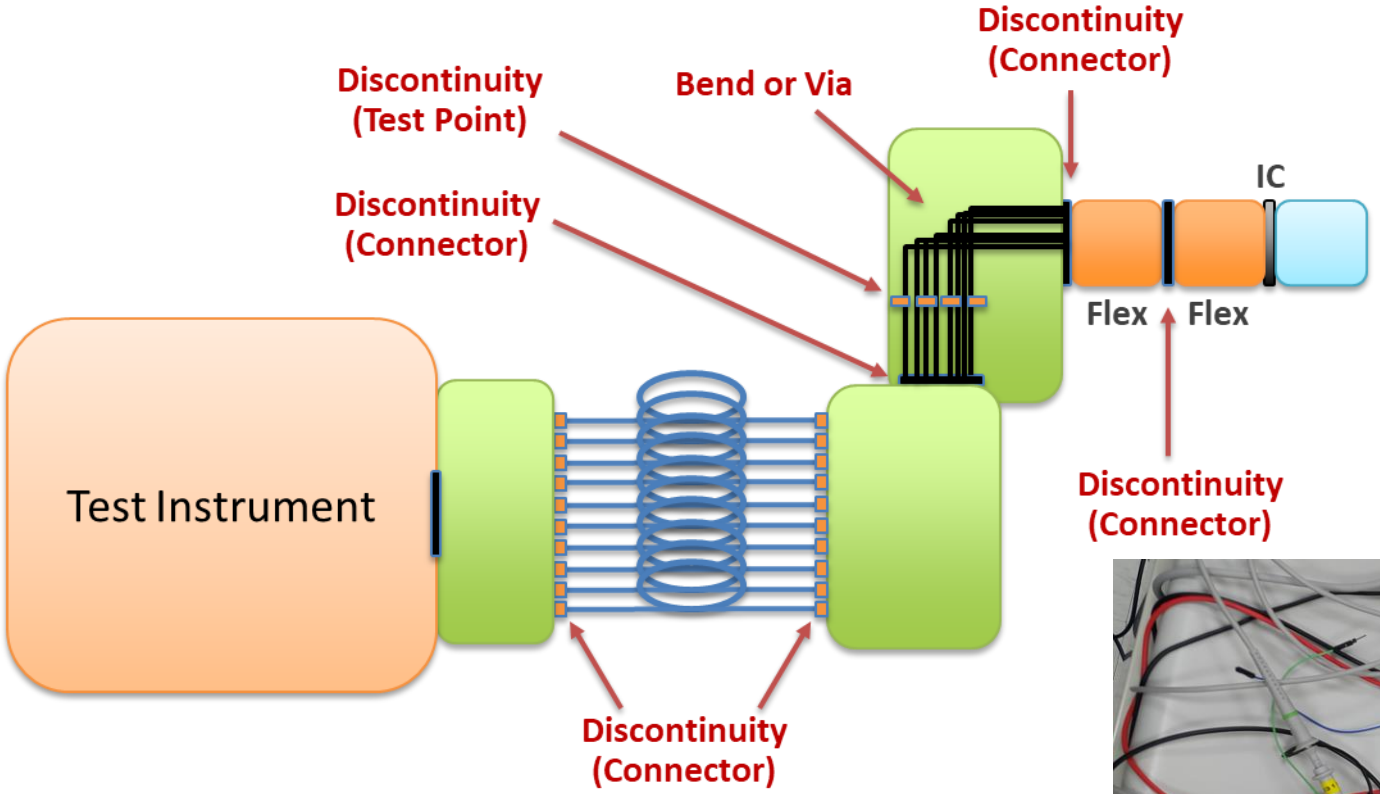
Instead, Use Active Probes!

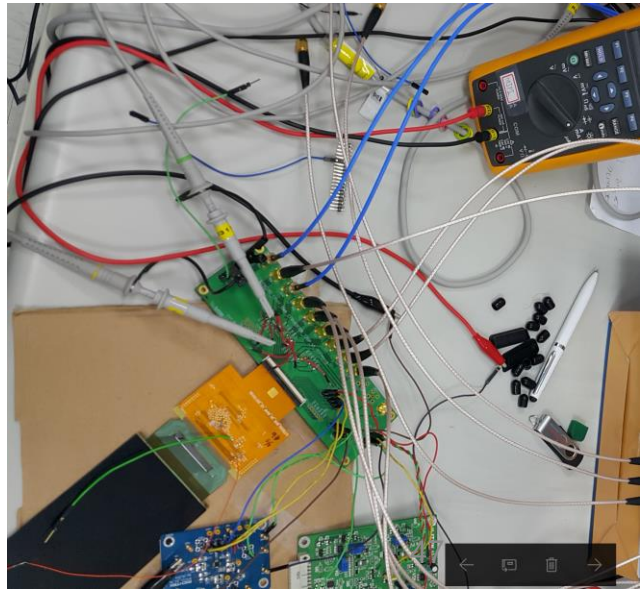
Illustrating how to use active probes to measure a live iPhone



Beware of the Discontinuities







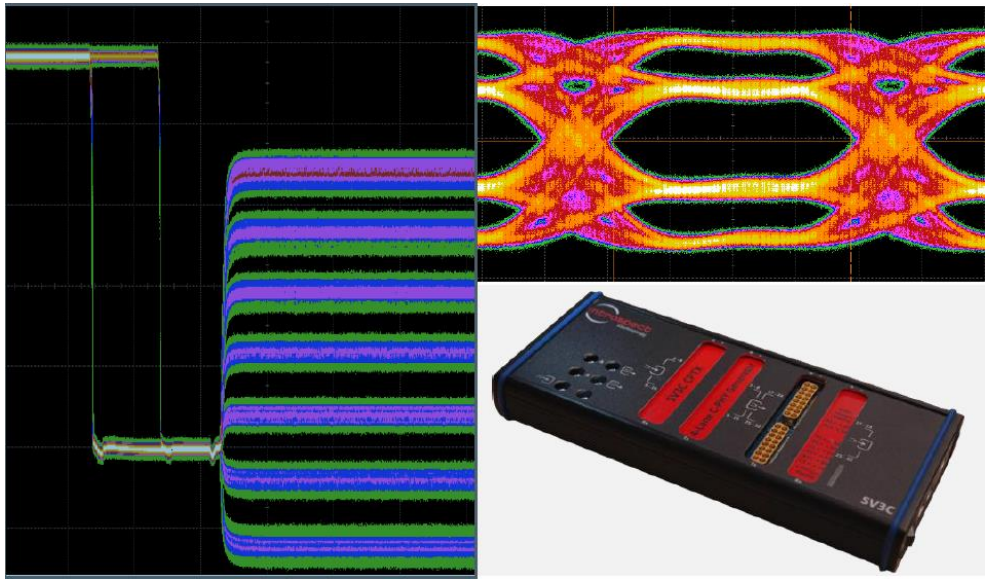
Beyond Mobile… Beyond 1 Lane… Beyond 1 Protocol

Key Takeaways

Limit cable lengths

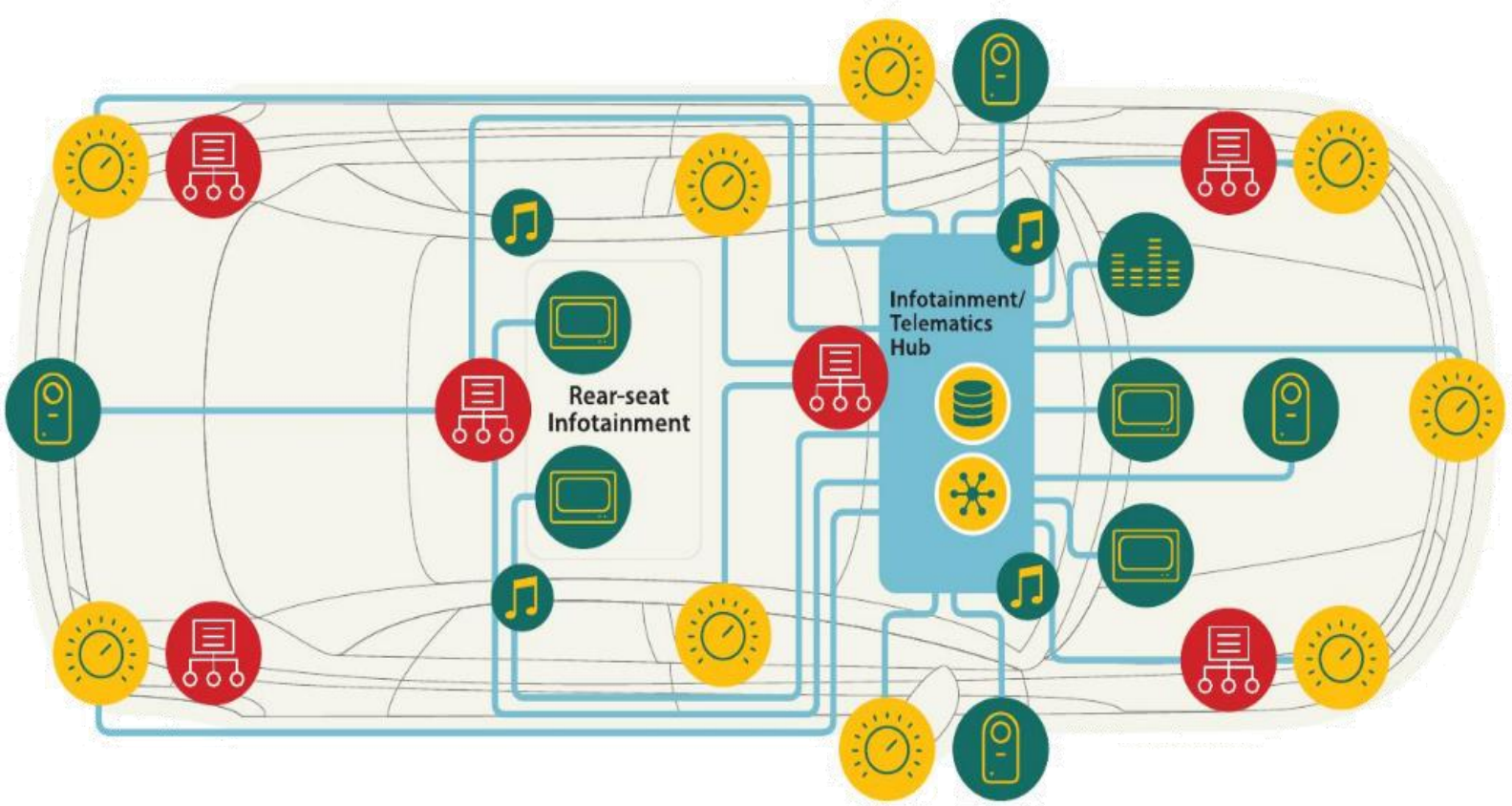
Avoid probing with passive signal taps

Ensure all-lane testing, but avoid discontinuities

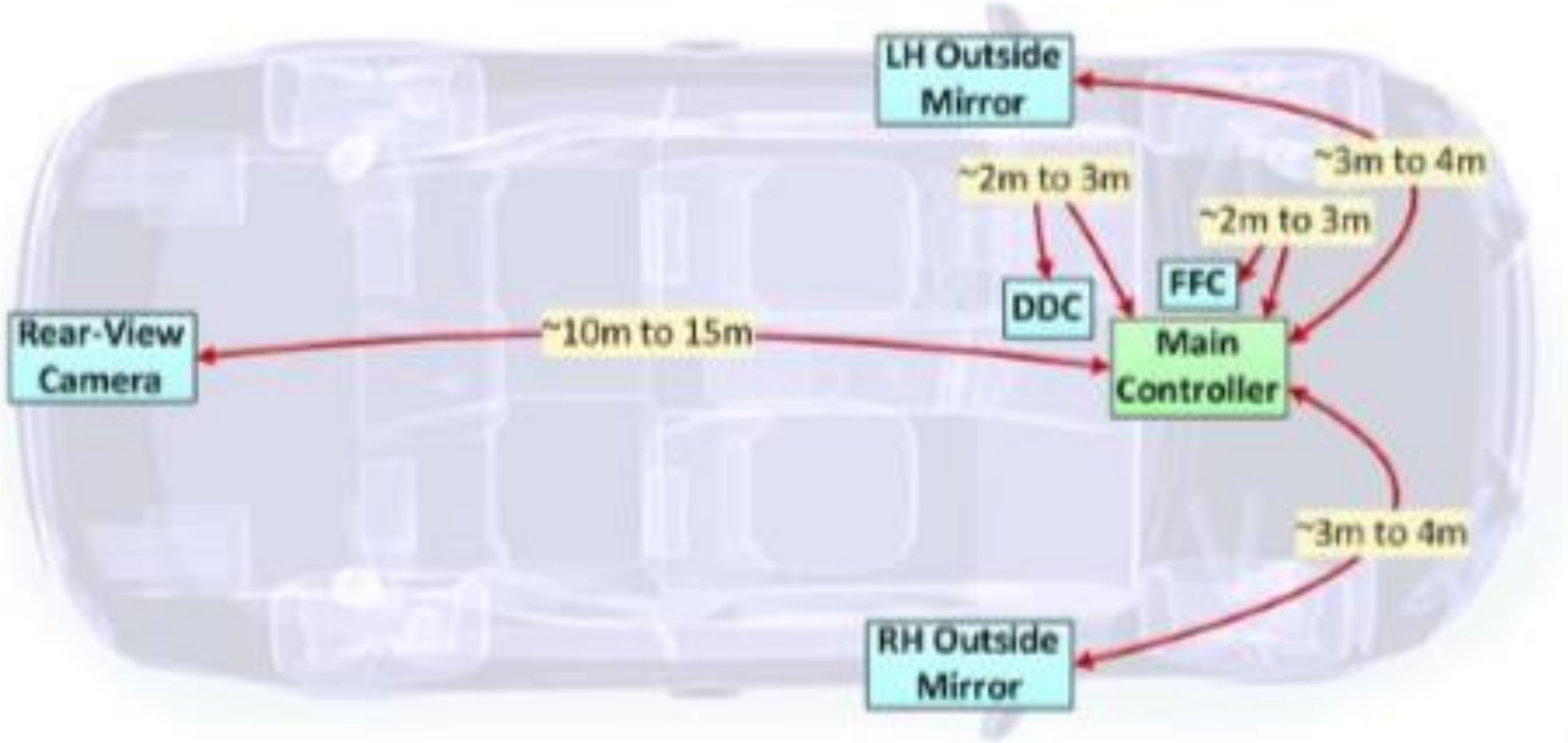


응용사례 연구
- MIPI Testing in ADAS -

Application Spotlight: ADAS

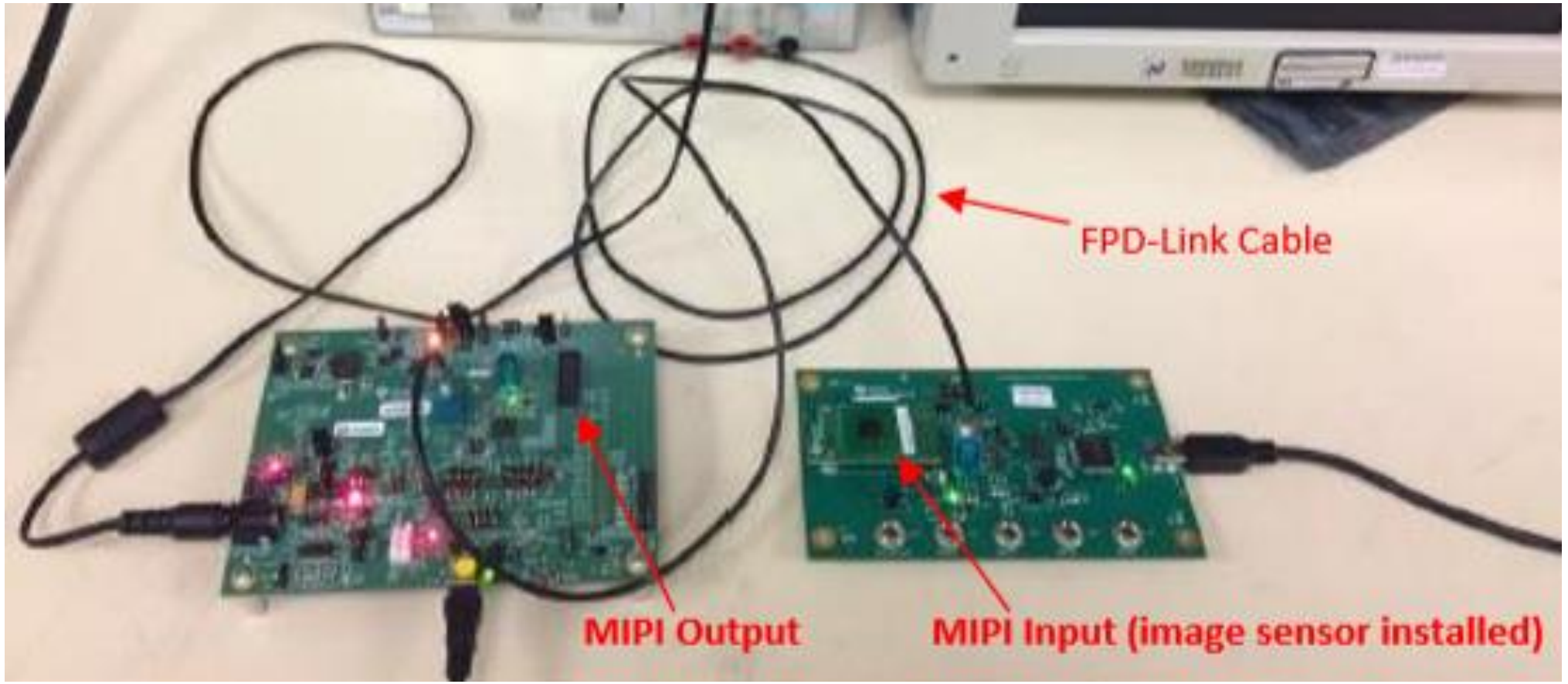


Auto SerDes Links in ADAS Systems



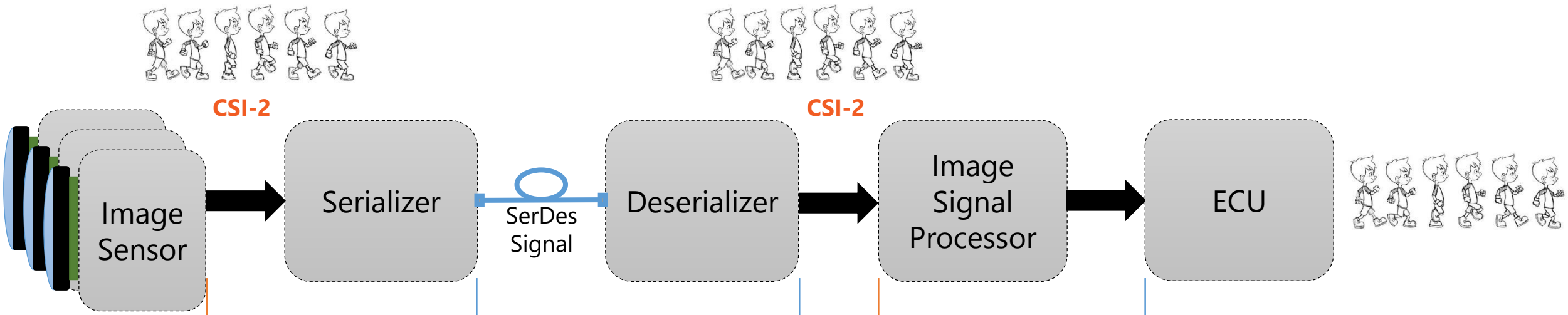
AutoSerDes links are used in ADAS systems to drive long cables (Source: MIPI Alliance)

Auto SerDes Links in ADAS Systems



FPD-Link III sub-system block diagram under test

Anatomy of an ADAS Sensor System



From mobile technology; increasing resolution and bandwidth

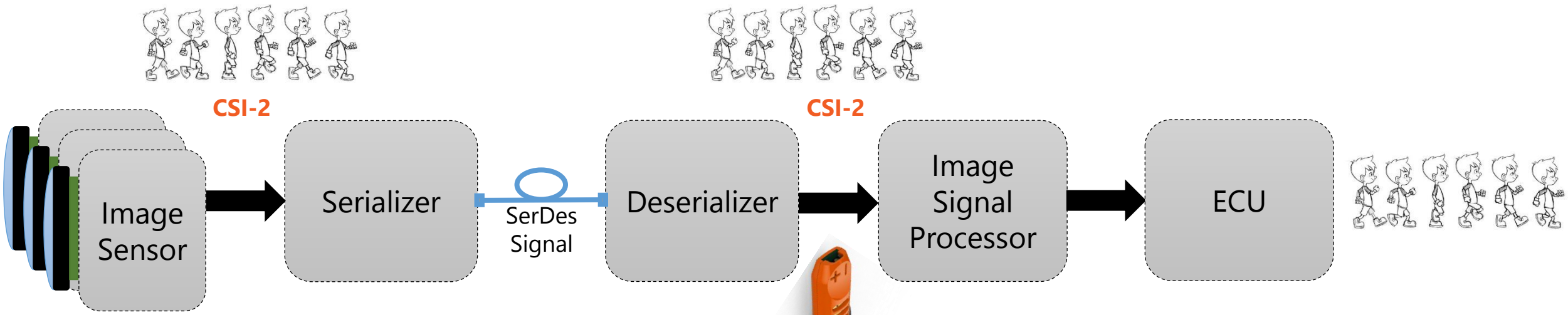
Proprietary technology for driving long cable in harsh environment

Proprietary technology for receiver over long cable in harsh environment

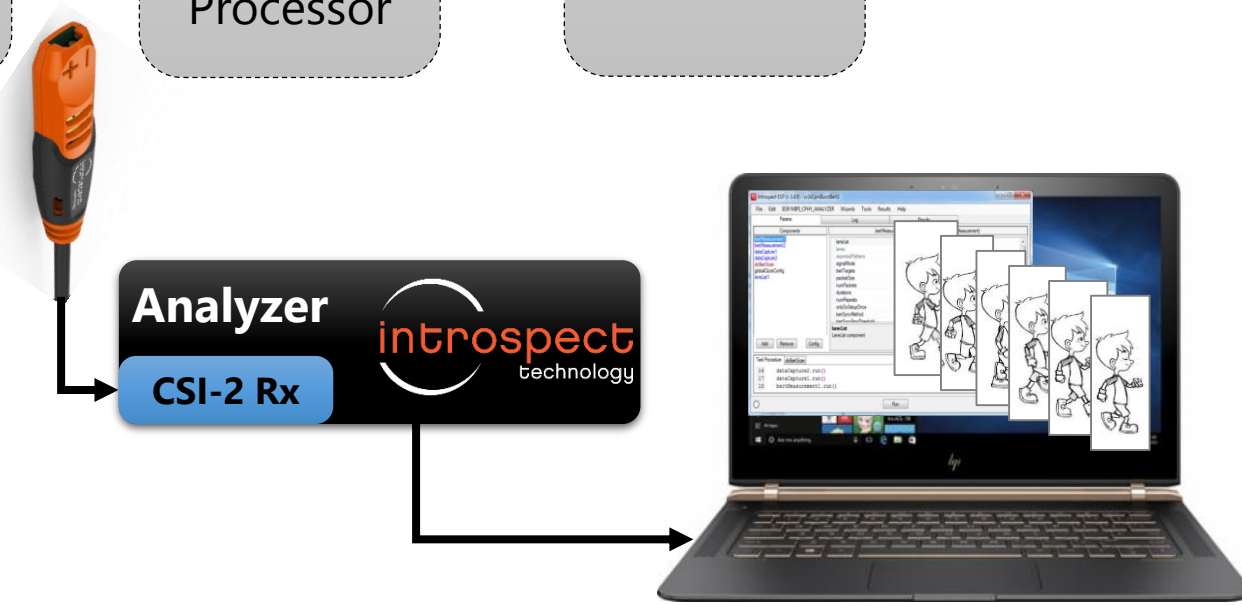
CSI-2 receiver just like the one found in smart phones; typically contains many links!

Extends processing from ISP; performs large computing tasks and redundancy checks

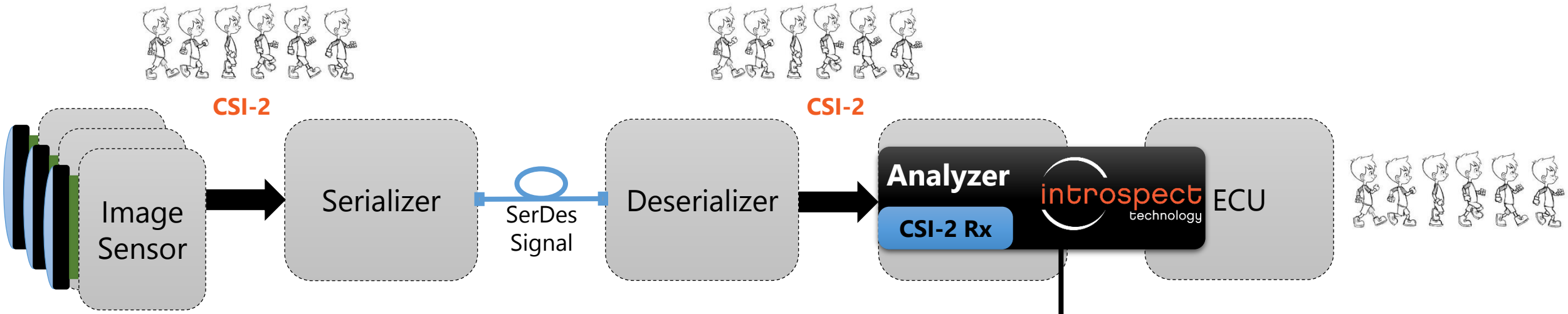
Test Scenario #1: Live Link Probing



- Check for proper reception of frames from multiple sensor streams
- Verify design configurations (e.g. data type, virtual channel, interleaving, scrambling, compression)
- Verify signal integrity effects (e.g. CRC errors)
- Perform system-level stress testing (e.g. cold/hot temperature functionality)

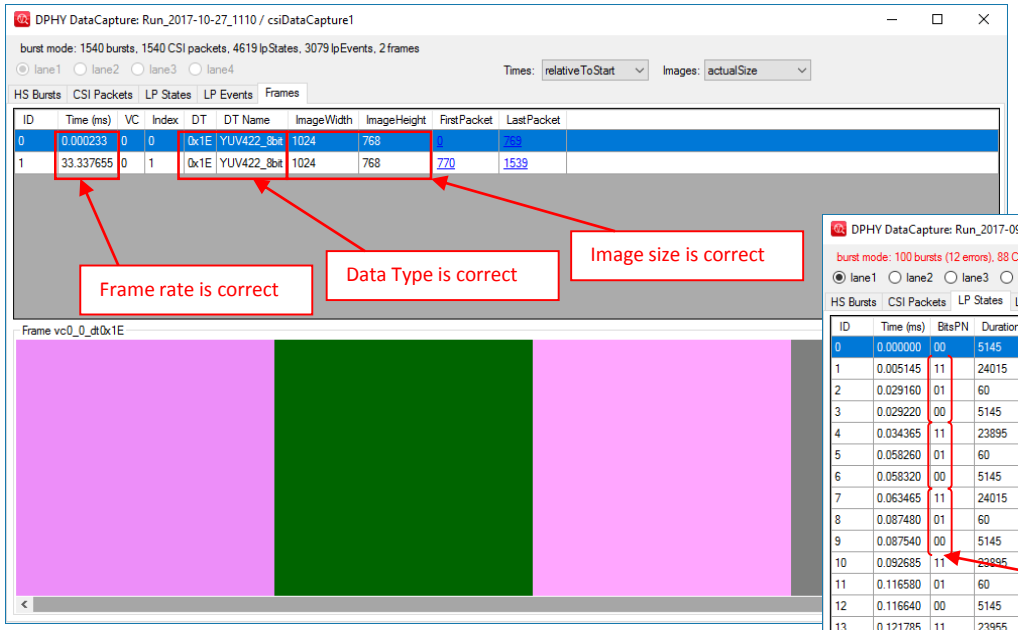


Test Scenario #2: Deserializer Verification



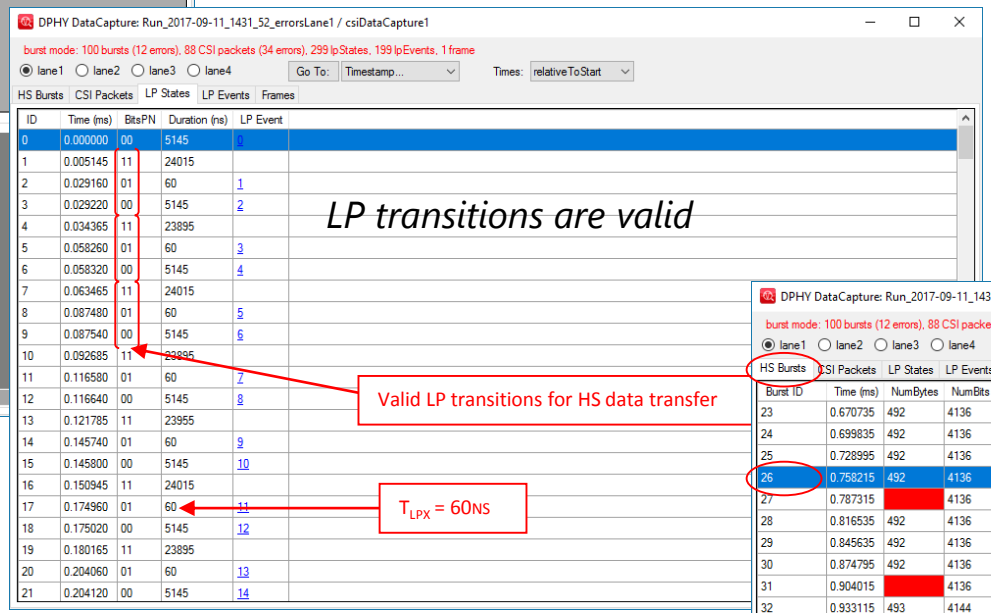
- Similar to live testing, but now focus on the deserializer output directly
- Perform characterization or global timing measurement by controlling the deserializer I2C bus and sweeping it through its analog parameter range

Test Results for Test Scenarios 1 & 2



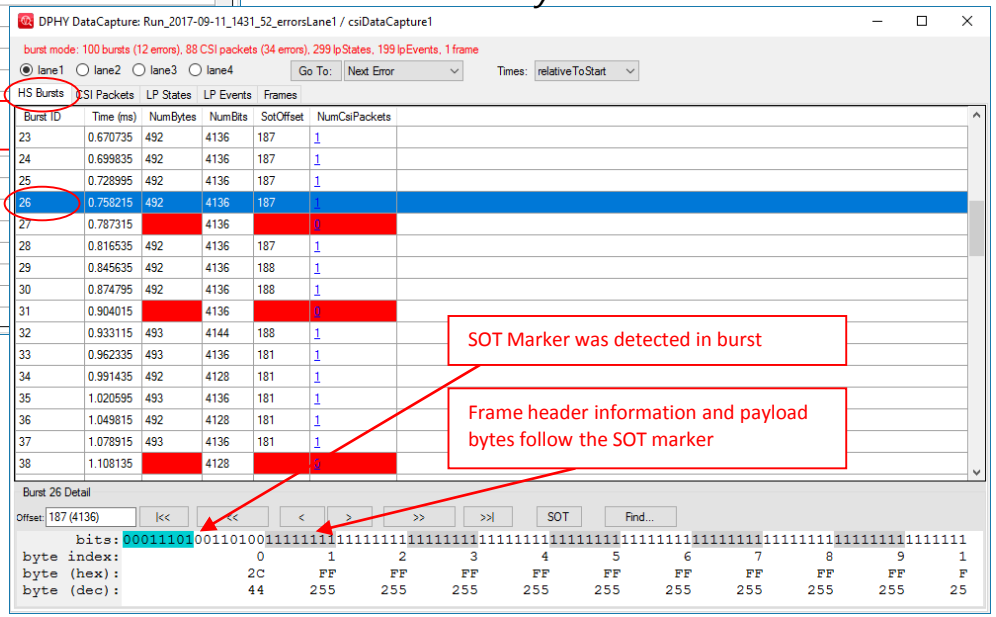
Valid capture with no errors

LP transitions are valid

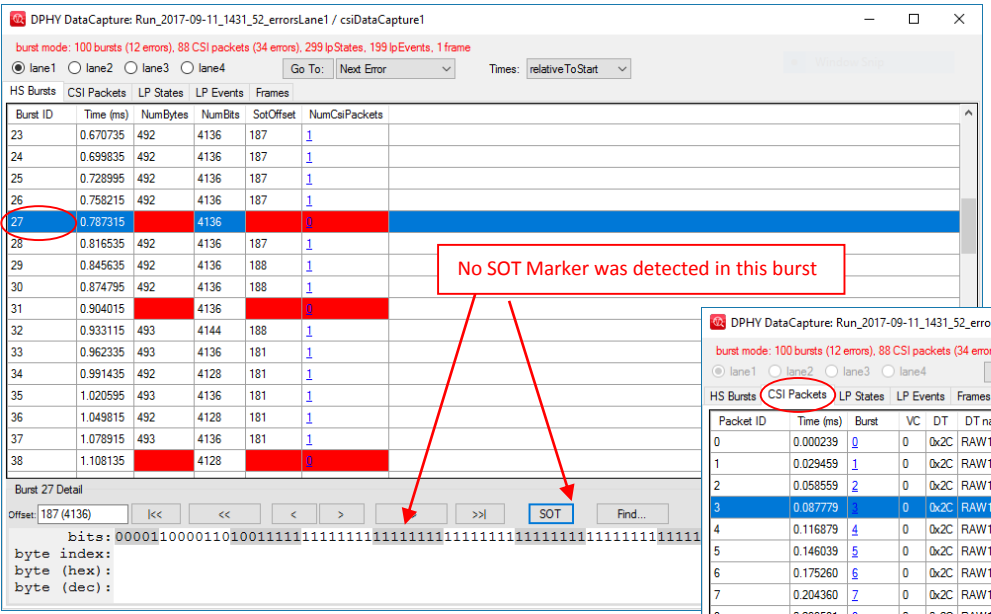


LP transitions are valid

Errors visible at the physical layer. Burst #26 has no errors

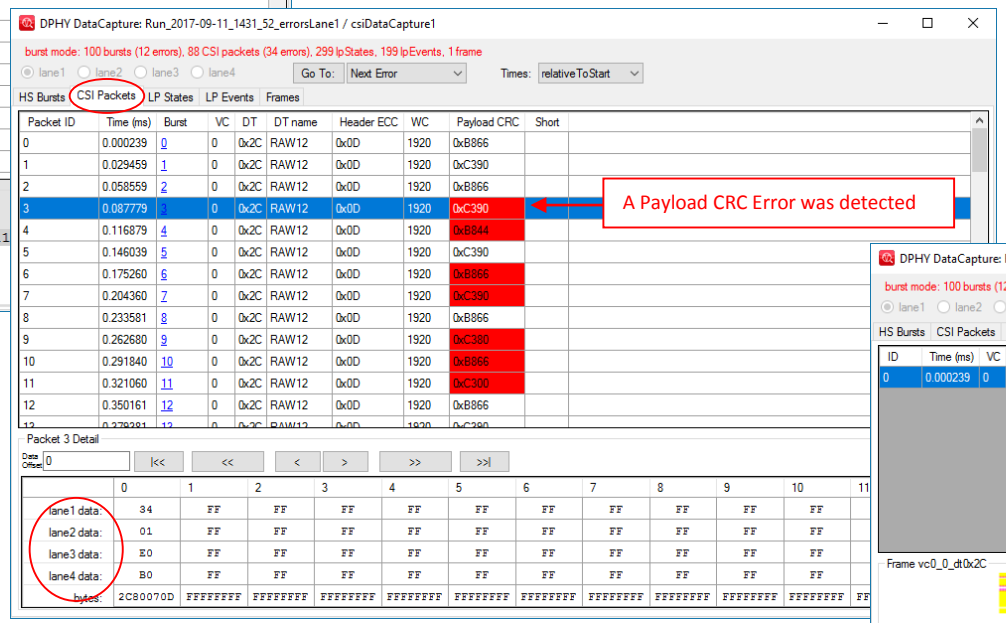


Test Results for Test Scenarios 1 & 2

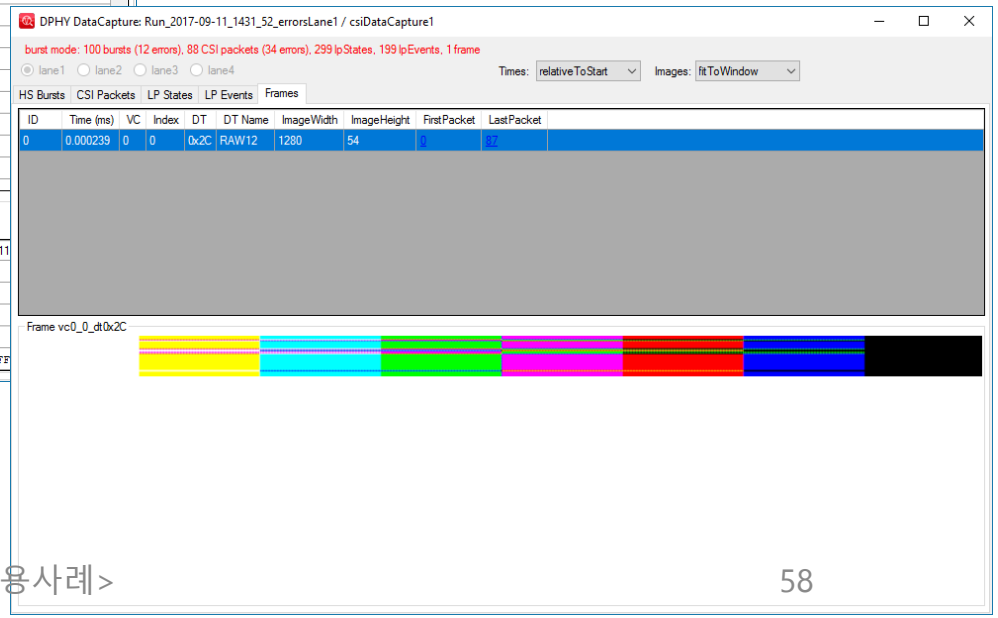


But burst #27 has a lot of errors.
There is no SOT marker

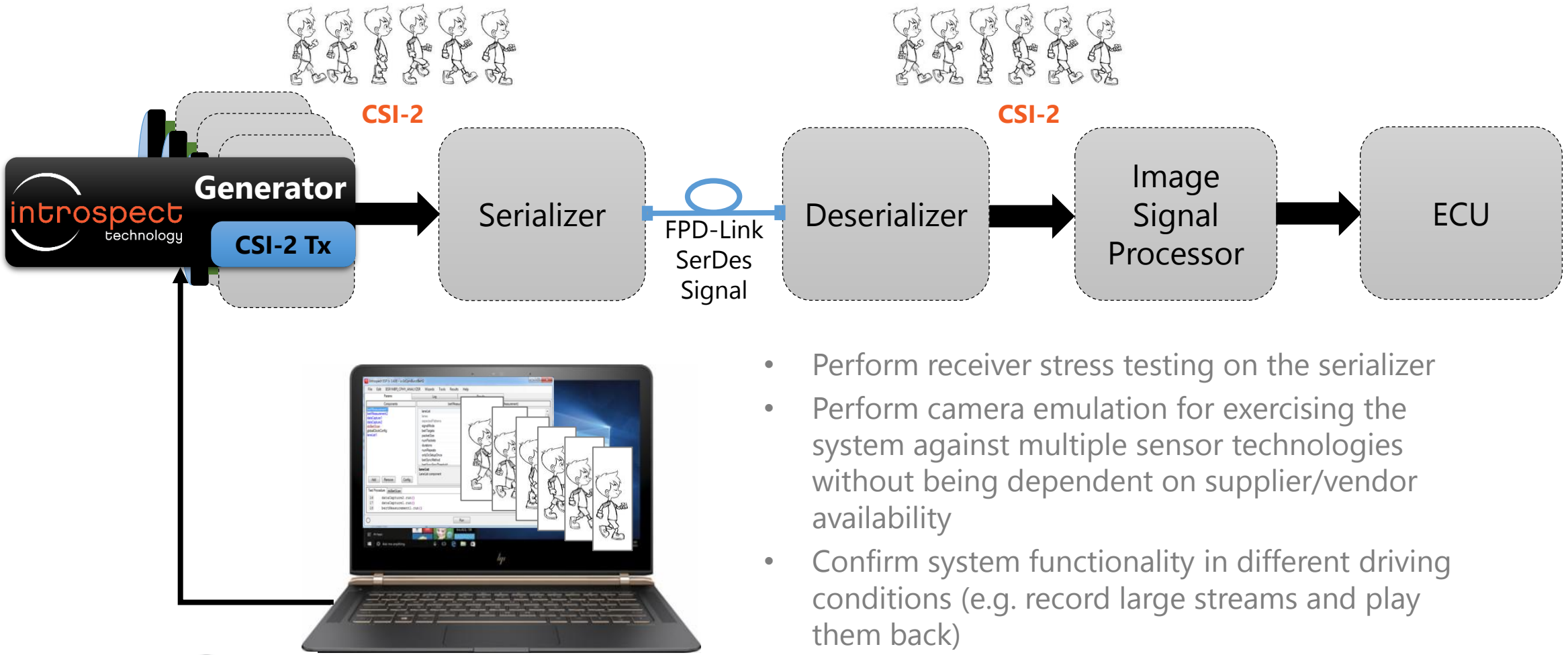
CSI-2 packet view reveals other CRC errors



Reconstructed frame shows many pixel artefacts

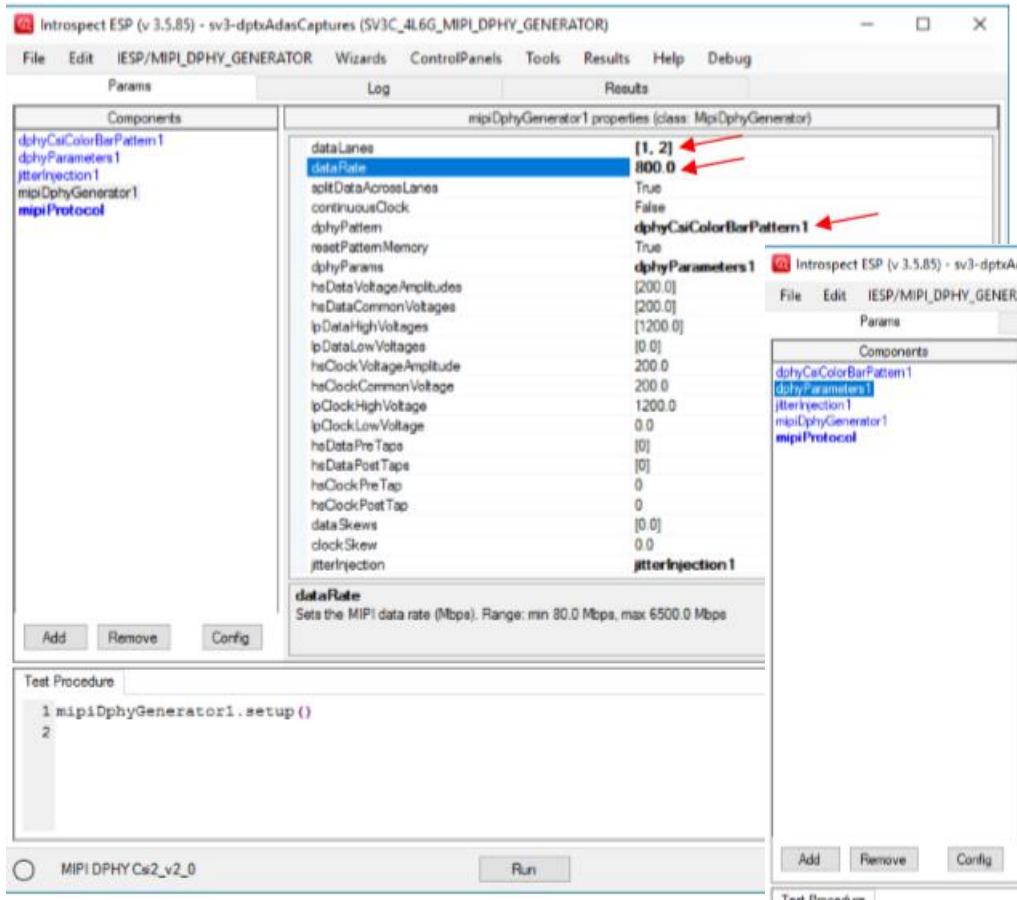


Test Scenario #3: Serializer Verification

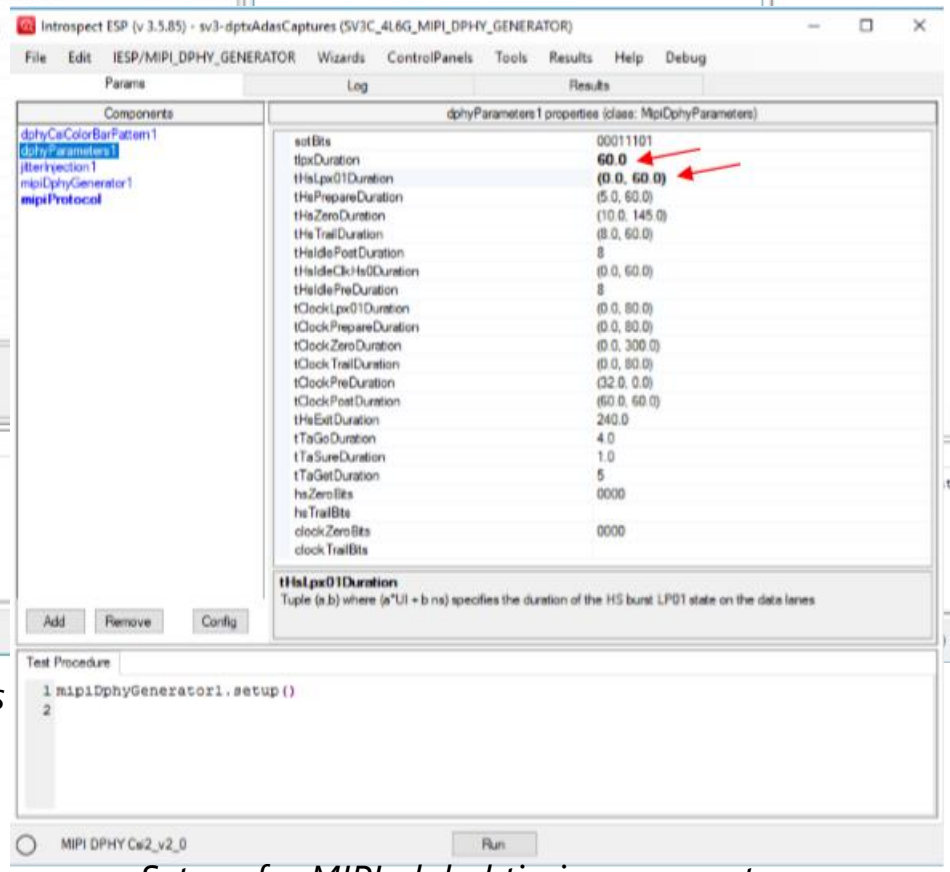


- Perform receiver stress testing on the serializer
- Perform camera emulation for exercising the system against multiple sensor technologies without being dependent on supplier/vendor availability
- Confirm system functionality in different driving conditions (e.g. record large streams and play them back)

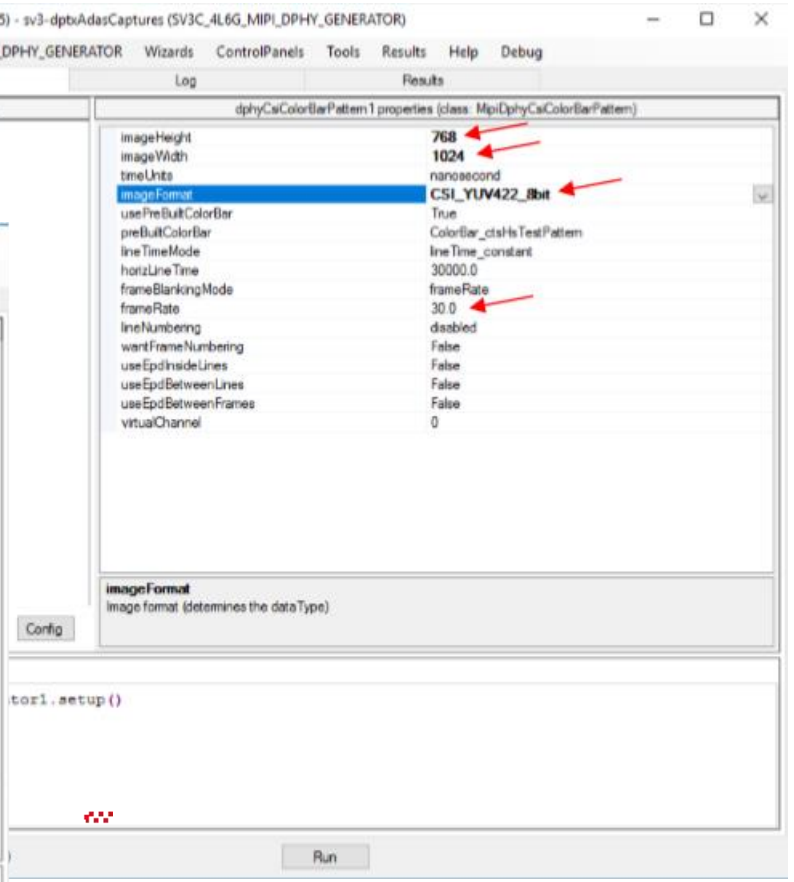
Test Set-up for Test Scenarios 3



Set-up for color bar image transfer on 2 lanes At 800Mbps

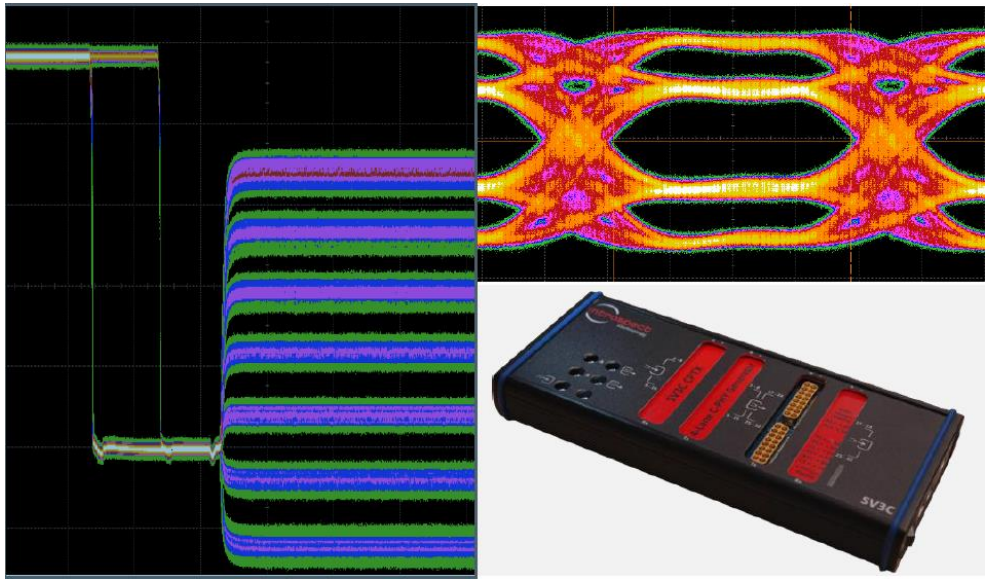


Set-up for MIPI global timing parameters



Set-up for color bar image properties

Introspect Technology
MIPI 측정솔루션



The Smart Phone of Test and Measurement

Smart Phone

Introspect SV1C

Shifting Product Development Landscape

Product Dev. Schedule

Enabling Multi-Disciplinary Tool Access

In the Design Lab
(Regression)

In the Silicon Validation Lab
(Data Collection)

In the Field
(Customer Validation)

Facts

Self-Funded and Growing

- Founded in Montreal, Canada with global distribution and support channel
- On-shore, outsourced model

Clearly Differentiated

- Ultra-compact, high-performance parallel SerDes tools for “high-volume” validation
- Unique correlation story in industry: same instrument for lab and for production

Facts

Cohesive, Skillful Development Team

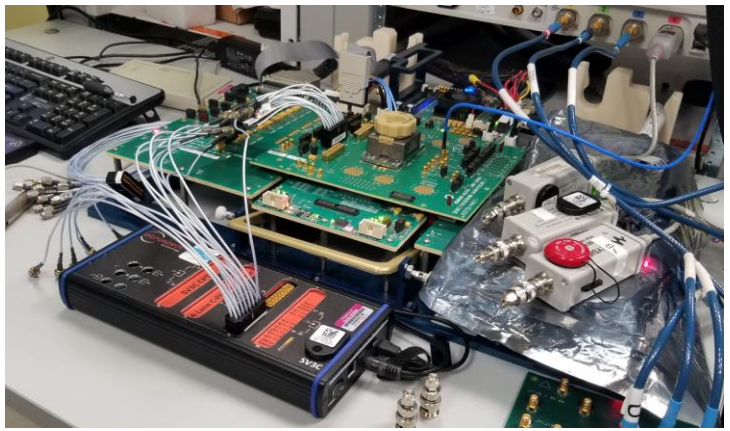
- Four generations of products and growing
- Team behind World's first MIPI C-PHY Analyzer

Recognized Industry Leadership

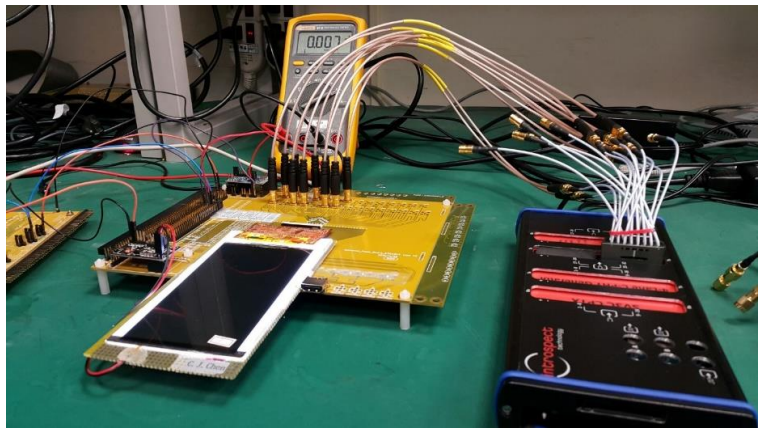
- Contributor member at MIPI Alliance
- Best in Design & Test Award 2013, 2015 (based on user votes)
- DesignVision Award 2007, 2010
- Finalist for ACE Executive of the Year Award 2014 (based on confidential judging committee)
- Finalist for ACE Design Team of the Year Award 2015

Coverage for All Phases of Development and Production

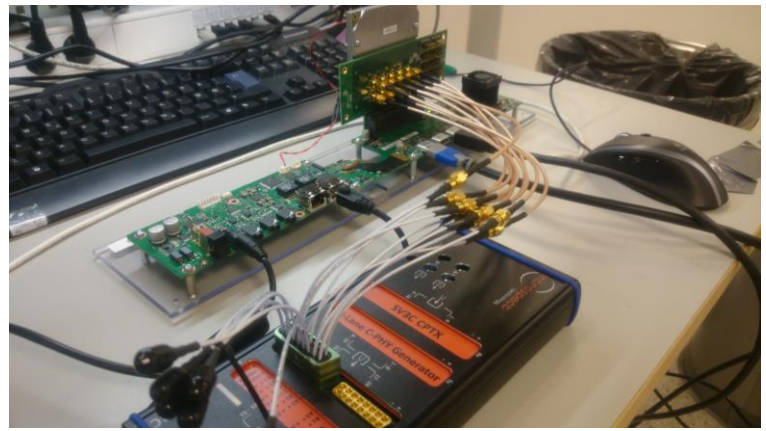
Electrical Characterization



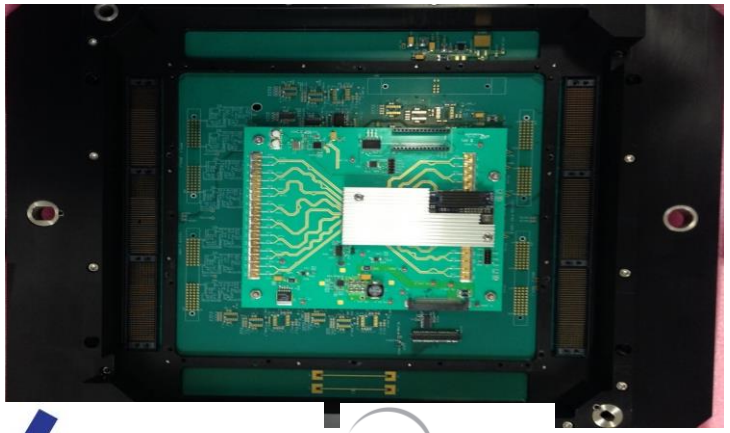
Design Validation



Applications Engineering



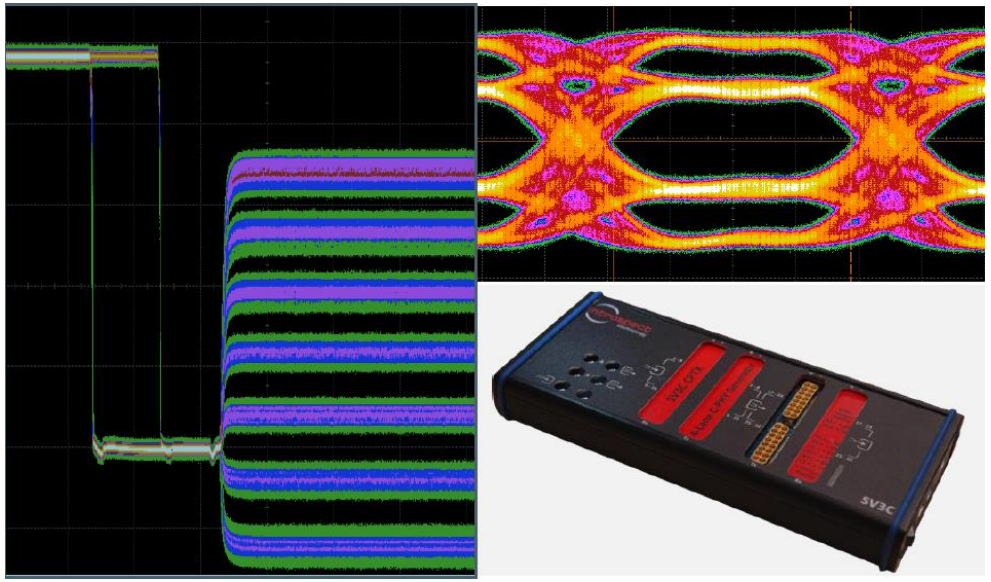
Production Testing



Failure Analysis

System-Level Test

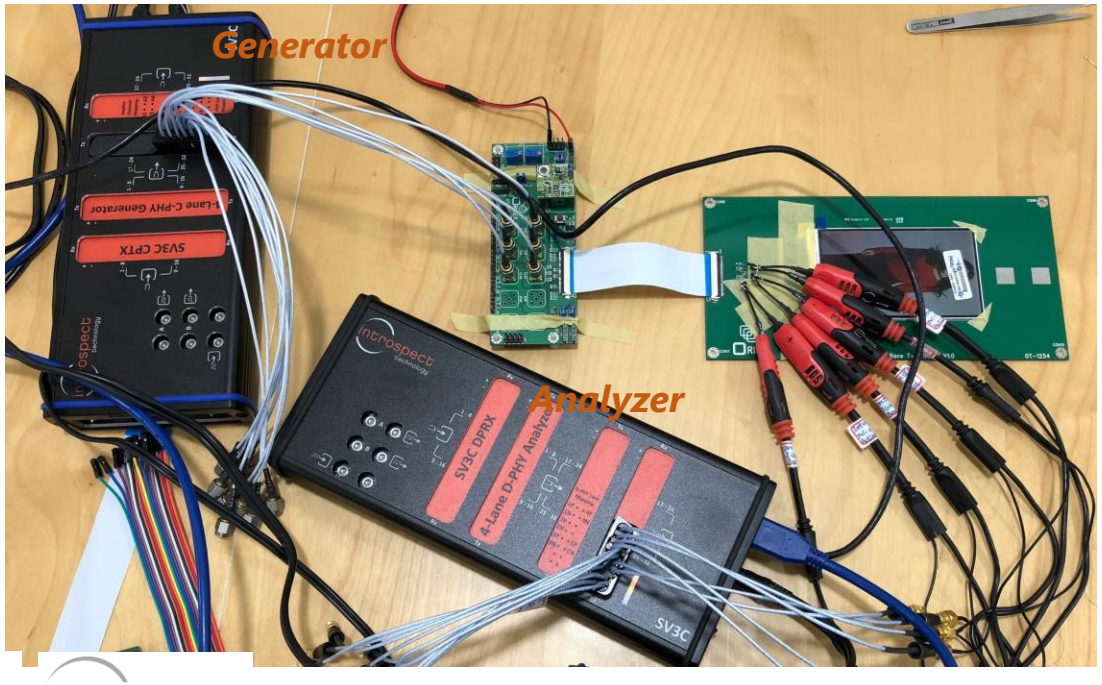
결론



Summary

MIPI interface specifications are updated at a rapid pace and increasingly achieve higher and higher performance

Introspect is here to help!



Module Emulation and SLT

Custom Protocol

CSI-2

DSI-2

Continuous and Burst Modes

6.5 Gbps	3.5 Gsps
CTS v2.0	CTS v1.1
D-PHY	C-PHY

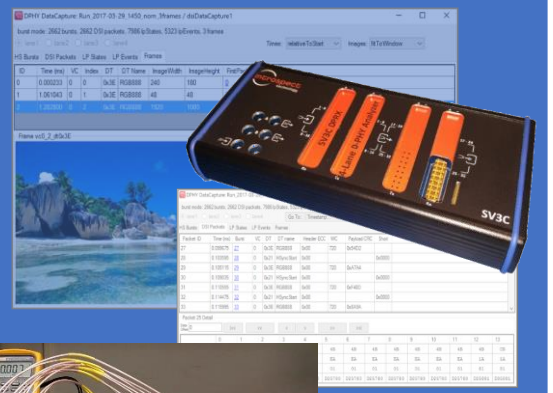
Introspect Test Solutions

Introspect Offers Complete MIPI Tool Coverage

Design Validation

FPGA-based design validation

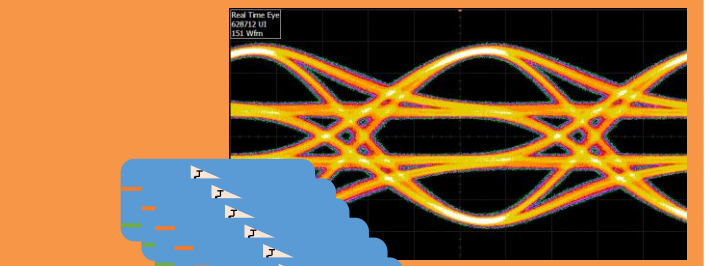
At-speed system-level testing



Device Characterization

Full-link receiver stress generation

Automated receiver conformance



Production Test

At-speed final test on ATE

Functional system-level test on ATE