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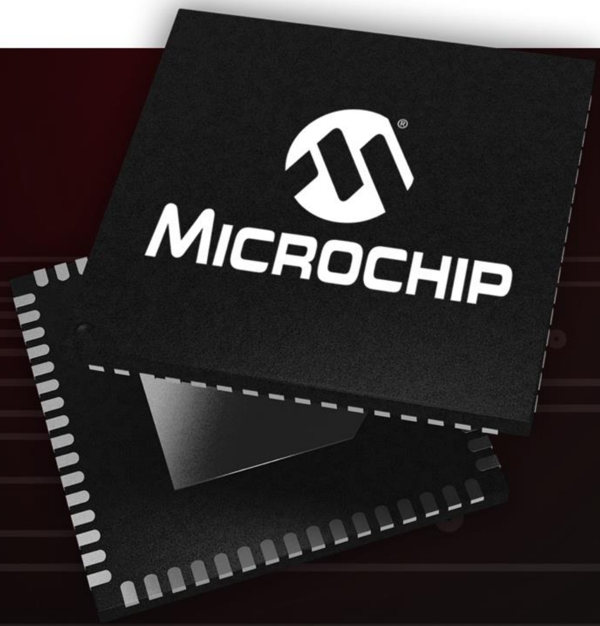


Presented by:
Jake Lee, Senior Embedded Solutions Engineer
May 10, 2018

Zero-Drift Operational Amplifiers

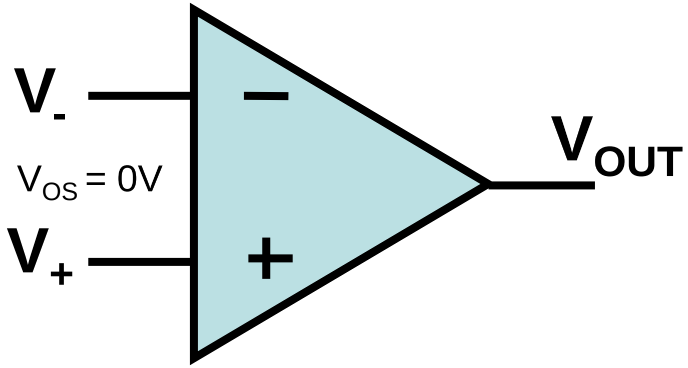
Architecture Overview and Design Considerations

Agenda

- **Definitions/Architecture**
  - “Precision” amplifiers, “zero-drift” amplifiers
- **Advantages of Zero-Drift Architecture**
  - Versus wafer/package trimmed, calibrated
- **Design Considerations**
  - Input bias and offset currents
  - Noise considerations
  - Thermal drift
  - Output settling/overload recovery
  - Enhanced EMI rejection

Amplifier Definitions

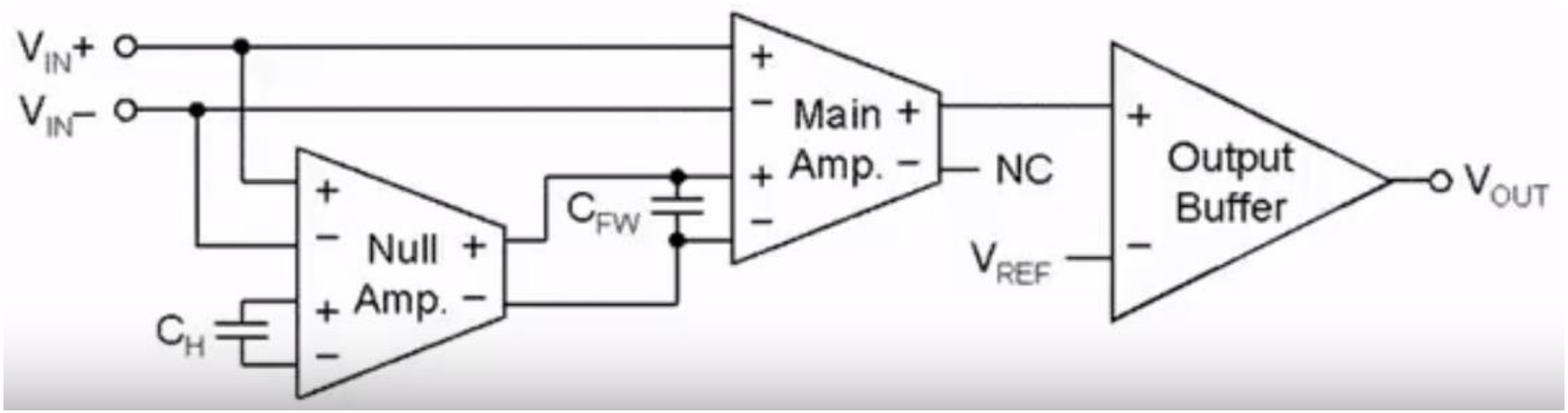
- **Input Offset Voltage**
  - Voltage delta between inverting and non-inverting amplifier inputs
- **“Ideal” Op Amp Model**
  - Input offset voltage is zero
- **“Precision” Amplifier**
  - Specifies a <u>maximum</u> offset voltage <1 mV

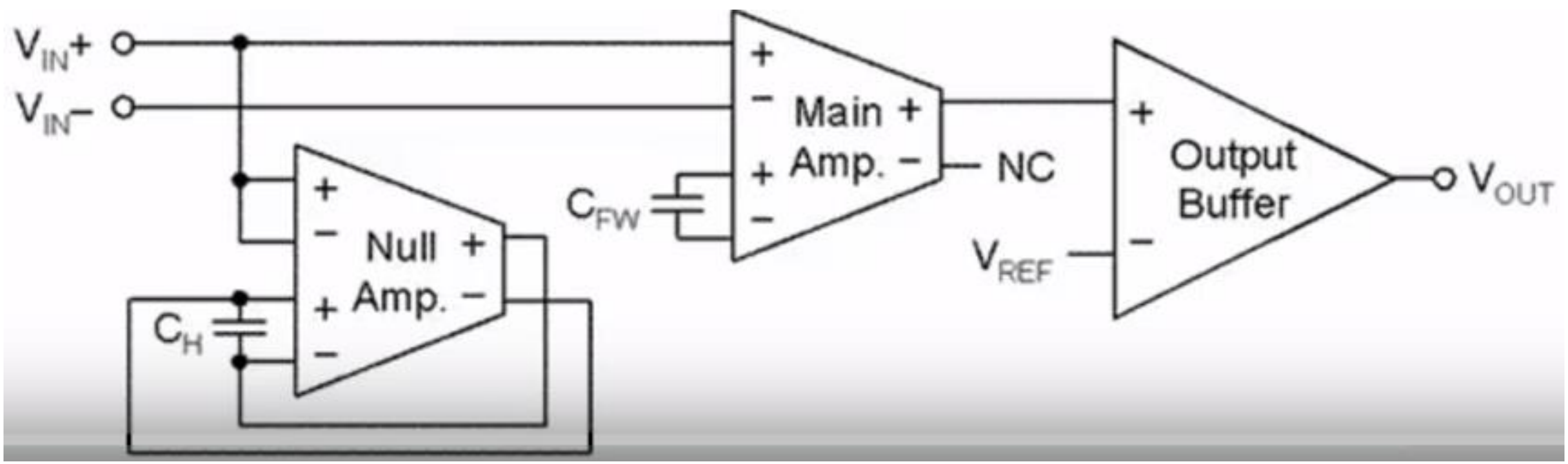


What is a Zero-Drift Amplifier?

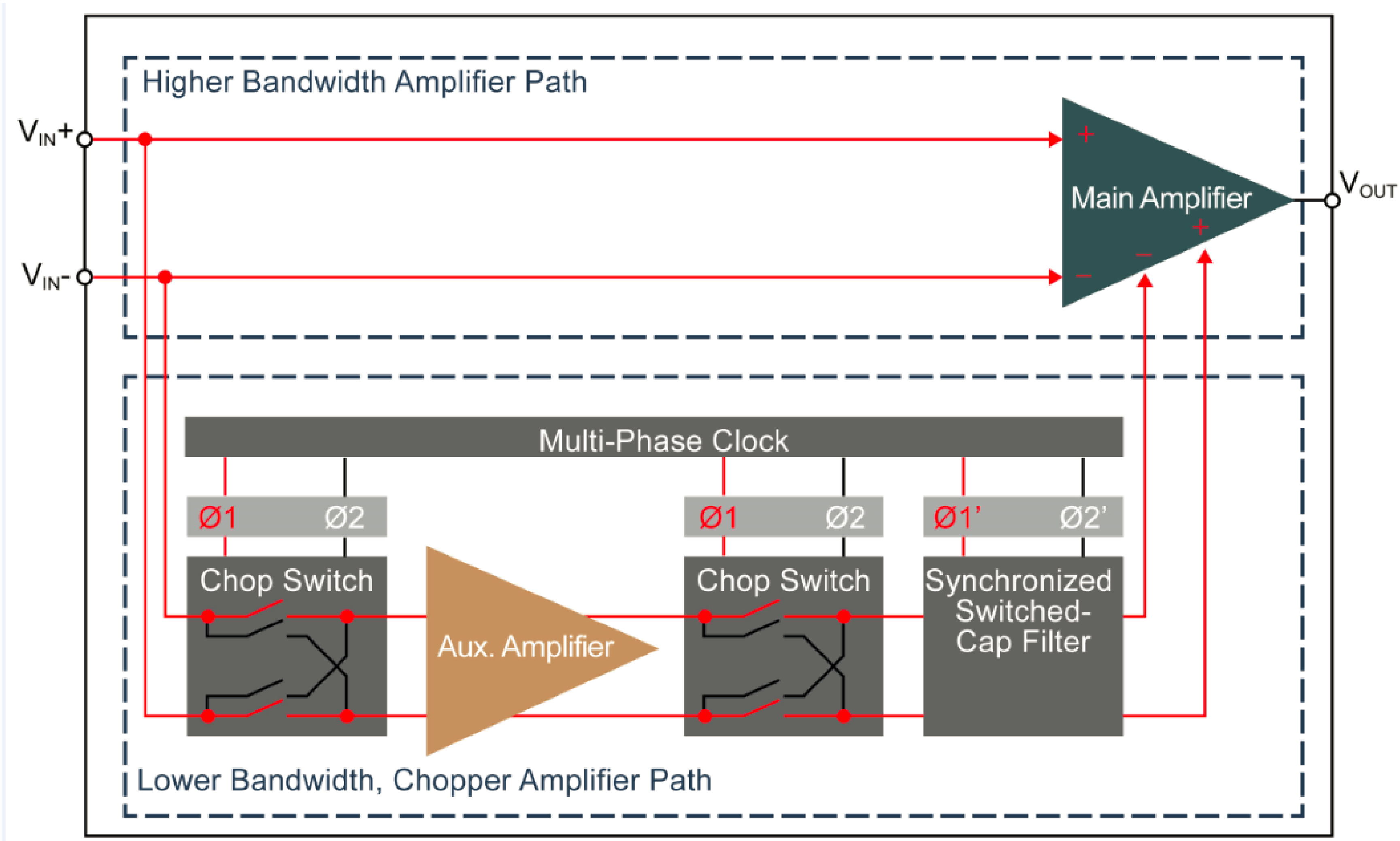
- **“Zero-Drift” Industry Standard Term**
- **V_{OS} is Continuously Corrected**
- **Two Basic Architectures**
  - Auto-zero
    - Use of a main amplifier and nulling amplifiers to correct offset
  - Chopper-stabilized
    - Use of a main amp and an “auxiliary amp” with chopped inputs/outputs to correct offset

Auto-Zero Architecture



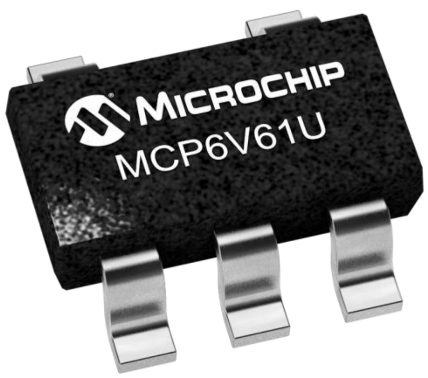


Chopper-Stabilized Architecture



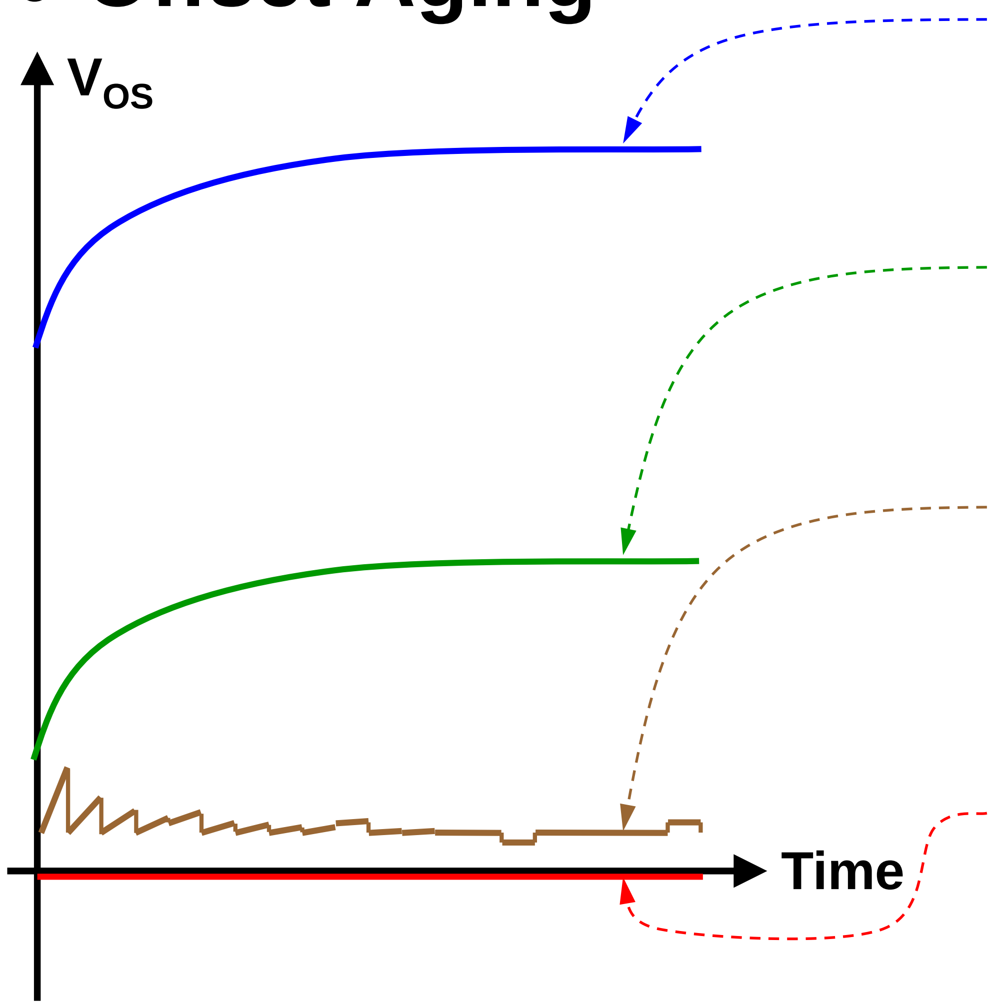
Zero-Drift Amplifiers Advantages/Disadvantages

- **V_{OS} is Corrected Frequently**
  - Example, every 10 µs
- **Advantages**
  - Accurate (DC up to 400 Hz, or more)
  - Insensitive to environment
  - V_{OS} aging virtually eliminated
  - No user inputs needed
- **Disadvantages**
  - Package size (auto-zero)
  - Higher price
  - Switching effects



Comparison of Op Amp Architectures

- **Offset Aging**



General Purpose
V_{OS} < ±3000 µV (typ.)
V_{OS} aging < ±300 µV (typ.)

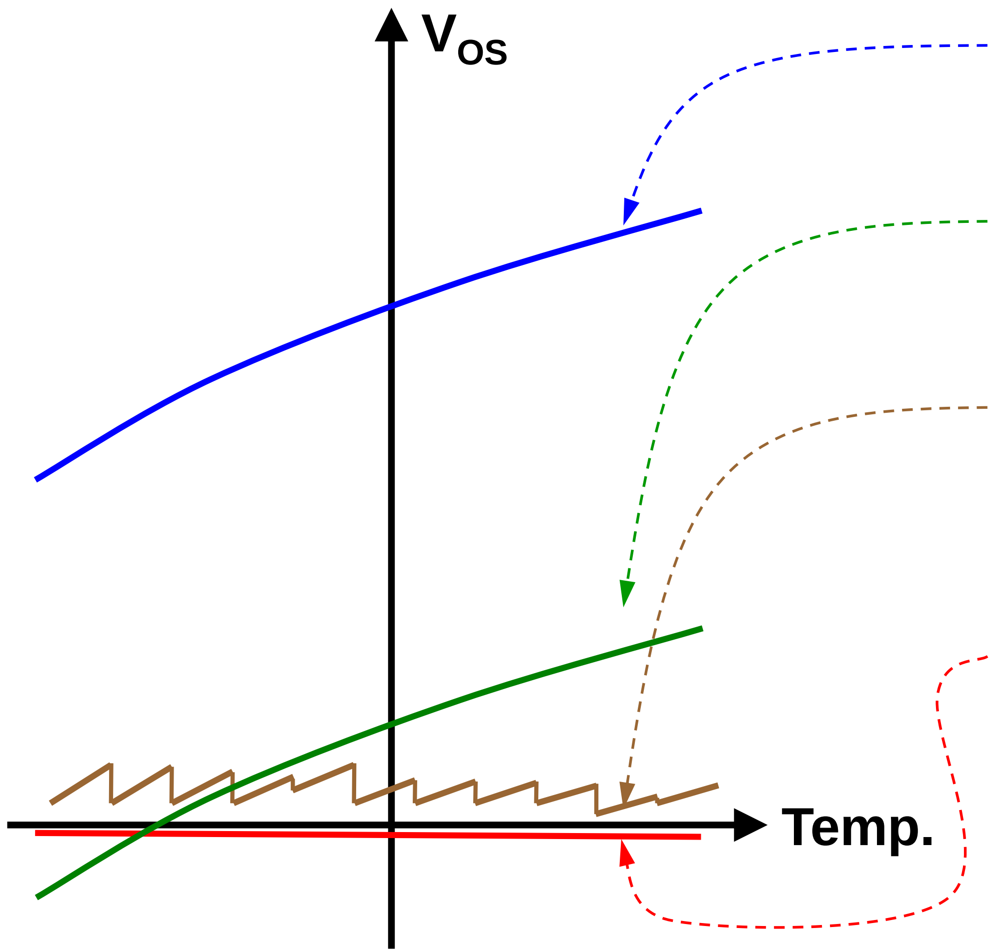
EPROM Trimmed
V_{OS} < ±250 µV (typ.)
V_{OS} aging < ±300 µV (typ.)

Calibrated (mCal)
V_{OS} < ±200 µV (typ.)
V_{OS} aging < ±50 µV (typ.)
V_{OS} repeatability < ±50 µV (typ.)

Zero-Drift
V_{OS} < ±3 µV (typ.)
V_{OS} aging < ±1 µV (typ.)

Comparison of Op Amp Architectures

- **Offset Drift (over Temperature)**



General Purpose
$\Delta V_{OS}/\Delta T_A = \pm 2\ \mu V/°C$ (typ.)

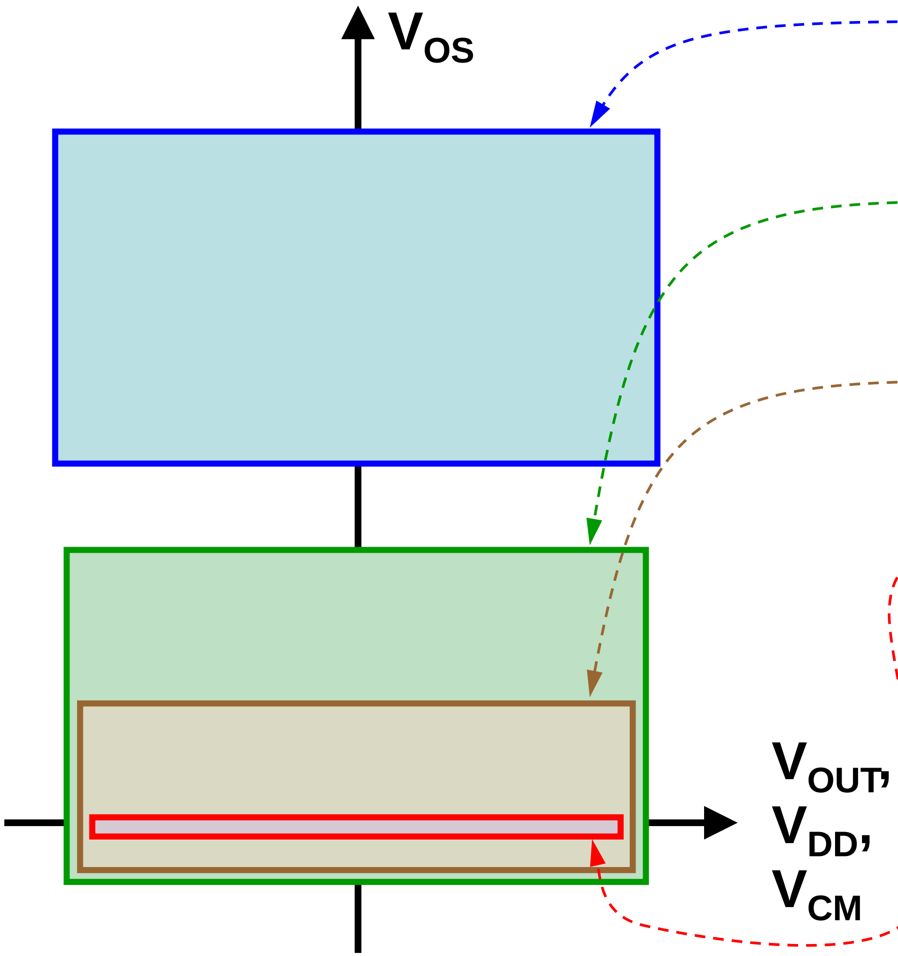
EPROM Trimmed
$\Delta V_{OS}/\Delta T_A = \pm 2\ \mu V/°C$ (typ.)

Calibrated (mCal)
$\Delta V_{OS}/\Delta T_A = \pm 2\ \mu V/°C$ (typ.)
V_{OS} repeatability < ±50 µV (typ.)

Zero-Drift
$\Delta V_{OS}/\Delta T_A = \pm 0.010\ \mu V/°C$ (typ.)

Comparison of Op Amp Architectures

- **Offset Changes due to Bias Condition**



General Purpose
$\Delta V_{OS} < \pm 1000\ \mu V$ (typ.)

EPROM Trimmed
$\Delta V_{OS} < \pm 1000\ \mu V$ (typ.)

Calibrated (mCal)
$\Delta V_{OS} < \pm 500\ \mu V$ (typ.)

Zero-Drift
$\Delta V_{OS} < \pm 1\ \mu V$ (typ.)

Note:
- **Calibrated (mCal)** parts can correct for slow changes in V_{OUT}, V_{DD} and V_{CM}.

Example Comparison: General Purpose VS Zero-Drift

Part #		MCP6401	MCP6V61	
Family		General Purpose	Zero-Drift	
GBWP (MHz)		1	1	
Specified Op Voltage (V)		1.8 to 6.0	1.8 to 5.5	
Max Vos (µV)		4500	8	560x Better!
Vos Drift (µV/°C)		2 (typ)	0.015	130x Better!
Typ CMRR (dB)		76	128	400x Better!
Typ PSRR (dB)		78	134	630x Better!
Noise (nV/√Hz) @ 1kHz		28	26	
Iq (µA)	Typical	45	80	
	Max	70	130	

Zero-Drift Application Examples

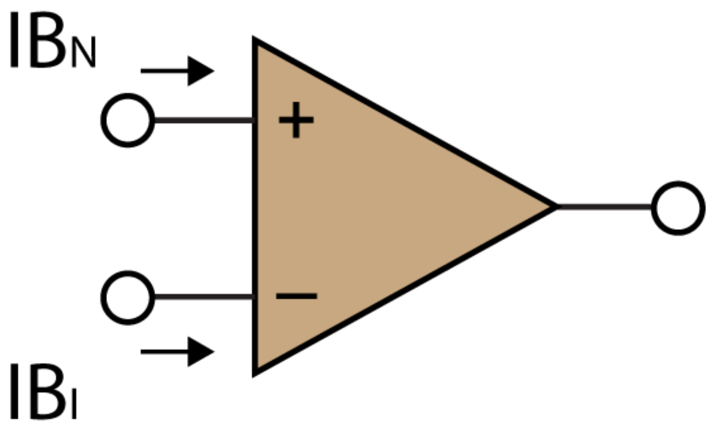
- Weight scales
- Oxygen sensor
- Temperature transmitter
- Methane detector
- Fire detection
- Lighting
- Flow meters
- Alcohol tester
- Thermocouple isolator
- Current sensor
- Appliances
- Cryogenics
- Power supplies
- Gas meters

Zero-Drift Operational Amplifiers

Design Considerations

Input Bias and Offset Current

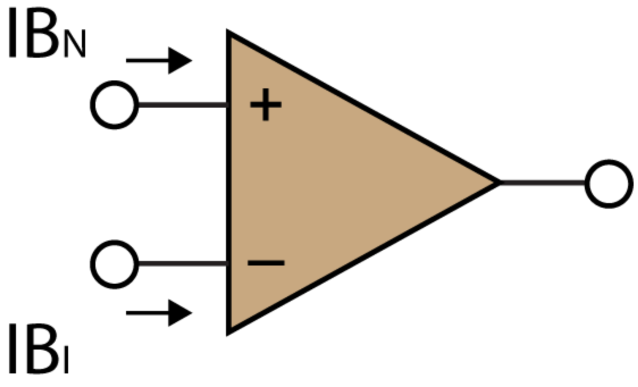
- **Two Physical Currents at the Input Pins**
- **Flow Into the Device is Positive, Flow Out of the Device is Negative**



Input Bias/Offset Current Definitions

- **Input Bias Current:**

$$I_B = \frac{IB_N + IB_I}{2}$$



- **Input Offset Current:**

$$I_{OS} = IB_N - IB_I$$

- **Rearranging:**

$$IB_N = I_B + \frac{I_{OS}}{2}$$

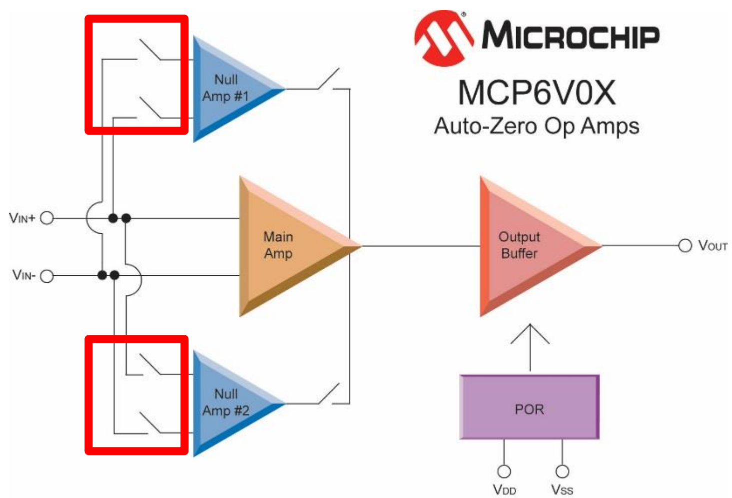
$$IB_I = I_B - \frac{I_{OS}}{2}$$

Input Bias/Offset Current Example

- **MCP6V06 Zero-Drift Op Amp**

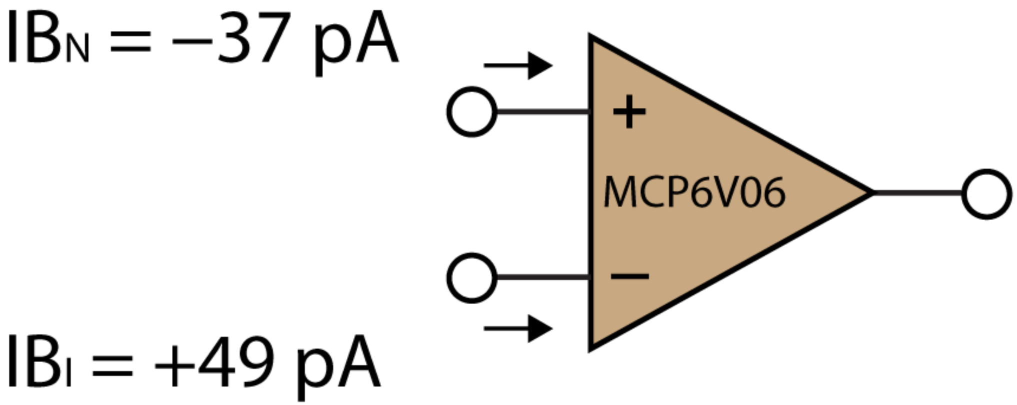
Input Bias Current and Impedance

Input Bias Current	I_B	—	+6	—	pA
Input Bias Current across Temperature	I_B	—	+140	—	pA
	I_B	—	+1500	+5000	pA
Input Offset Current	I_{OS}	—	-85	—	pA



Input Bias/Offset Current Example

- **MCP6V06 Leakage Currents**

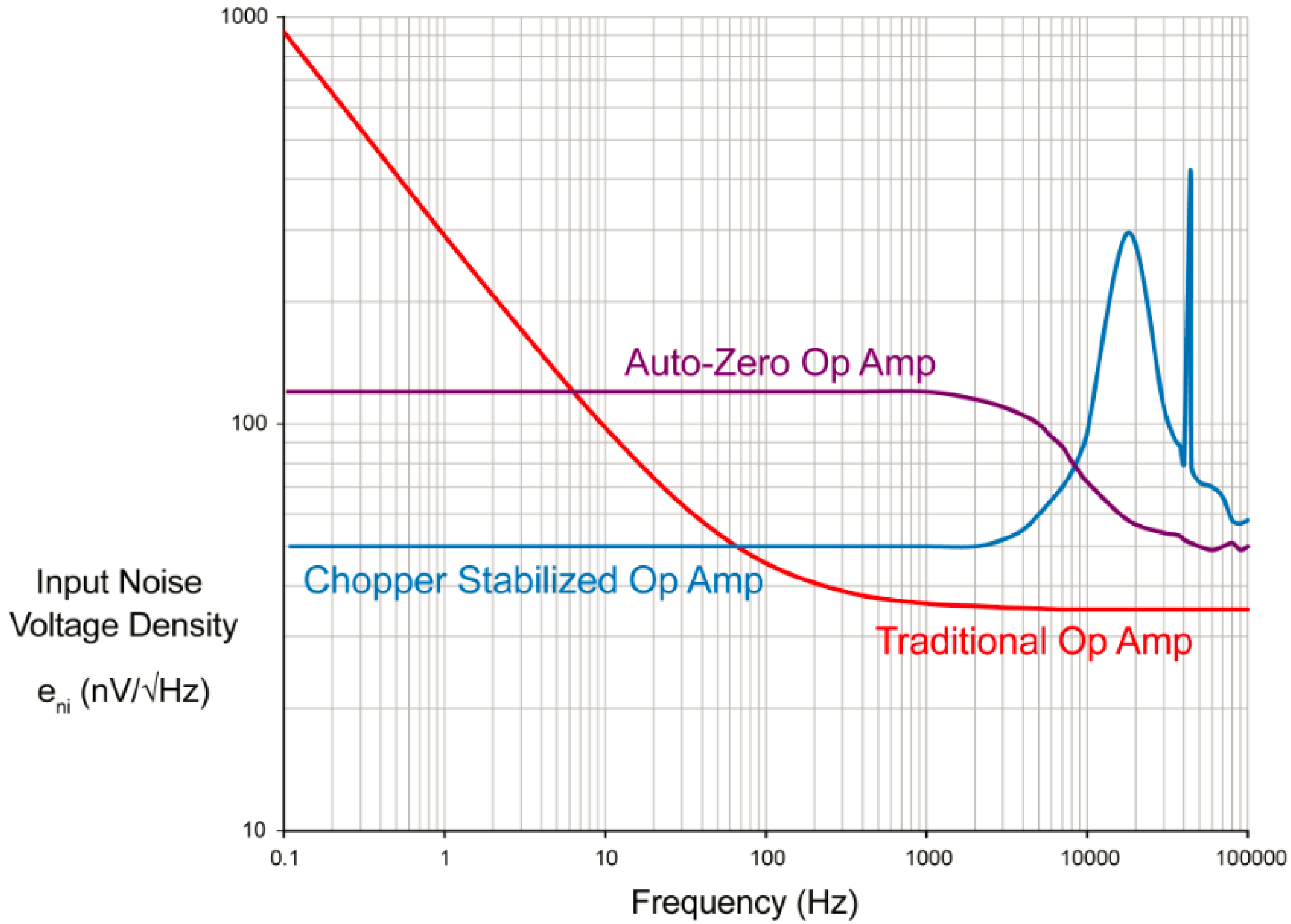


- **Summary**
  - For traditional amplifiers, I_{OS} is small
  - For zero-drift, may factor into error budget

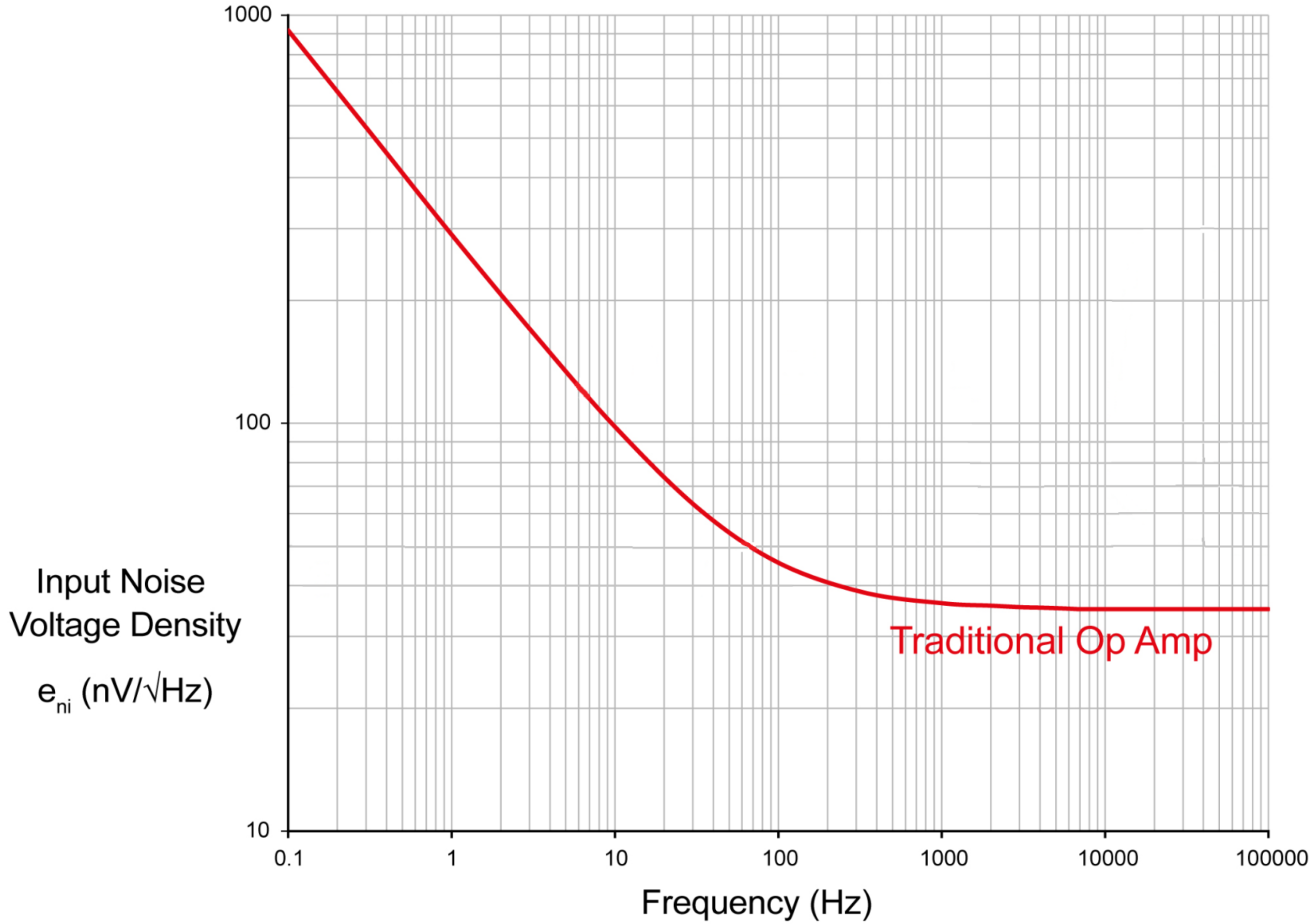
Noise Considerations: 1/f Noise

- **Also known as "flicker" noise, caused by stray currents on the silicon substrate**
- **Inherent to all silicon based electronics**
- **Dominate noise source at low frequency**
- **Zero-drift architecture eliminates 1/f noise as part of the offset correction**

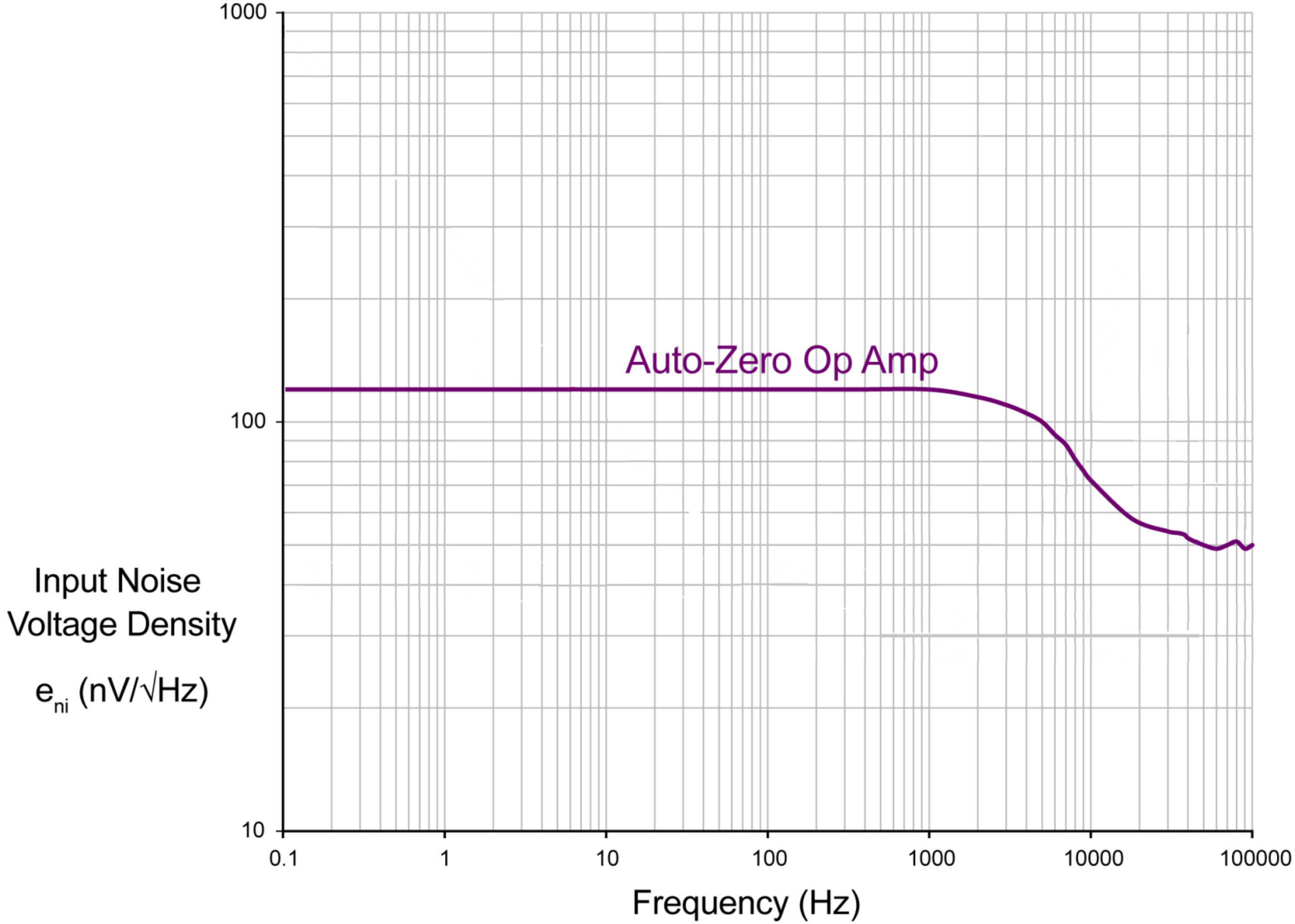
Noise Profiles by Architecture



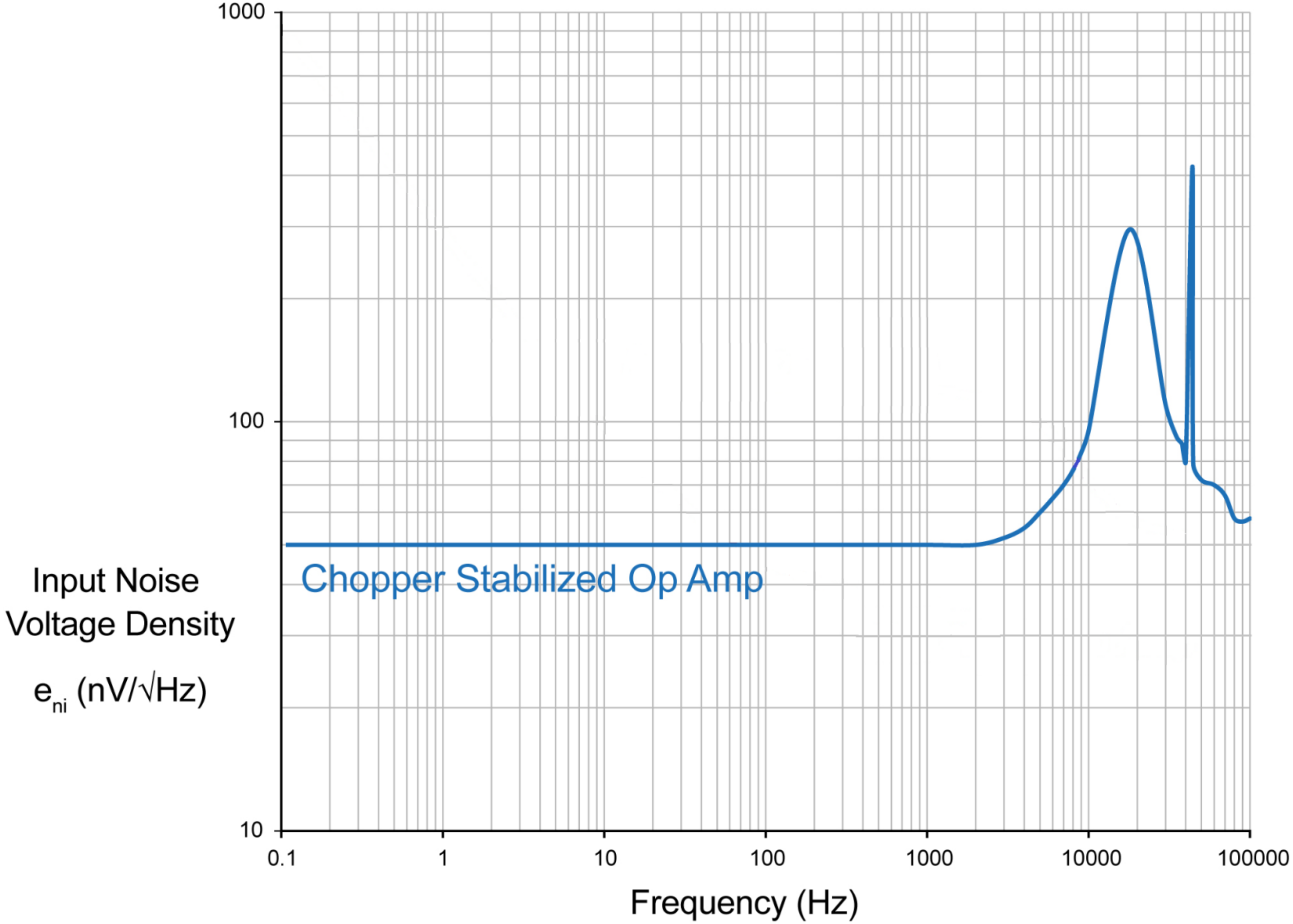
Noise Profile
1) Traditional Op Amp



Noise Profile
2) Auto-Zero Op Amp

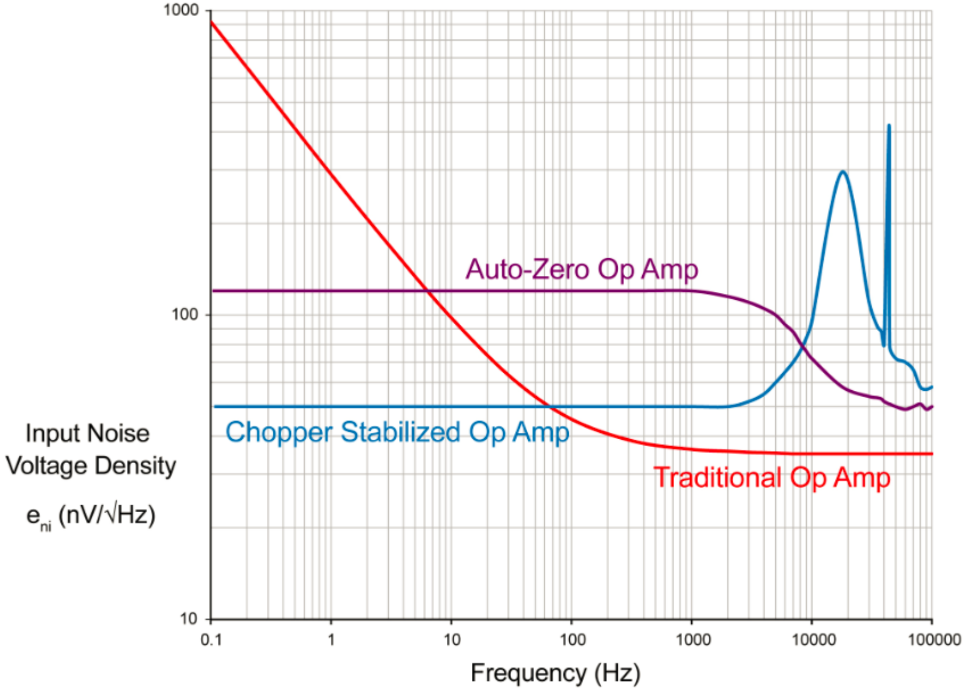


Noise Profile
3) Chopper Op Amp



1/f Noise Summary

- Zero-drift architecture eliminates 1/f
- Chopper is lower noise, noise peaking
- Auto-zero, noise folded into baseband

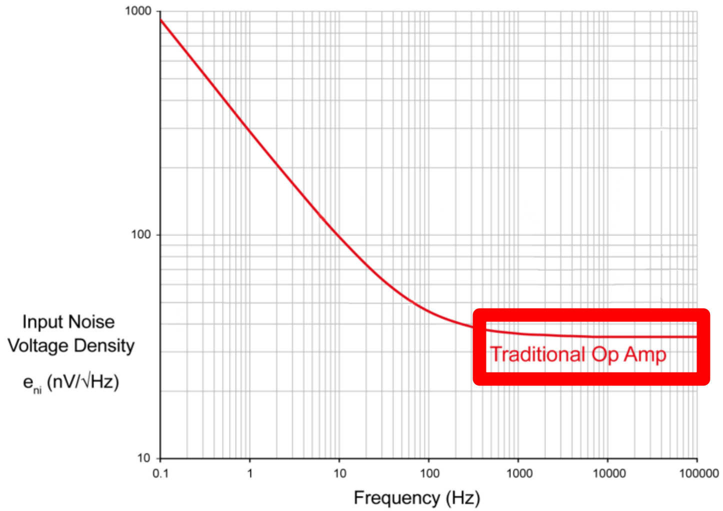


Noise Considerations: Voltage and Current Noise

- **When discussing noise, voltage noise tends to be the first consideration**
- **Current noise can also be a factor**
- **Definitions**
  - <u>Voltage noise:</u> Internal voltage noise of the amplifier that is reflected back to an ideal voltage source in parallel with the input pins
  - <u>Current noise:</u> Internal current noise of the amplifier that is reflected back to an ideal current source in parallel with the input pins

Noise Considerations: Voltage and Current Noise

- **Noise has power spectrum:**
  - Voltage noise: nV/√Hz
  - Current noise: pA/ √Hz
- **Specified where the white noise of the amplifier dominates**
  - Eliminates any 1/f noise effects



Voltage and Current Noise Application Example

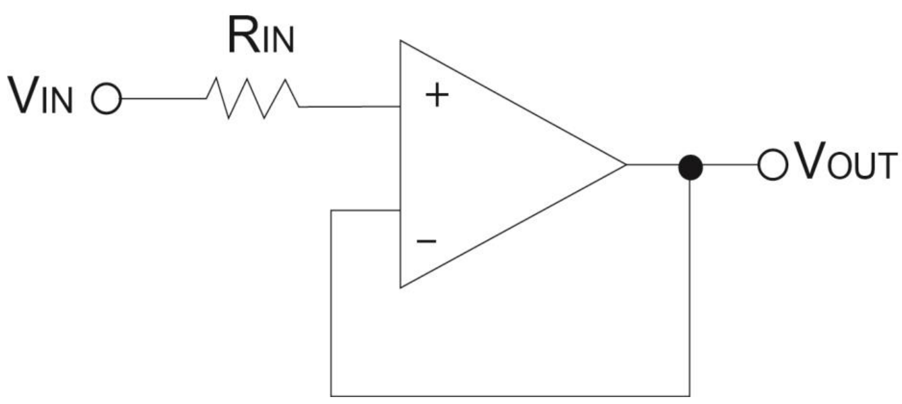
- **Application example**
  - Two precision amplifiers available on the market today

Parameters	Op Amp A	Op Amp B
Max Input Offset Voltage (µV)	200	500
GBWP (MHz)	20	22
Supply Voltage Range (V)	2.5-5.5	1.8-5.5
Voltage Noise Density (nV√Hz)	13	2.9
Current Noise Density (fA√Hz)	4	1100

  - Similar in speed, operating voltage, but noise varies considerably

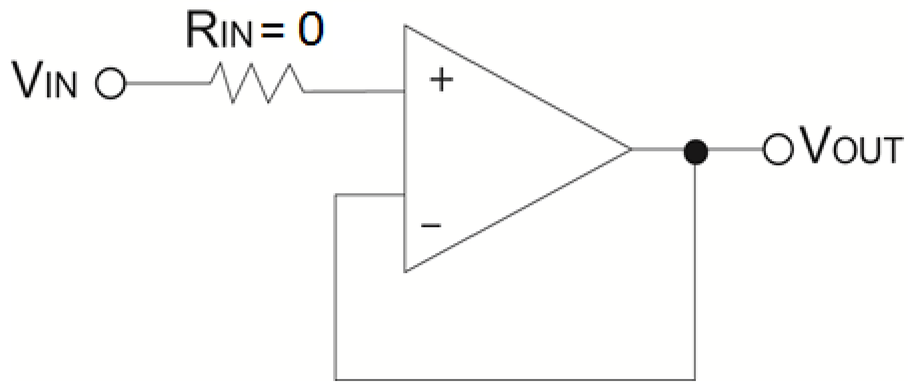
Voltage and Current Noise Application Example

- **Voltage follower circuit**
  - Amplifier noise
  - Input resistor noise
    - $V_{TH} = \sqrt{4kTRB}$



Voltage and Current Noise Application Example

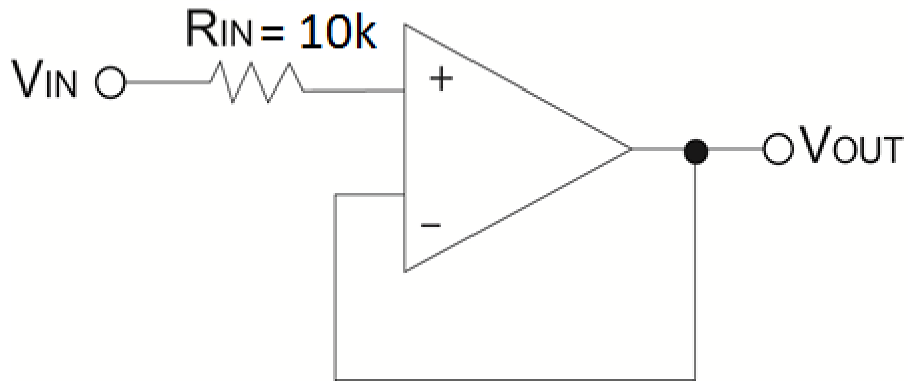
- **Case 1: Input resistance is 0Ω**



Noise Source (nV/√Hz)	Op Amp A	Op Amp B
Amplifier Voltage Noise	13	2.9
Amplifier Current Noise	0	0
Thermal Noise of R_{IN}	0	0
Total Noise	**13**	**2.9**

Voltage and Current Noise Application Example

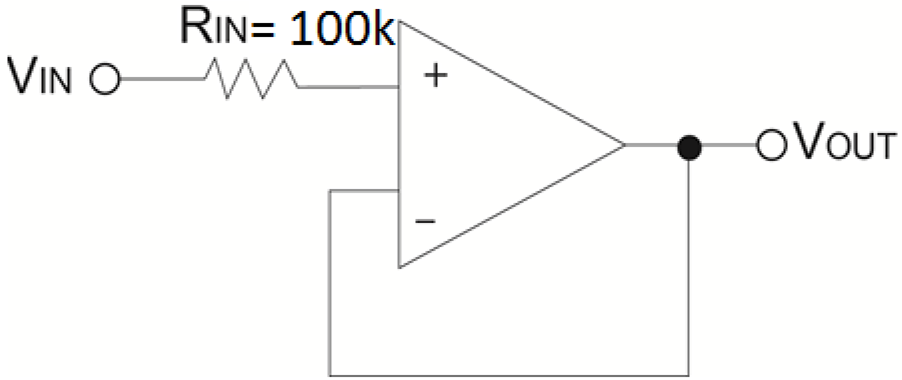
- **Case 2: Input resistance is 10 kΩ**



Noise Source (nV/√Hz)	Op Amp A	Op Amp B
Amplifier Voltage Noise	13	2.9
Amplifier Current Noise	0.04	11
Thermal Noise of R_{IN}	13	13
Total Noise	**18**	**17**

Voltage and Current Noise Application Example

- **Case 3: Input resistance is 100 kΩ**



Noise Source (nV/√Hz)	Op Amp A	Op Amp B
Amplifier Voltage Noise	13	2.9
Amplifier Current Noise	0.4	110
Thermal Noise of R_{IN}	41	41
Total Noise	**43**	**117**

Voltage and Current Noise Summary

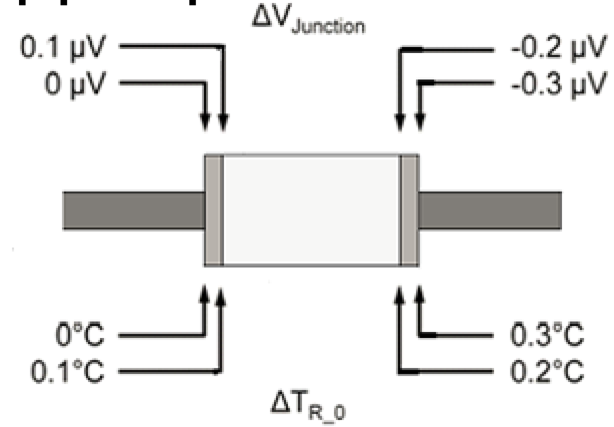
- **Both voltage and current noise must be considered**
- **Independent of amplifier architecture**
- **Especially true for high impedance applications**
  - pH meters, oven oscillators, thermocouple circuitry (isolation)

Minimizing Thermal Drift

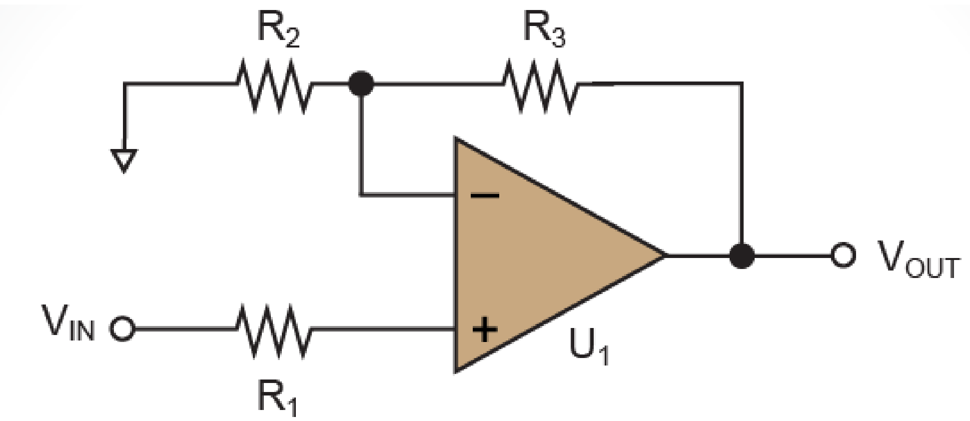
- **Terminology “Zero-Drift”**
  - Although never actually “zero”, extremely low relative to non zero-drift architectures
  - On the order of 100x better
- **Precision circuitry requires other components (including passives) to also be low drift**
  - Highly dependent on PCB layout

Minimizing Thermal Drift

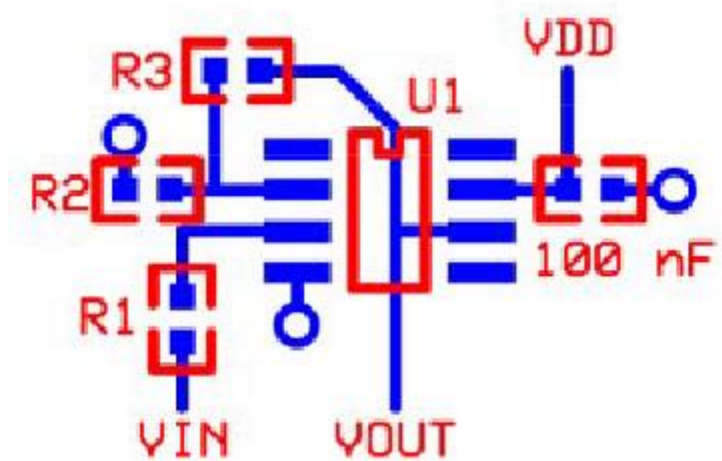
- **Thermo-junctions**
  - Two dissimilar metals come into contact
  - Creates a temperature dependent voltage shift
- **Common to PCBs**
  - Components soldered to copper pads
  - Jumpers
  - Vias



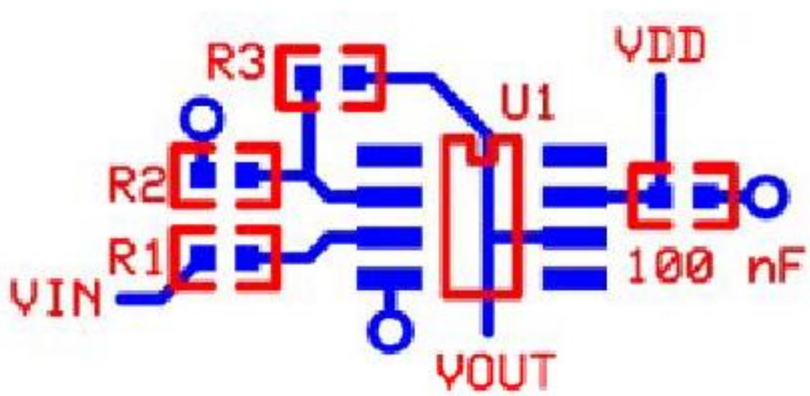
Minimizing Thermal Drift Application Example



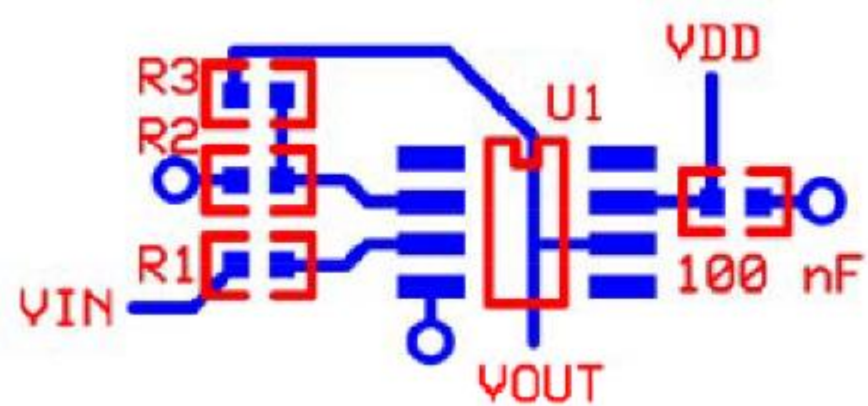
Schematic: non-inverting gain



Case 1: Worst layout for drift



Case 2: Better layout for drift



Case 3: Best layout for drift

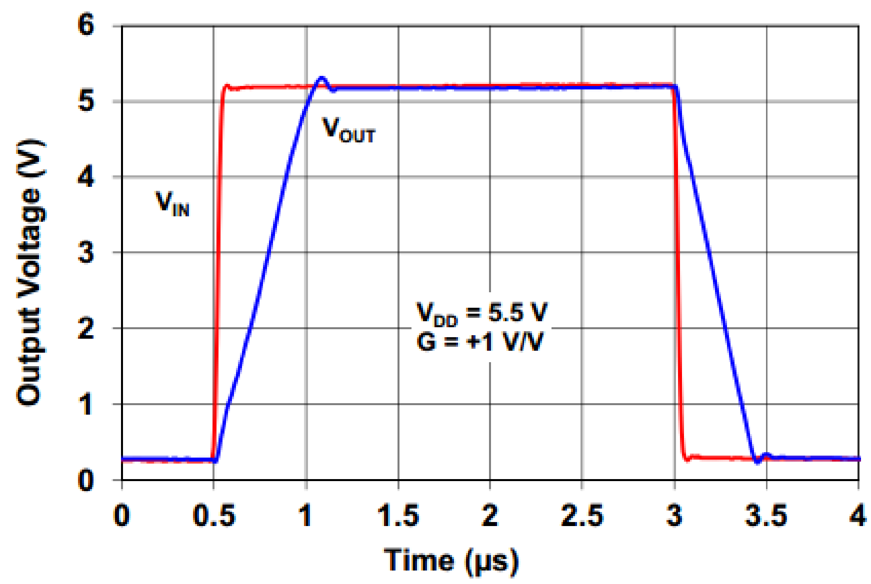
Minimizing Thermal Drift Summary

- **Selecting precision, low drift ICs not enough**
- **Thermo-junctions create voltage shifts that are dependent on temperature transients**
- **Proper PCB layout can minimize the adverse effects of thermo-junctions**

Output Settling/Overload Recovery Time

- **Large scale step responses or overload conditions are difficult for Zero-Drift Amplifiers**

- **Two signal paths:**
  - High bandwidth path (GBW, slew rate)
  - Lower bandwidth chopper path



Electromagnetic Interference (EMI)

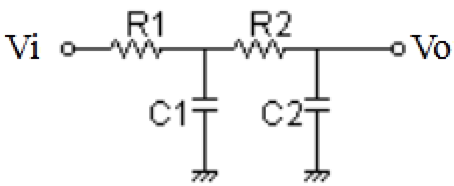
- **Benefits of EMI enhanced amplifiers:**
  - Reduced dependence on external filtering
  - Maintain signal integrity with fewer components
  - Reduction of development time and component cost
  - Specified performance requires good PCB layout and component selection

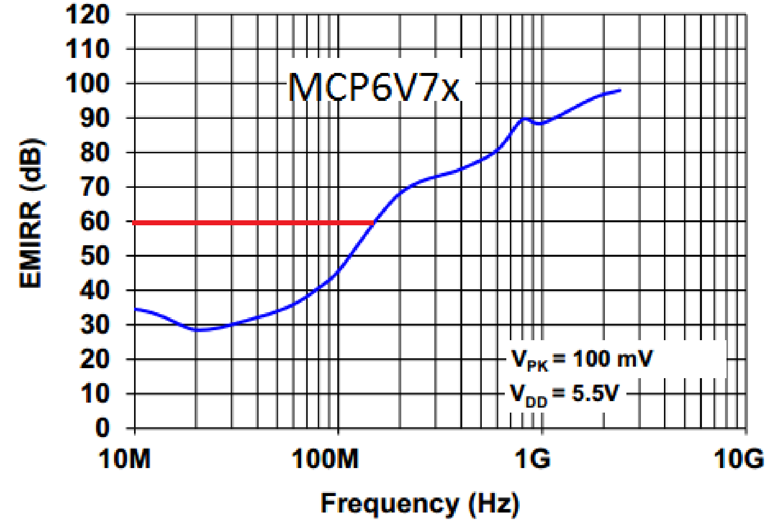
MCP6V7x EMI enhanced amplifier data sheet:

EMI Rejection Ratio	EMIRR	—	75	—	dB	V_{IN} = 0.1 V_{PK}, f = 400 MHz
		—	89	—		V_{IN} = 0.1 V_{PK}, f = 900 MHz
		—	96	—		V_{IN} = 0.1 V_{PK}, f = 1800 MHz
		—	98	—		V_{IN} = 0.1 V_{PK}, f = 2400 MHz

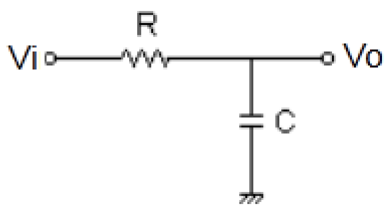
EMI Rejection Microchip vs. Competition

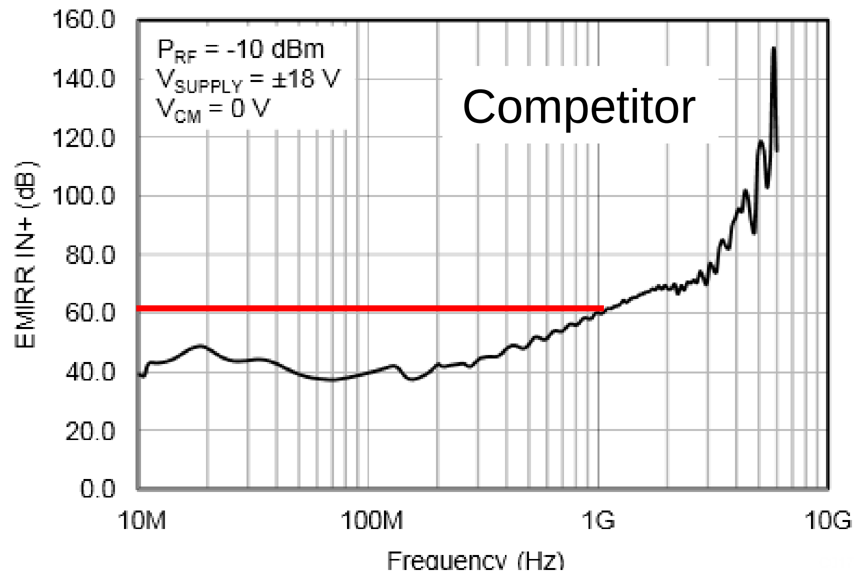
- Microchip second order “RC” architecture for EMI protection





- Simple “RC” architecture for EMI protection





Zero-Drift Amplifiers Summary

- **Zero-Drift Architecture: continuously self-correcting offset voltage errors**
  - Inherent benefits:
    - Low initial offset, low offset drift, eliminates 1/f noise, excellent common mode/power supply rejection
  - Design considerations:
    - Input bias currents, noise, drift, output behavior, susceptibility to EMI

Thank You