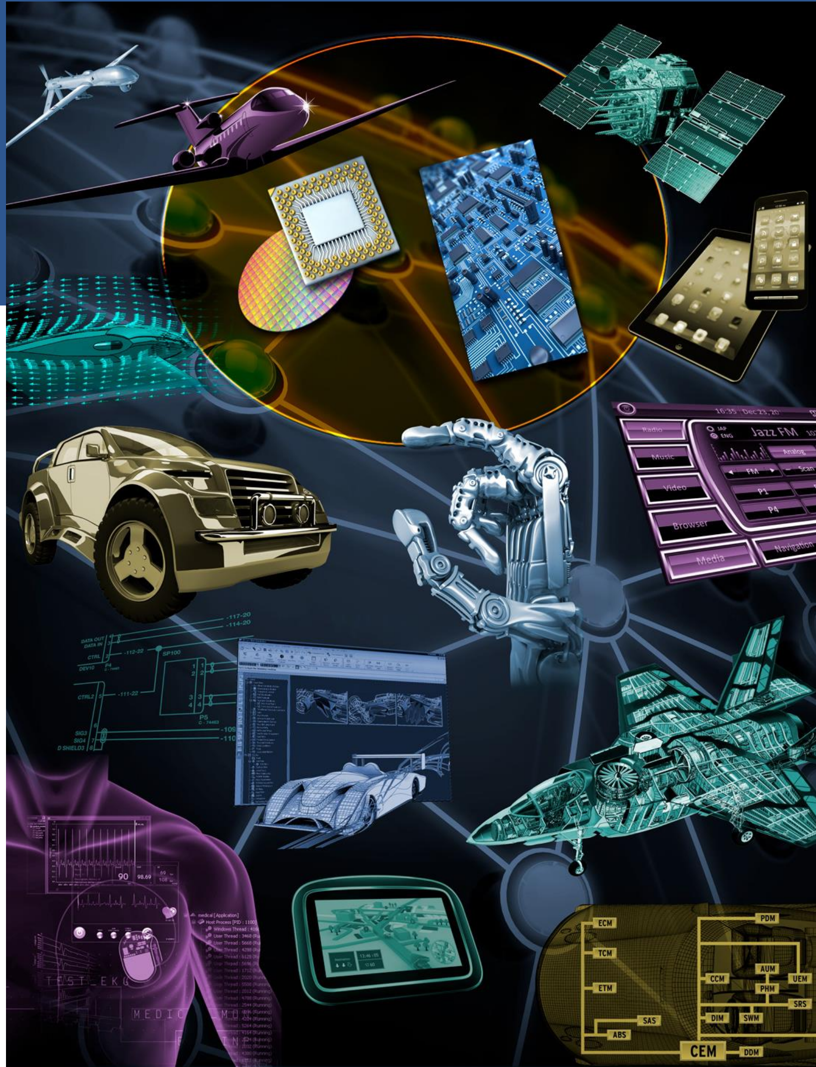

True Advanced Heterogeneous 3D IC-Package Verification & Implementation

Rock Kim

Corporate Application Engineer

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Agenda

- HDAP Introduction
- Key Customers using Xpedition IC Packaging
- Heterogeneous 3D IC – Package Planning & Prototyping
- HDAP Implementation
- Heterogeneous 3D IC – Package Assembly Verification
- Summary

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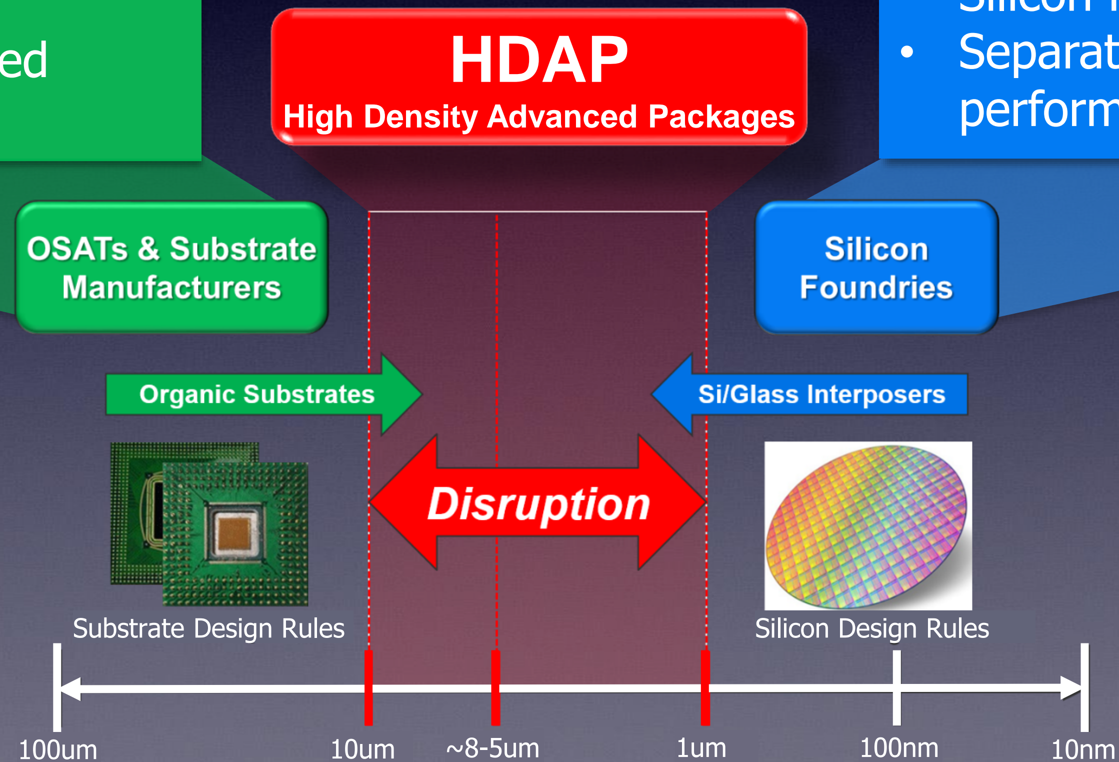
HDAP – HIGH DENSITY ADVANCED PACKAGING

HDAP – Introduction

different design methodologies and characteristics

- Gerber output
- Windows based tools
- Design drives manufacturing
- Non-Manhattan shapes
- Organic RDL layers
- Built-in DRC checks performed within design database

- GDSII output
- Linux based tools
- Manufacturing drives design (PDKs)
- Manhattan based shapes
- Silicon RDL layers
- Separate verification (DRC) performed on mfg. output



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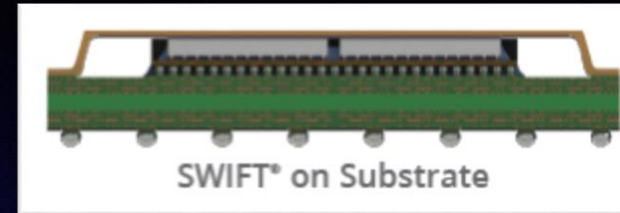
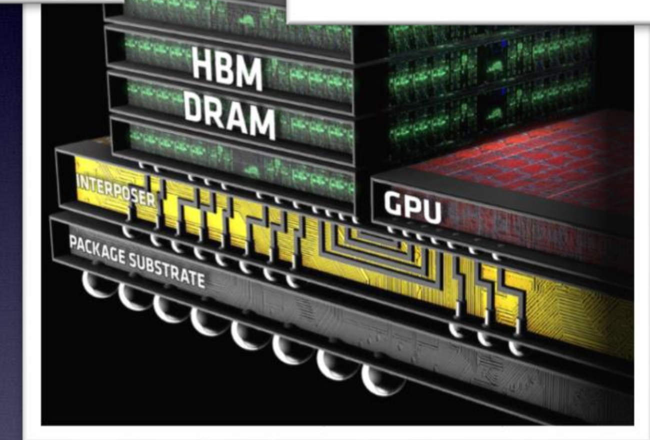
High Density Advanced Packaging (HDAP)

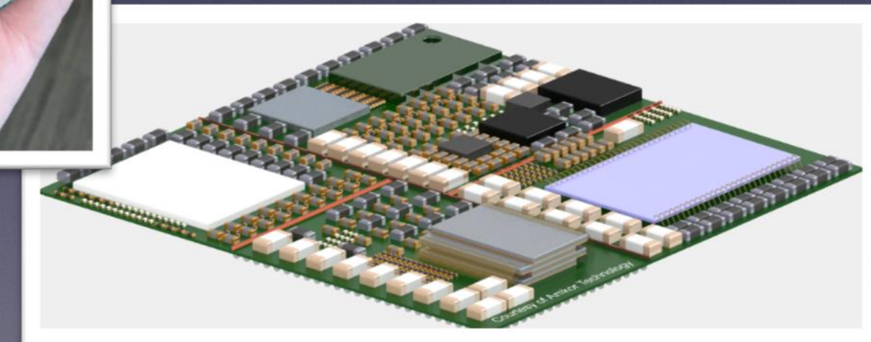
Target applications / field of use

- FOWLP Fan-Out Wafer Level Packages (single- or multi-die)
- 2.1D, 2.5D, and 3D Interposers
  - Organic or silicon
- High-density flip-chip >10K pins
- Applications
  - Heterogeneous integration
  - HPC, AI, networking
  - Mil-aero and automotive
  - Mobile compute & communication

- Heterogeneous multi-die modules, SIP system-in-package
  - 5G, IoT, automotive, etc…







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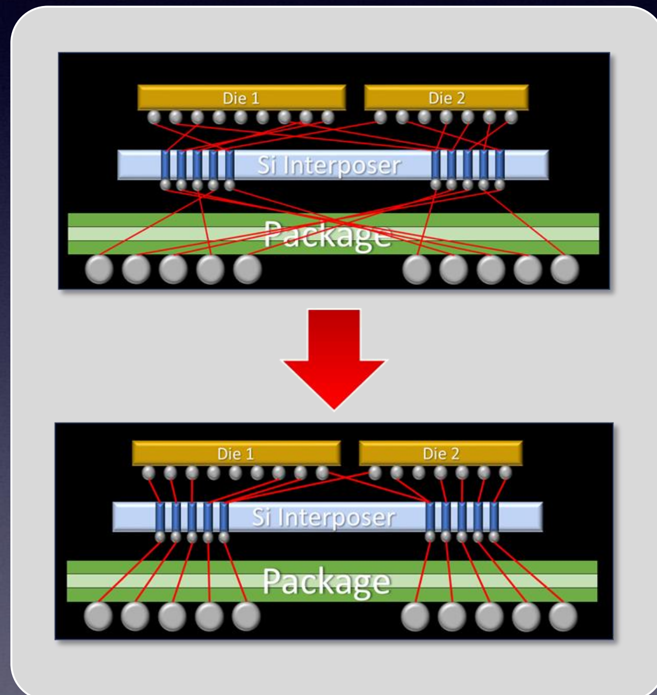
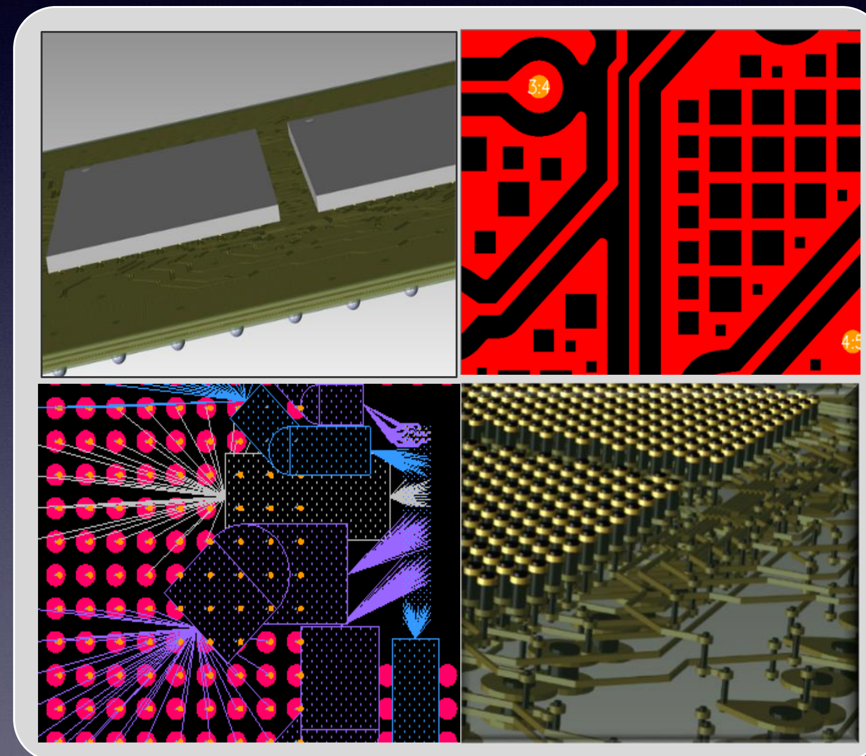
The scale and complexity of HDAP exposes challenges in existing processes and tools

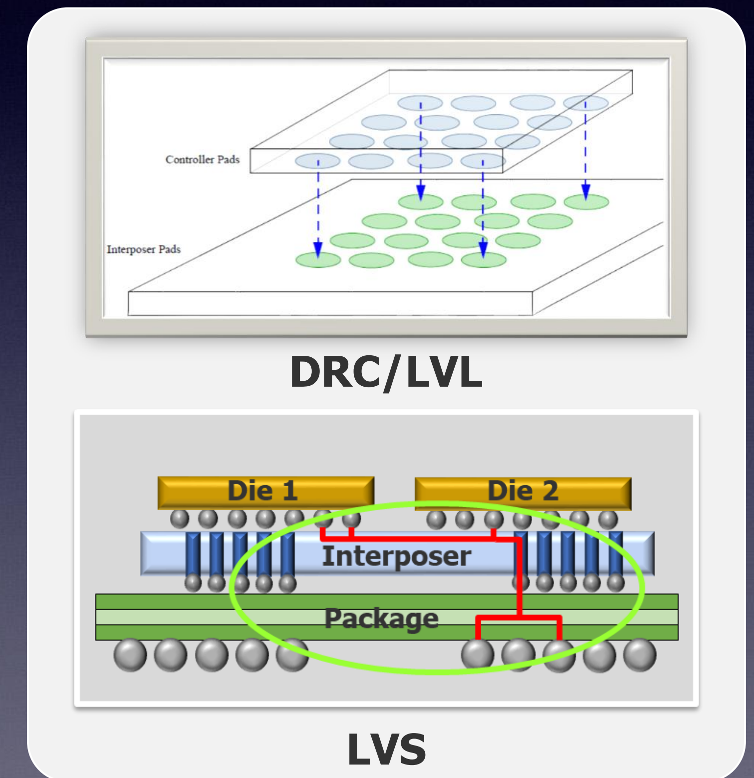
- Cost, risk, and limitations of monolithic scaling is driving growth of multi-die (heterogeneous) packaging solutions creating opportunity and challenges throughout the design process



Heterogeneous Planning and Rapid Prototyping



Physical Implementation



Package Assembly Verification

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Do you struggle with your flow and tools?

Common Problem Areas	Your Experience?
Multi-die/package integration errors due to use of spreadsheet's and static data	
Need for multiple workarounds and scripts	
Fabrication/manufacturing issues constantly being missed by DRC flow/process	
2D only design flow that limits productivity	
Multiple ECOs to create error free filled shapes/planes	
Poor quality GDSII output resulting in ECO's	
Time consuming creation of simulation package models	
Performance issues with very large (pin count) designs	

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Mentor's HDAP Solution Components

Xpedition Substrate Integrator
- Heterogeneous planning & prototyping
- System assembly and design mgmt.

Xpedition Package Designer
- Physical implementation
- Extraction
- In-process verification

Windows & Linux platforms

Calibre 3DSTACK DRC/LVS
- Verification

Calibre RVE
- Results visualization

Linux platform

OSAT Alliance Program (PDK/ADK enablement)

Developed specifically to meet the capacity and performance challenges of 2.5D/3D heterogeneous assemblies

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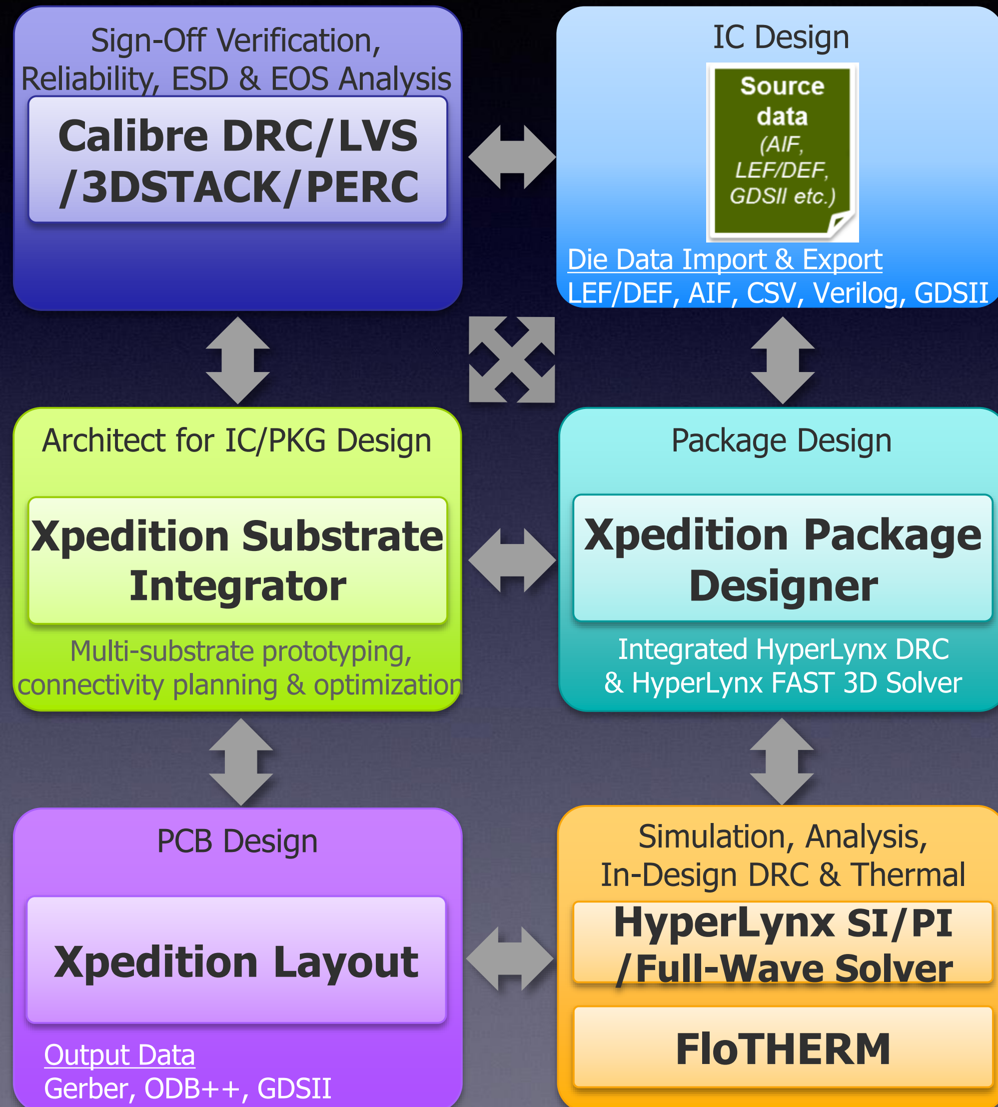
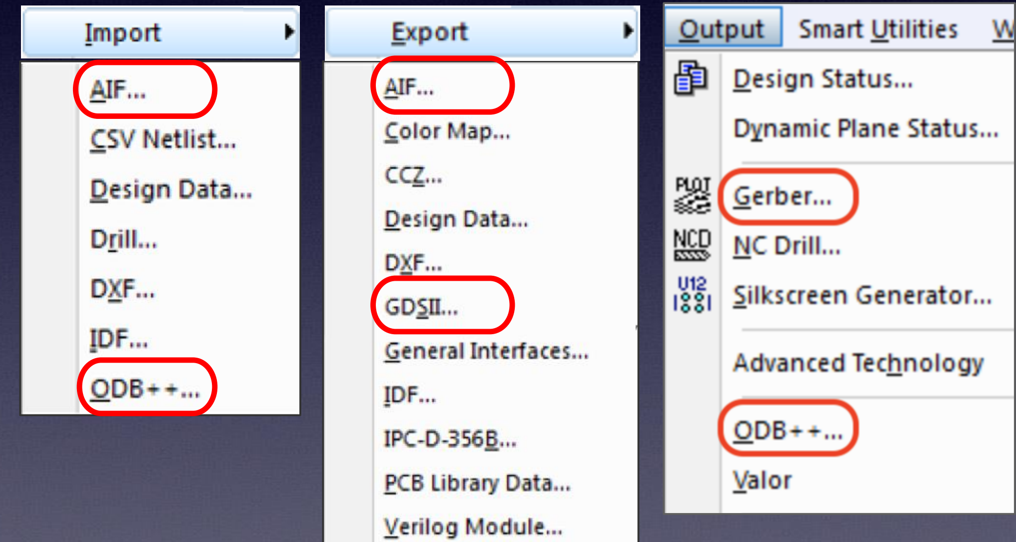
Design Across IC, Package, and PCB

2.5D/3D IC, Package and PCB Co-Design Solutions



- **From XPD (Xpedition Package Designer)**



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KEY CUSTOMERS USING XPEDITION IC PACKAGING

Key Customers using Xpedition IC Packaging

Items	Computer Chip Maker	Smartphone Processor Maker	Foundry	OSAT	IDM	Fabless Semi
EDA tools used for Advanced Packages	**XPI (XSI/XPD)**	**XPI (XSI/XPD)**	**XPI (XSI/XPD)**	**XSI/XPD**	**XPD**	**XSI**
Triggers to choose Mentor	○ **Tool Crash & Performance** ○ Poor Tool C Capacity & Support ○ Engineering Roadmap ○ IC package co-design	○ **Tool Crash & Performance** ○ Cross domain net naming tracking ○ Package Level LVS initiative ○ Module design ○ 3DSTACK ADK support from OSATs	○ **GDSII quality issue** ○ Second source for reference flow ○ Tool C technical issues (GDS)	○ **Tool Crash & Performance** ○ GDSII output quality ○ 2.5D interposer assembly issue ○ Smartphone Processor Maker pressure	○ **Poor Tool C Capacity, Frequent Tool Crashes & Performance**	○ Elimination of internally developed package planning tool ○ Cross domain net naming tracking (Die to Package optimize) ○ 3DSTACK integration
What for	○ Package design ○ Computer Chip Maker Custom Foundry Services	○ Package Design ○ Module design (300-400 parts on a package module) ○ PDK and ADK support from Foundries and OSATs	○ Package Design ○ PDK (FOWLP process design kit) ○ DRC (Calibre & HyperLynx DRC) ○ Calibre 3DSTACK ADK support	○ Package Design ○ Package Level LVS ○ FOWLP PDK and ADK support ○ Launches as 1st Mentor OSAT Alliance Program member	○ Design tool capacity and performance required when designing an Interposers with more than 200K pins	○ Package Planning ○ Package Level LVS

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Mentor vs. Tool C Comparison

	A	B	C
Netlist Management & Connectivity Planning (XSI)	☑	☑	☑
3D-IC Assembly Verification (LVS) (XSI – Calibre 3DSTACK)	☑	☑	☑
Layout Implementation (XSI – XPD)	☑	☑	☑

PKG Design Coverage	XPD / XSI	S**	A**
Single Die(Flip Chip)	✓	✓	✓
Wire Bonding	✓	✓	✓
Stacked Die / Multi-Die(2.5D/3D)	✓	✓	✗
Tackle all HDAP challenges – FOWLP etc	✓	Need to purchase option	✗
Interposer Based PKG	✓	✗	✗
ASIC - HBM Routing Automation	✓	✗	✗
Accurate error free the smallest area/plane fills	✓	✗	✗
Fast quality GDSII creation – error free	✓	Poor quality GDS(.sf) output	Poor quality GDS(.sf) output
Geometry based DRC with custom rules	Support through native application HyperLynx DRC with 72 Built-in rule ✓	Only as a paid service with 3rd party tool or SKILL language	Only as a paid service with 3rd party tool or SKILL language
Calibre(3D STACK DRC / LVS) integration for verification and signoff	True GDSII extraction, XSI with direct integration with Calibre 3DSTACK ✓	✗	✗
RLGC Parasitic Extraction	✓	Need to purchase 3rd party tool	Need to purchase 3rd party tool
3D Bump / Copper Pillar Modeling	✓	✗	✗
Multi-user real-time concurrent design	✓	Need to purchase option	✗
ODB++ import for design migration	✓	✗	✗
Automation Development	Allows most languages, including VBScript, Jscript, Tcl, Python, C ++ and others	SKILL Language only	SKILL Language only
Capacity and performance for >200K pin designs	✓	Poor Capacity, Tool Crashes & Performance	Poor Capacity, Tool Crashes & Performance

HETEROGENEOUS 3D IC - PKG PLANNING & PROTOTYPING

Xpedition Substrate Integrator

HDAP planning and prototyping

Xpedition Substrate Integrator

- Heterogeneous planning & prototyping
- System assembly and design mgmt.

Xpedition Package Designer

- Physical implementation
- Extraction
- In-process verification

Windows & Linux platforms

Calibre 3DSTACK DRC/LVS

- Verification

Calibre RVE

- Results visualization

Linux platform

OSAT Alliance Program (PDK/ADK enablement)

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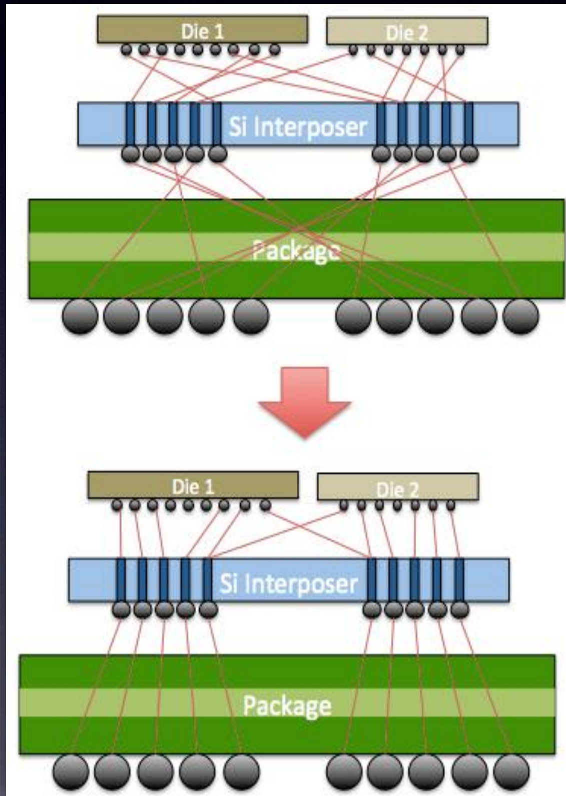
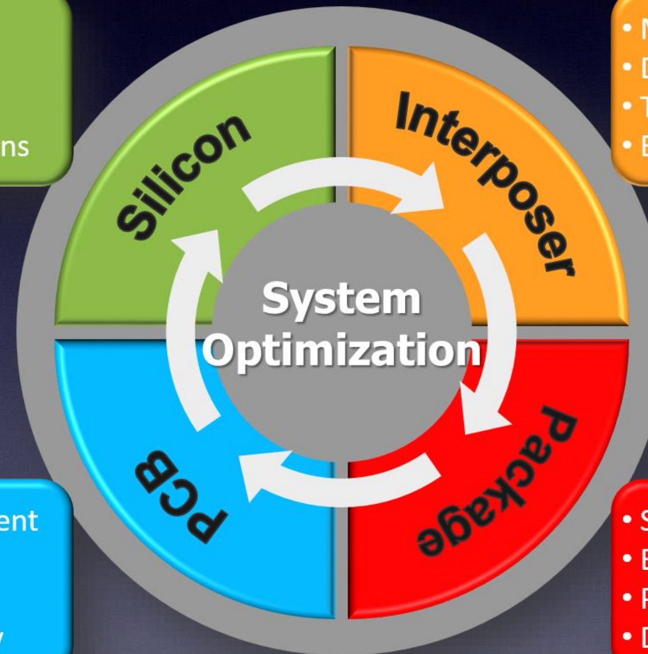
Heterogeneous planning and prototyping

Interdependences and impact



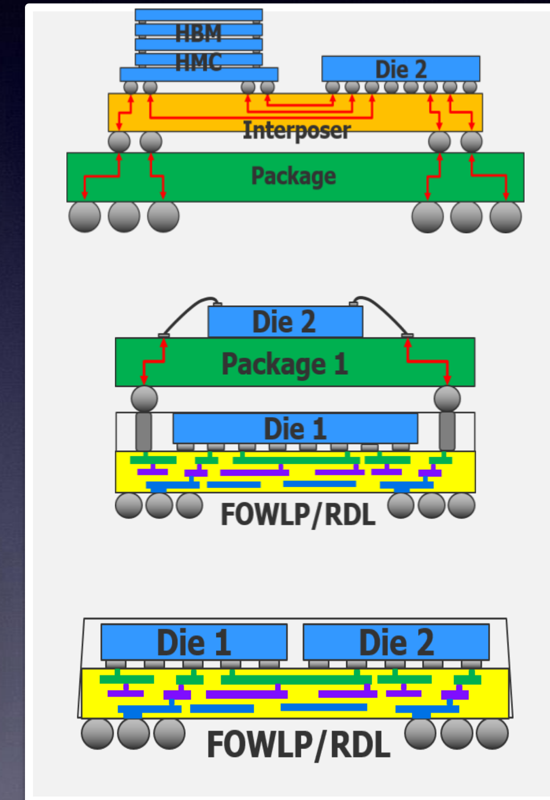
- Bump placement
- Signal – PG ratio
- Bump connectivity
- RDL tech and patterns

- Micro bump patterns
- Die to die connectivity
- TSV placement
- Bump pattern & nets



- Critical part placement
- BGA matrix & nets
- Escape routing
- Socket compatibility

- Substrate technology
- Ball matrix & net list
- PG supply strategy
- Die place & config



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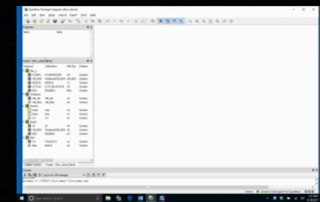
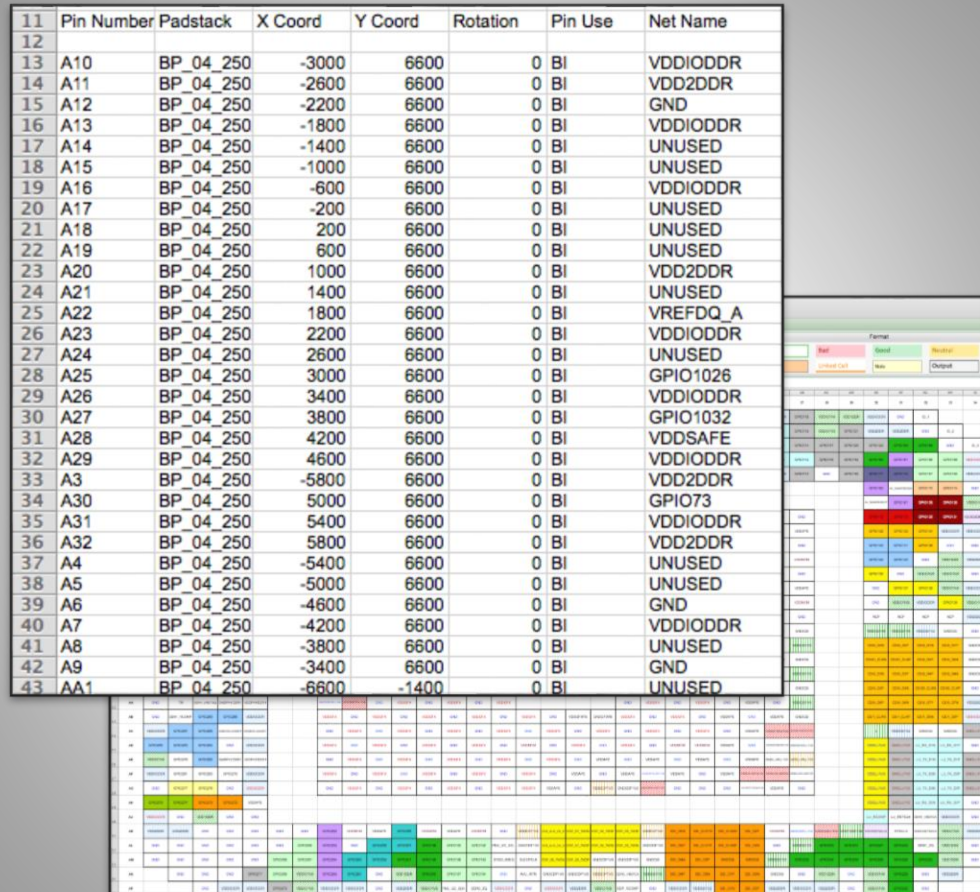
Spreadsheet based IO planning is failing





11	Pin Number	Padstack	X Coord	Y Coord	Rotation	Pin Use	Net Name
12							
13	A10	BP_04_250	-3000	6600	0	BI	VDDIODDR
14	A11	BP_04_250	-2600	6600	0	BI	VDD2DDR
15	A12	BP_04_250	-2200	6600	0	BI	GND
16	A13	BP_04_250	-1800	6600	0	BI	VDDIODDR
17	A14	BP_04_250	-1400	6600	0	BI	UNUSED
18	A15	BP_04_250	-1000	6600	0	BI	UNUSED
19	A16	BP_04_250	-600	6600	0	BI	VDDIODDR
20	A17	BP_04_250	-200	6600	0	BI	UNUSED
21	A18	BP_04_250	200	6600	0	BI	UNUSED
22	A19	BP_04_250	600	6600	0	BI	UNUSED
23	A20	BP_04_250	1000	6600	0	BI	VDD2DDR
24	A21	BP_04_250	1400	6600	0	BI	UNUSED
25	A22	BP_04_250	1800	6600	0	BI	VREFDQ_A
26	A23	BP_04_250	2200	6600	0	BI	VDDIODDR
27	A24	BP_04_250	2600	6600	0	BI	UNUSED
28	A25	BP_04_250	3000	6600	0	BI	GPIO1026
29	A26	BP_04_250	3400	6600	0	BI	VDDIODDR
30	A27	BP_04_250	3800	6600	0	BI	GPIO1032
31	A28	BP_04_250	4200	6600	0	BI	VDDSAFE
32	A29	BP_04_250	4600	6600	0	BI	VDDIODDR
33	A3	BP_04_250	-5800	6600	0	BI	VDD2DDR
34	A30	BP_04_250	5000	6600	0	BI	GPIO73
35	A31	BP_04_250	5400	6600	0	BI	VDDIODDR
36	A32	BP_04_250	5800	6600	0	BI	VDD2DDR
37	A4	BP_04_250	-5400	6600	0	BI	UNUSED
38	A5	BP_04_250	-5000	6600	0	BI	UNUSED
39	A6	BP_04_250	-4600	6600	0	BI	GND
40	A7	BP_04_250	-4200	6600	0	BI	VDDIODDR
41	A8	BP_04_250	-3800	6600	0	BI	UNUSED
42	A9	BP_04_250	-3400	6600	0	BI	GND
43	AA1	BP_04_250	-6600	-1400	0	BI	UNUSED

Spreadsheet based IO planning originally conceived for single die devices lacks the capacity, visualization, automation, and optimization required for multi-die heterogeneous systems

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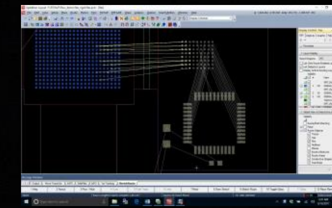
Single environment for silicon-package-PCB

Cross substrate connectivity planning and optimization



Project - [MultiDesignProject]

Name
- WBBGA
  - WB_DIE
  - WB_BGA
- REF_BOARD
  - WB_BGA
  - PCB_DRAM
  - PCB_CONN
  - FCBGA
- FC_BGA1
  - FCBGA
  - Bumps1

Device Hierarchy

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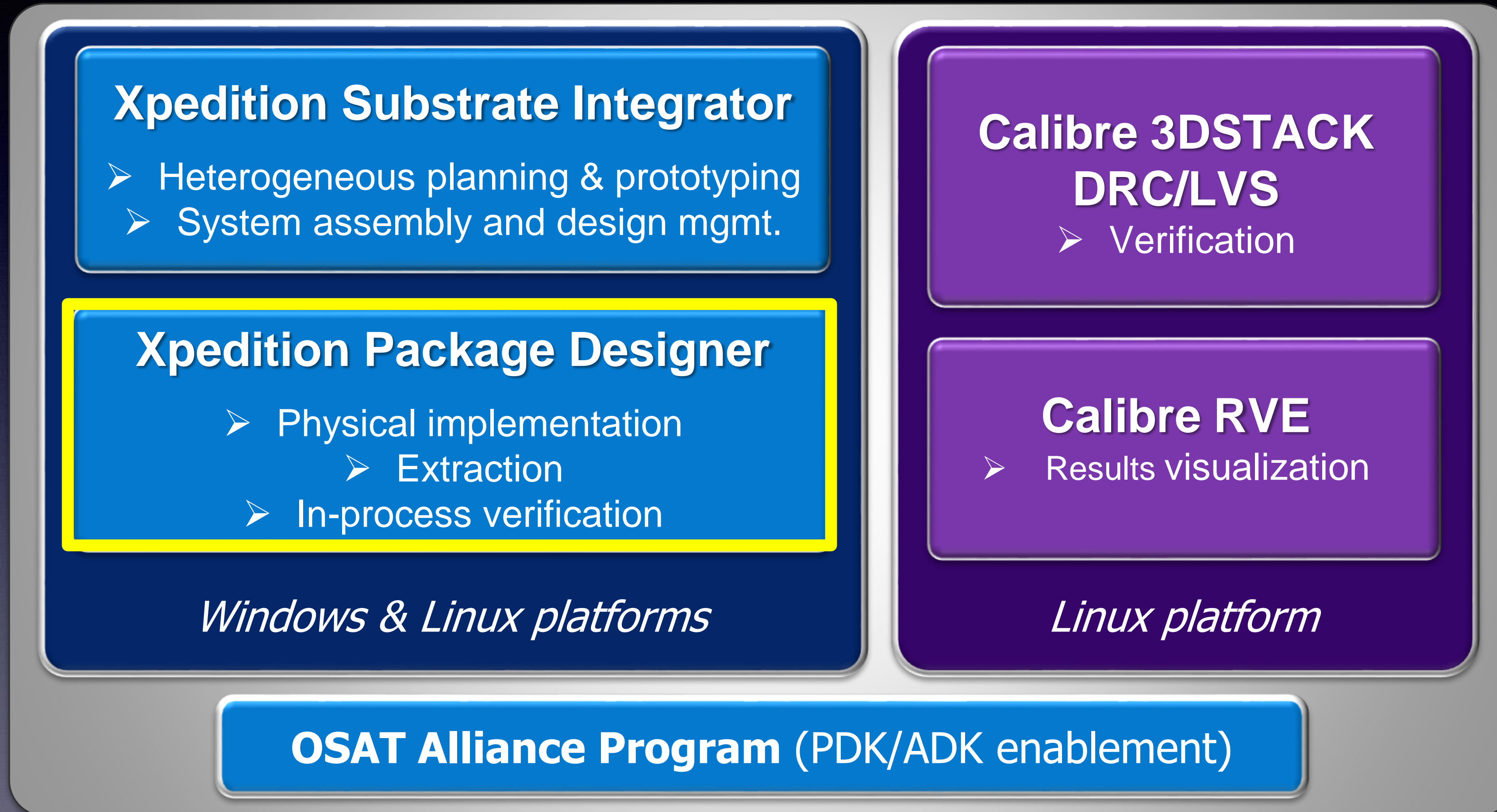
HDAP IMPLEMENTATION

Xpedition Package Designer

HDAP Implementation



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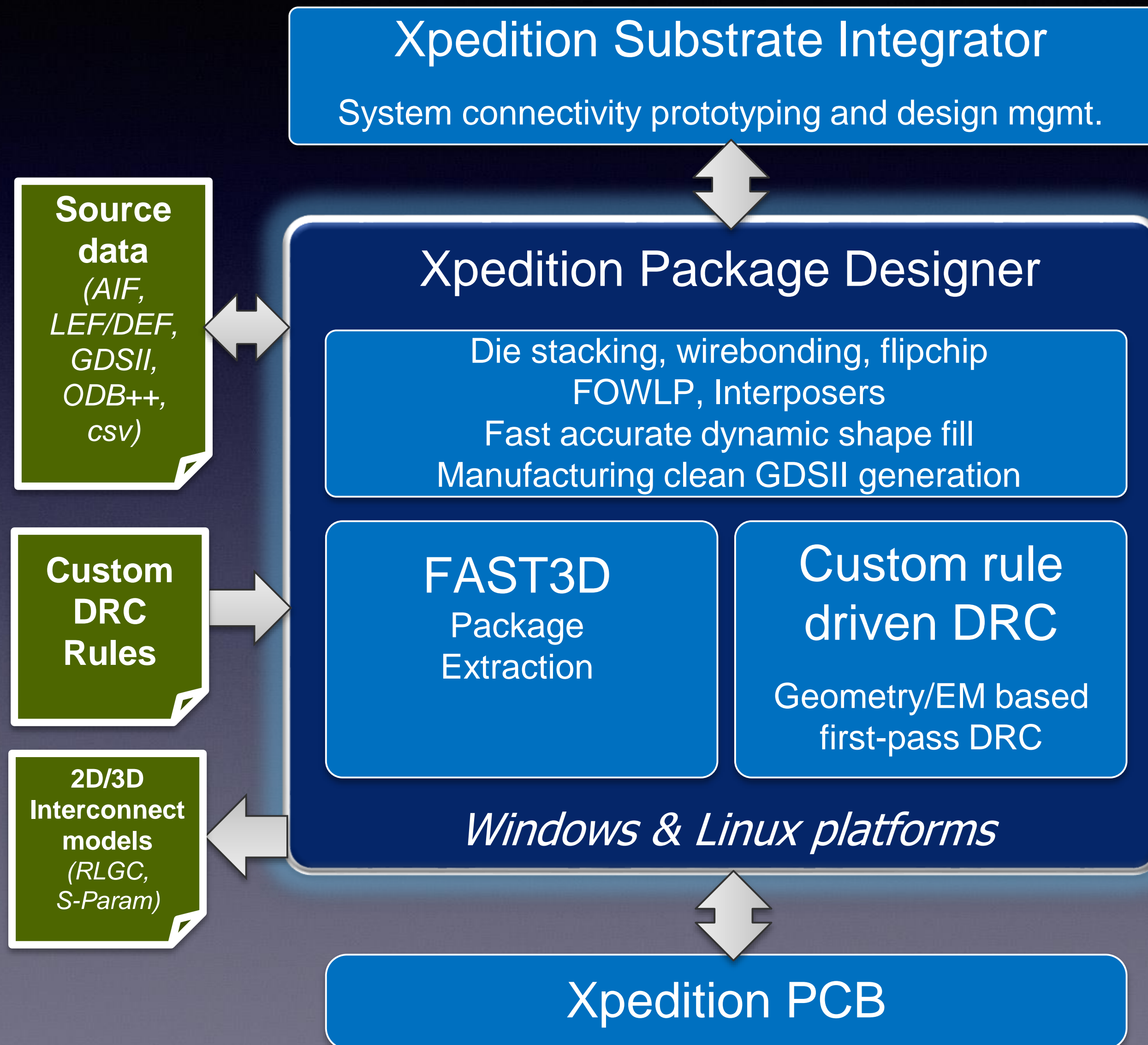
Xpedition Package Designer for HDAP



- Fully integrated 3D design environment
- Rapid physical prototyping with Layout Driven Design (LDD)
- Capacity and performance for the highest pin count designs – 250K+
- Complex areafill with accurate representation of smallest geometries
- Graduated degassing, metal balancing, dummy metal insertion and acute angle checking
- Quality GDSII of non-Manhattan shapes

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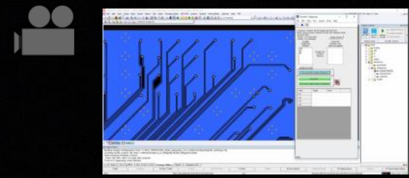
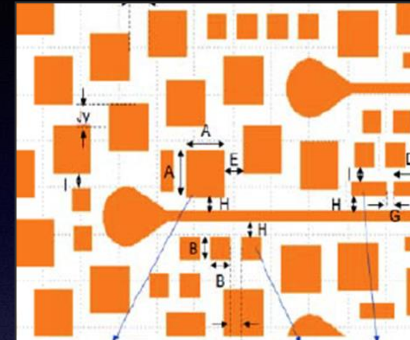
Xpedition Package Designer

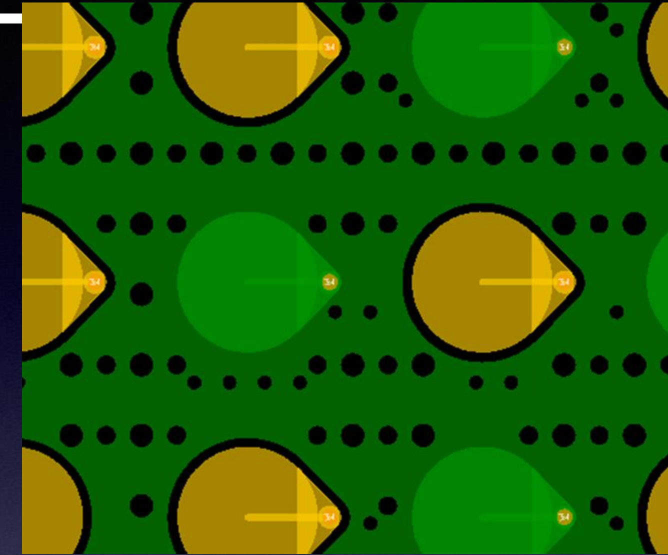
Advanced shape processing to meet complex requirements



- Supporting graduated degassing, metal balancing, acute angle checks, and stress relief features
- Automatic dummy metal insertion in layout database
  - Minimal performance impact
  - Ensure accurate electrical/thermal modeling
- Automatic metal balancing with degassing
  - Balance layer pairs to specified threshold
  - Iterates insertion/analysis of graduated degassing holes (see image)
  - Supports different shapes and configurations
- Produces quality GDSII of non-Manhattan shapes minimizes false verification errors



Dummy metal insertion



Pair layer density gap w/ degassing holes

Start	100	80	60
L02-91.4	L02-85.9	L02-85.9	L02-85.9
L03-95.5	L03-88.9	L03-88.9	L03-88.9
L01-84.6	L01-80.7	L01-80.7	L01-80.7
L04-91.9	L04-88.2	L04-85.9	L04-85.3

Target density w/degassing holes

Layer	Target	Start	100	80	60
L01	75-70	L01-84.4	L0...	L01-74.7	L01-74.7
L02	85-80	L02-92.1	L0...	L02-83	L02-83
L03	80-75	L03-95.9	L0...	L03-80.8	L03-80.[illegible]
L04	87-82	L04-92	L0...	L04-86	L04-86

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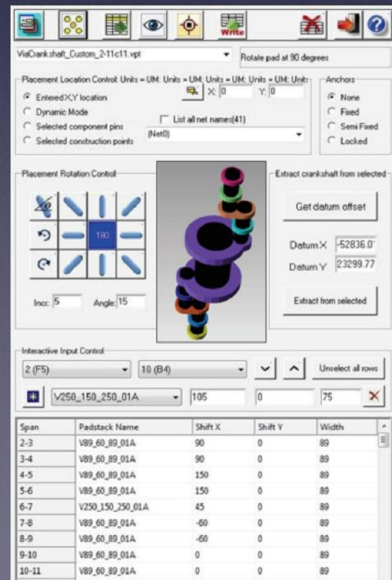
Xpedition Package Designer

Superior capacity and performance

- High pin count devices / designs
  - Multiple 10K+ pin devices
  - Capacity and performance
- Test case description
  - Interposer
  - GPU with four HBM stacks
  - 250K+ total pins
  - Four layers



Customer measured benchmark data

Design Operation	XPD	Tool C
Net list import	4 min.	3 min.
Save – just die/pkg	No delay	8 min.
Save - w/planes and degassing	25 sec. ⟷	9 min.
Change padstack	2 min.	7 min.
Plane generation – one layer	No delay ⟷	12 min.
Degass hole generation – one layer	10 sec. ⟷	55 min.
Degass hole generation – all (4) layers	1 min.	No function
Add staggered via – all die pads	2 min.	No function
Copy metal planes to all layers	1 min.	No function
Gerber export	3 min. ⟷	30 min.

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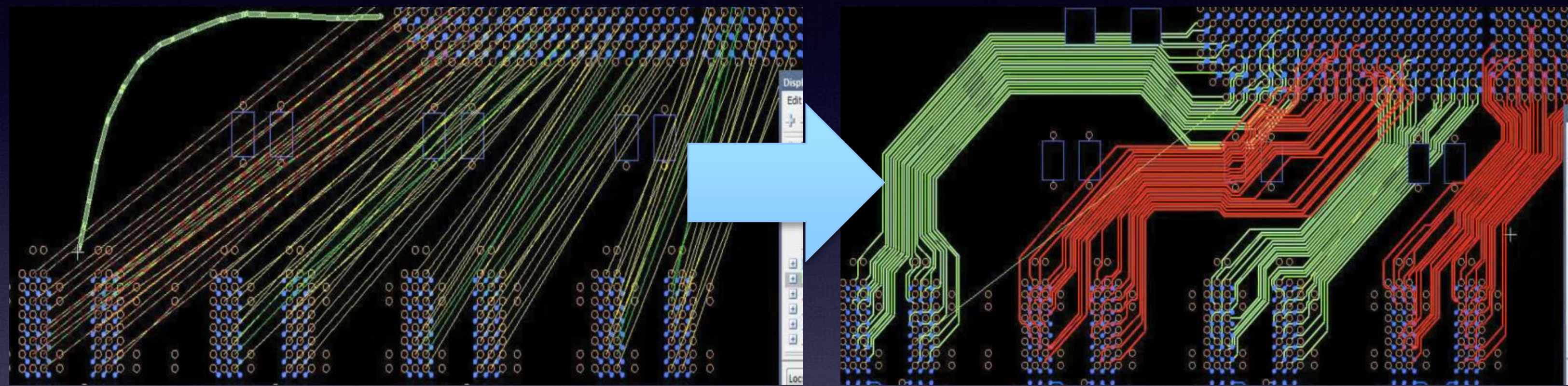
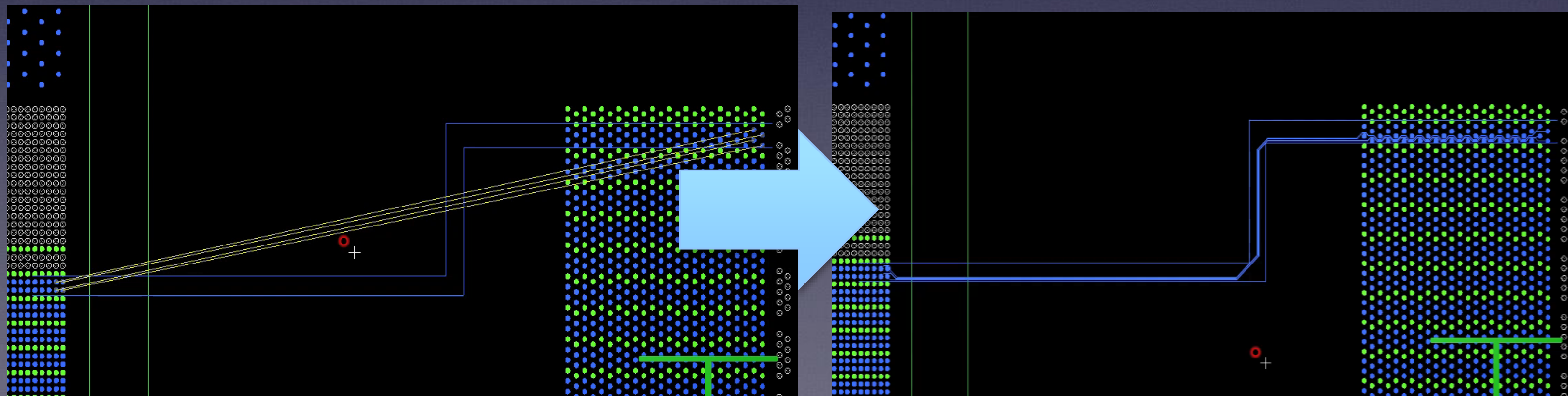
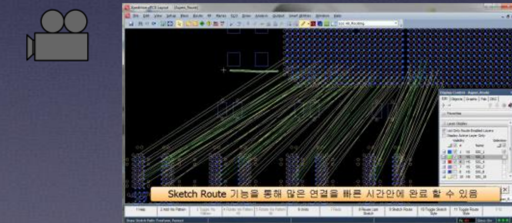
Sketch Technology and HBM Routing Reuse

- Manual-routing quality in a fraction time





- **Sketch Route & Planner**
- **Sketch Route for HBM Routing**
- **HBM Routing Reuse**



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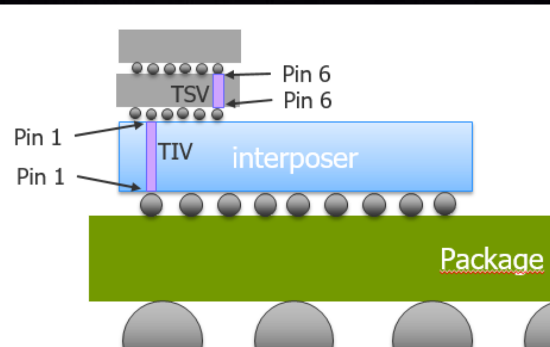
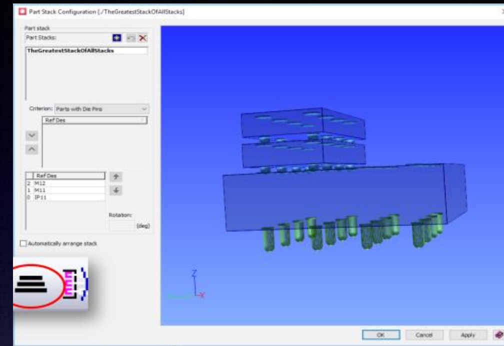
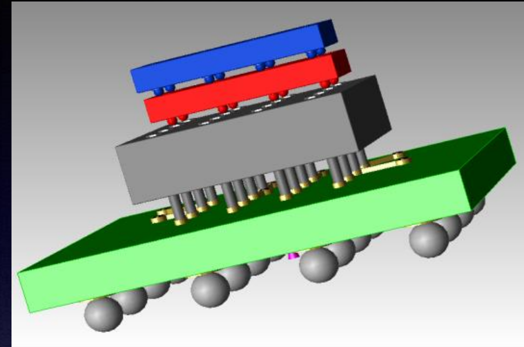
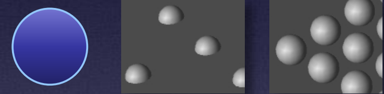
Xpedition Package Designer

2D/3D editing, visualization and DRC

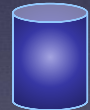




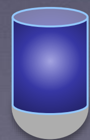




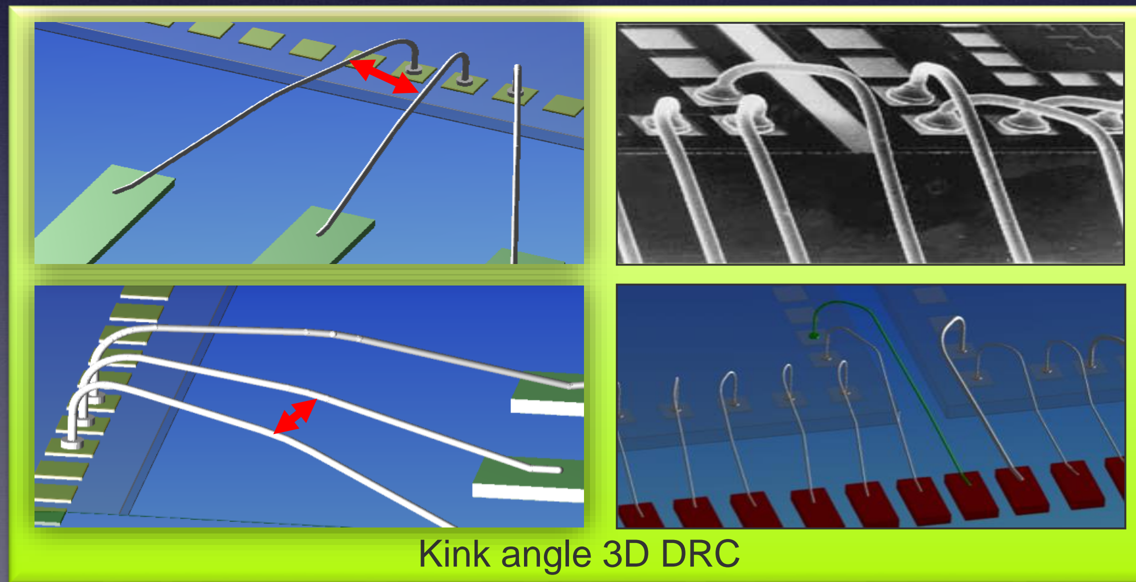
Ball



Copper Pillar



Capped Copper Pillar



Kink angle 3D DRC

- Design and verify complex packages in a fully supported 3D environment
- Supporting interposer, stacked-FOWLP, and stacked die applications
- Real-time 3D wire bonding for the most complex multi-die packages
- Component stack dialogue and Xpedition 3D view will use 3D pin models and apply automatic 3D modelling to visualize solder balls or die bumps

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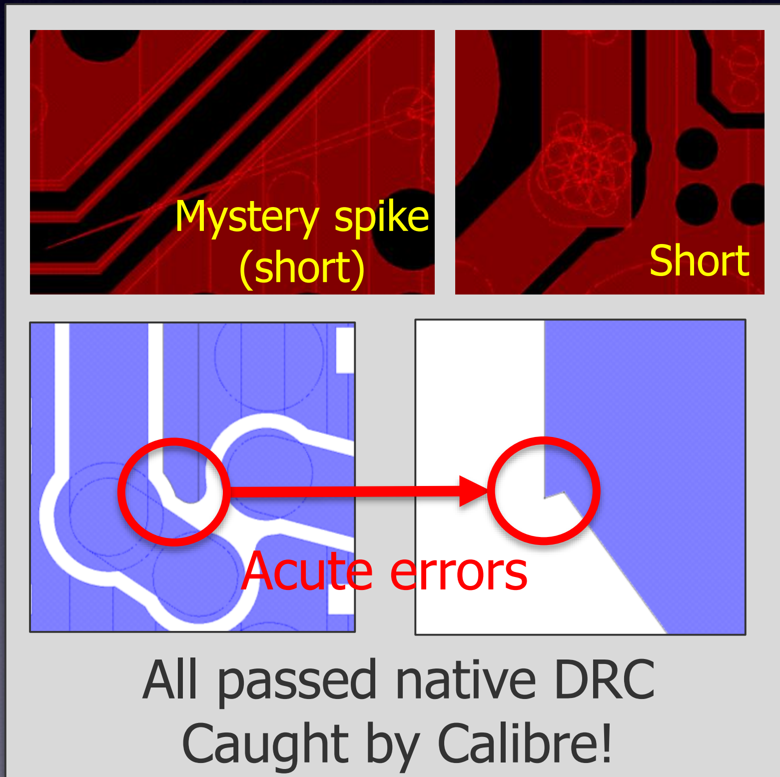
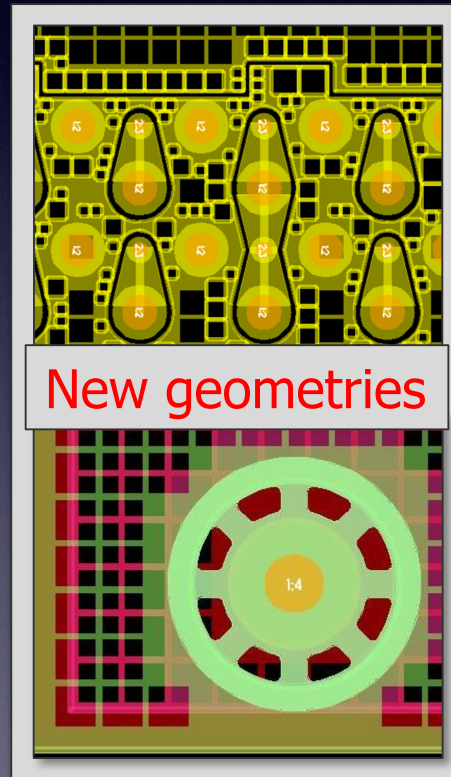
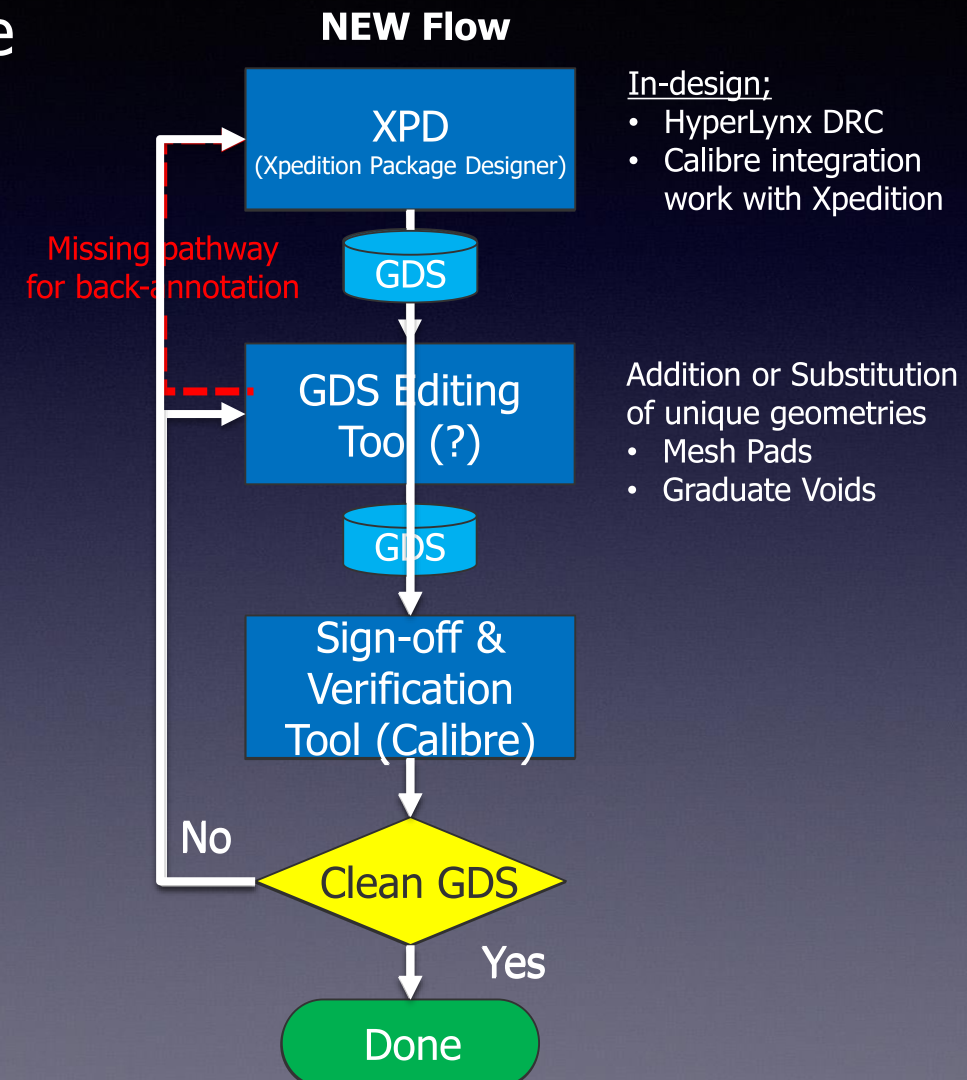
Common GDS Quality and Accuracy Issues

- GDS edits never back-annotate to layout database
- Layout database out of sync with outputs







In-design;
- HyperLynx DRC
- Calibre integration work with Xpedition

Addition or Substitution of unique geometries
- Mesh Pads
- Graduate Voids

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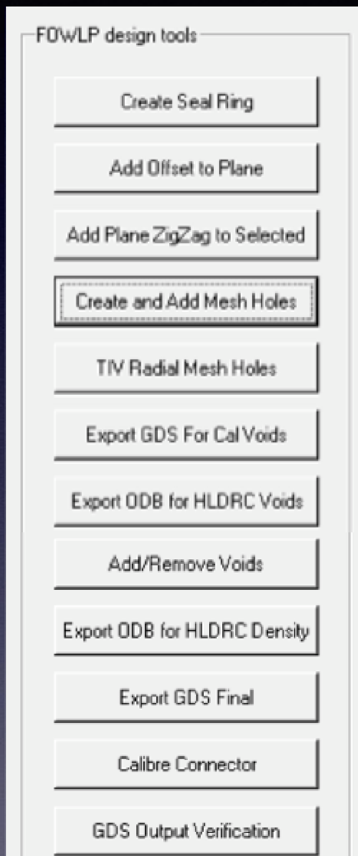
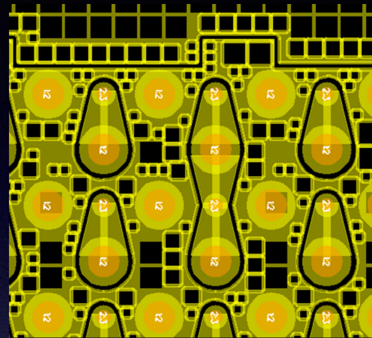
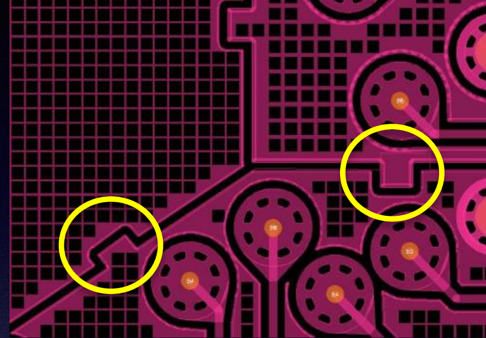
Dedicated FOWLP Technology Kit

Specialized functionality in a comprehensive flow

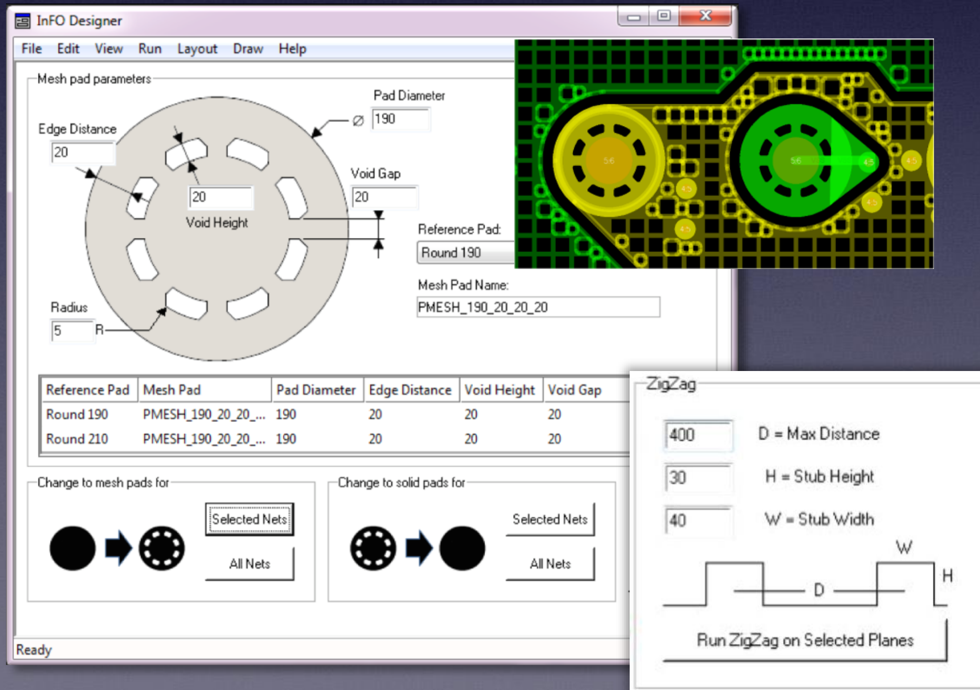




Graduated degassing voids



Stress relief



- Certified layout and verification flows for TSMC InFO WLP processes
- New innovative layout functionality specifically for FOWLP
  - Allows for multi-size degassing hole with incrementally smaller voids
  - Allows easily for customized teardrop on rule based
  - Automated stress relief features Fast optimized GDS output
- Dedicated support resources for rapid design kit development

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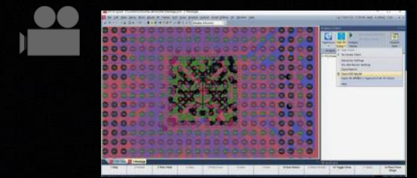
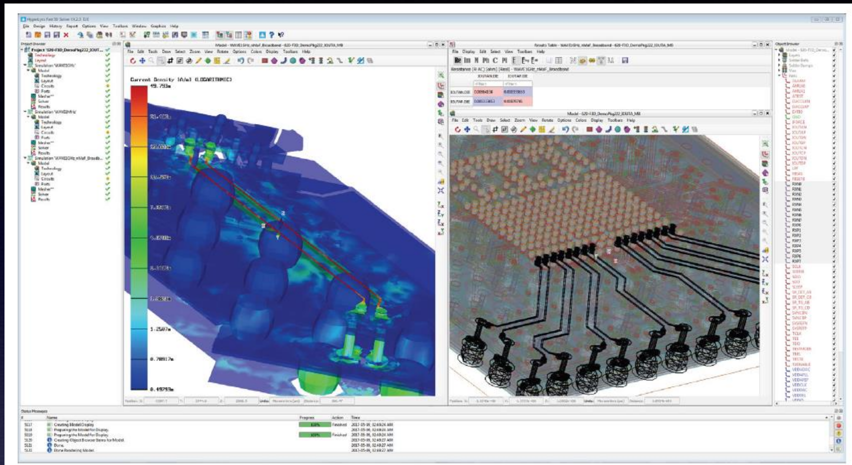
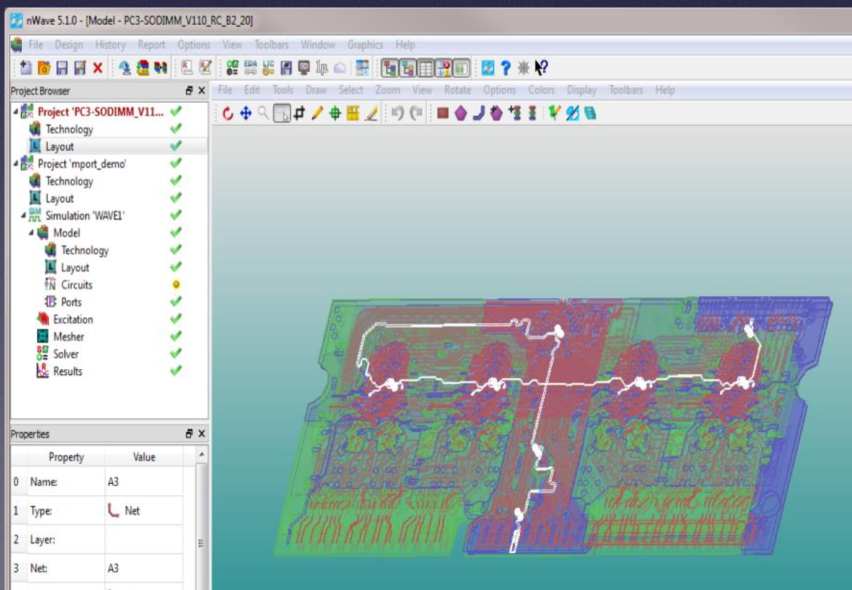
Analysis of the Entire Package/System

Powered by HyperLynx







- Embedded HyperLynx 3D quasi-static field solver for package model creation
  - Handles all package design styles
  - Generates SPICE, IBIS and RLCG matrices
- 3D Full-wave, Chip to System analysis
  - Speed, scale, and accuracy competitive advantages
  - Generates S-Parameters and EMI/EMC field plots
- High Performance SI/PI analysis
  - Generates S-Parameters for SI/PI/SSO analysis
  - Calculates loop inductance, DC drop, current density

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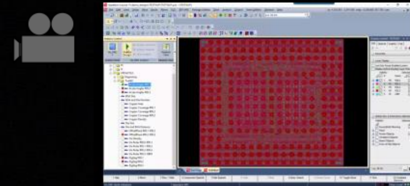
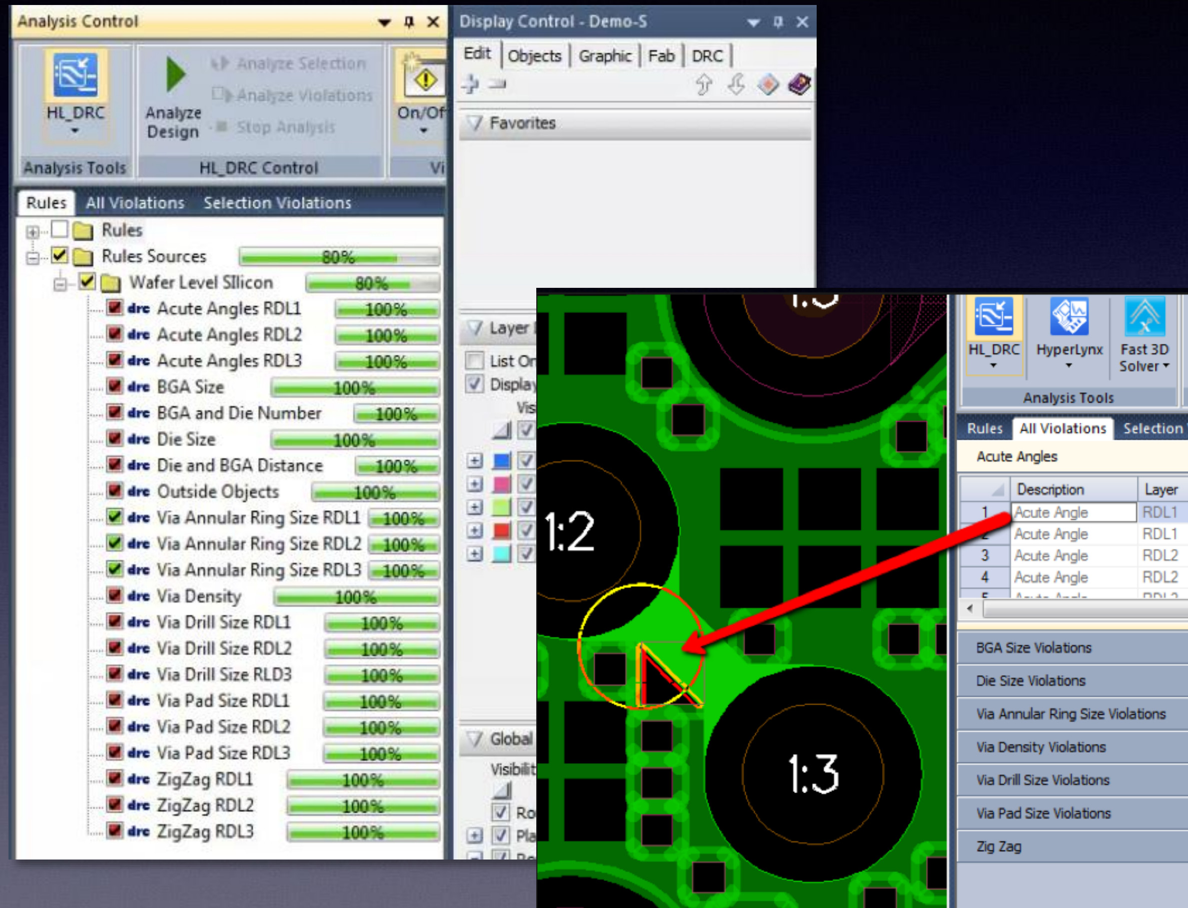
Xpedition Package Designer

Independent in-process verification





Unique in-design verification (HyperLynx DRC)

- Addresses the rapidly changing complex rules of HDAP/FOWLP
  - Automates checking of new or non-standard rules
  - Supports both physical and electrical checks
- Combines powerful geometry processing engine with field solver technology
  - Built in checks for EMI, SI, PI
  - User definable custom rules
- Identify and resolve most problems before final sign-off
  - Same platform as design tools
  - Easy to use, fast, and accurate

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Xpedition Package Designer

Industry standard languages for automation development

- COM Automation exposes a language independent library of functions.
- Choice of scripting languages:
  - VBScript, Jscript
    - Provided with Windows by Microsoft
    - Provided with MainWin by Mainsoft
  - Tcl
    - Support for Windows and Linux
    - Provided by Mentor with COM bindings for Windows and Linux
  - Perl, Python, Java and others
    - Perl and Python - Windows only, from http://www.activestate.com
- C/C++, Visual Basic, etc. can be used as well

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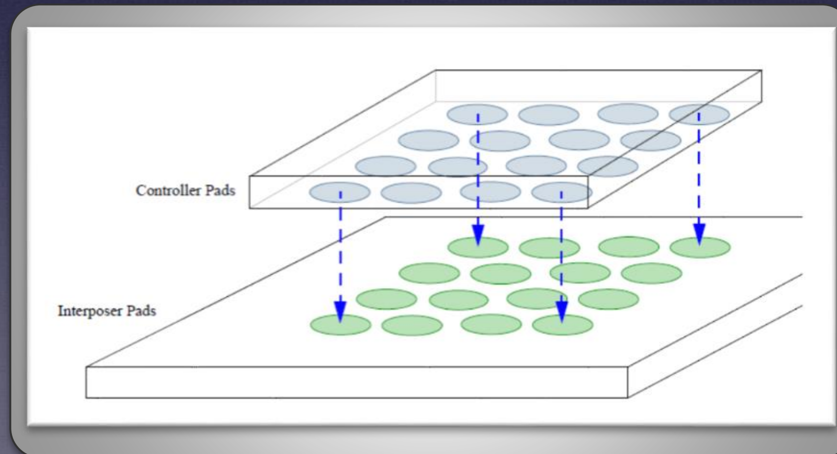
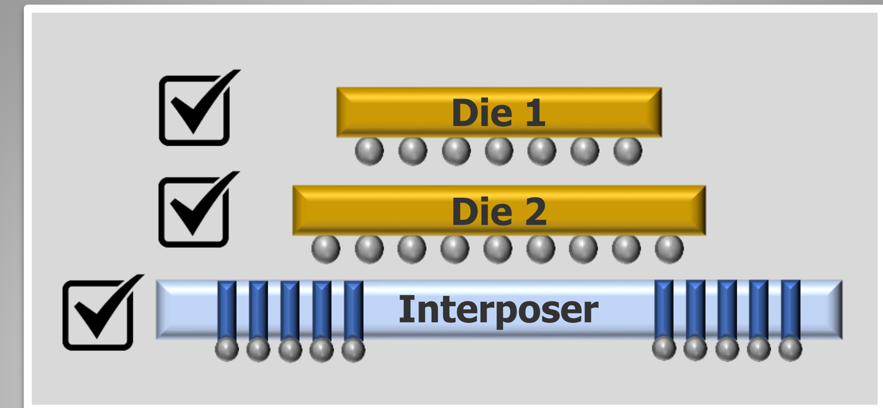
HETEROGENEOUS 3D IC - PKG ASSEMBLY VERIFICATION

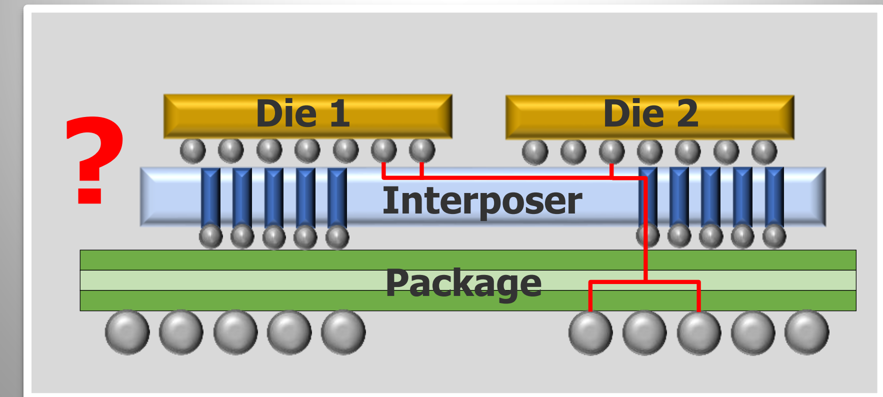
Individual device verification isn't enough

Independently verifying discrete die and substrates per their process rules does not ensure the overall 2.5D/3D package assembly is correct or will perform as expected



Physical (DRC and LVL)





Logical (LVS)

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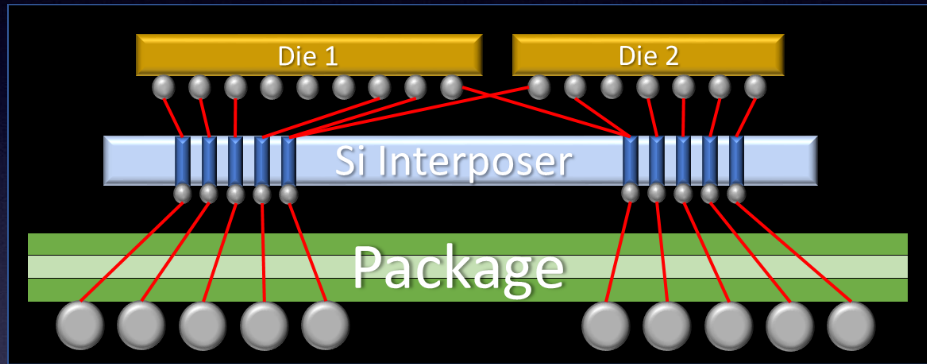
2.5D/3D heterogeneous package verification needs



Incorporate silicon verification requirements and methods into package design

- Established flows for silicon but it's a new concept for interposers and packages
- System assembly using standardized formats
  - ODB++, CSV, AIF, LEF/DEF, GDS, etc…
  - Compatibility with existing design flow
- Physical checks across substrate interfaces
  - Alignment, scaling, overlaps
- Connectivity verification between all components and substrates
  - Connectivity between connected shapes
  - Mismatch connections
  - Verify locations of electrical pins
- Synchronization with package database

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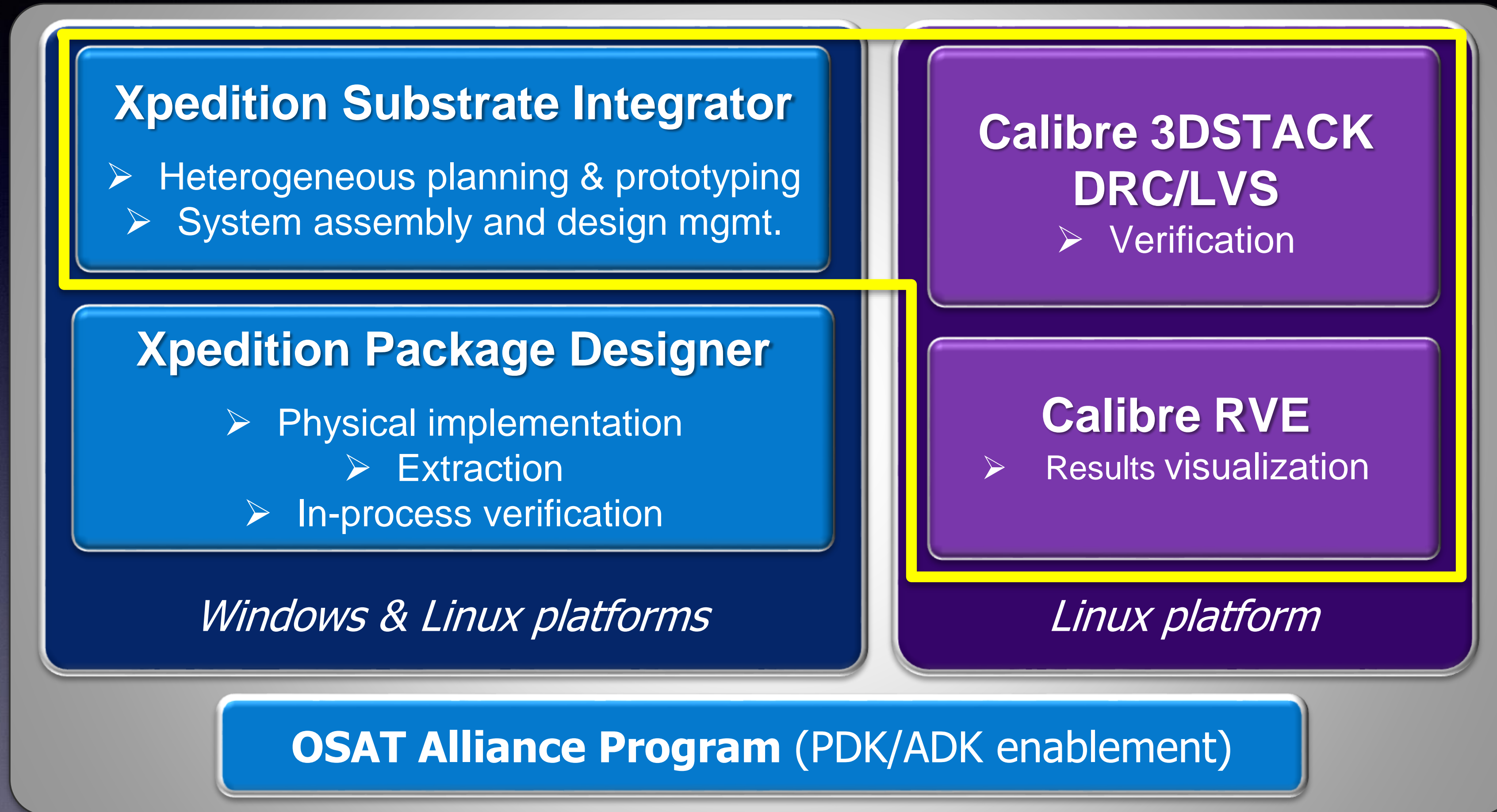
Xpedition Substrate Integrator & Calibre 3DSTACK



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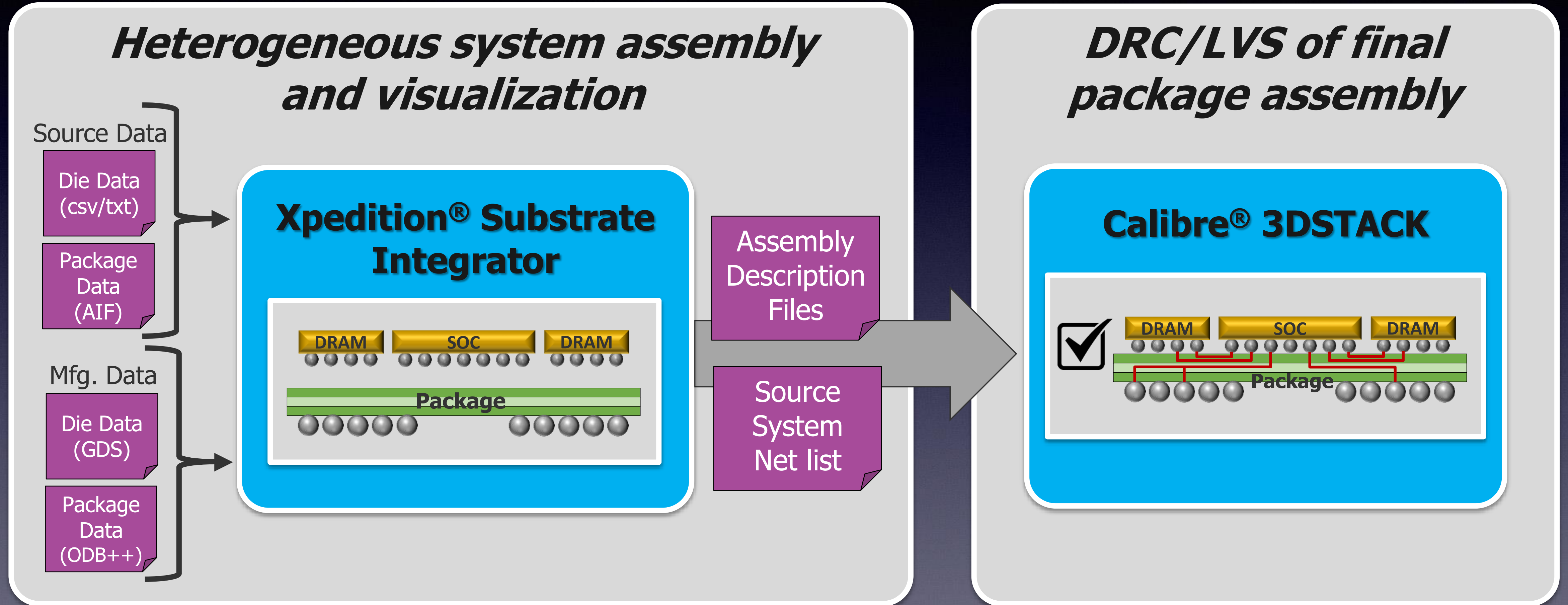
Xpedition Substrate Integrator & Calibre 3DSTACK

2.5D/3D package assembly verification flow



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XSI – Calibre 3DSTACK Integration

Sign-Off & Verification

XSI Calibre 3DSTACK Wizard

Expand All | Collapse All
Include | Exclude
Move Up | Move Down
Move To Top | Move To Bottom
Move In | Move Out
Add Tier | Remove Tier
Load Design ... | Load Project ...
Load Config ... | Save Config ...
Close | Reset

One Click 3DSTACK Deck

Calibre 3DSTACK Configuration

- Include
  - Bottom I14 <Crystal_35_Bottom_I14>
  - Crystal_35
  - Top I01 <Crystal_35_Top_I01>
    - CRYSTAL3
    - DDR3_0
    - DDR3_1
    - DDR3_2
    - DDR3_3
    - DDR3_4
    - DDR3_5
    - DDR3_6
    - DDR3_7
    - C1
    - C10
    - C11
    - C12
    - C13
    - C14
    - C15
    - C16
    - C17
    - C18
    - C19
    - C2

Assembly Connect | Assembly Stack | Assembly Checks | 3DSTACK Netlist | Main (main.3ds+) | Run Cont

Calibre 3DSTACK Assembly Connect

./assembly_die.3ds+ — Die 3ds+ File ...
./assembly_package.3ds+ — Interposer 3ds+ File ...
./generate_die.tcl — Generate Die Tcl File ...

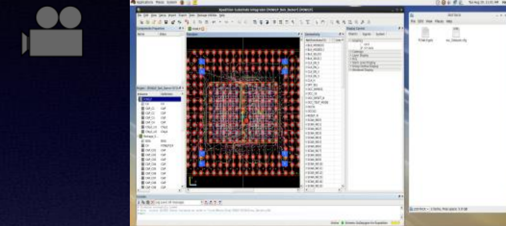
Generate
- Die Assembly
- Interposer Assembly
- Generate Die Script

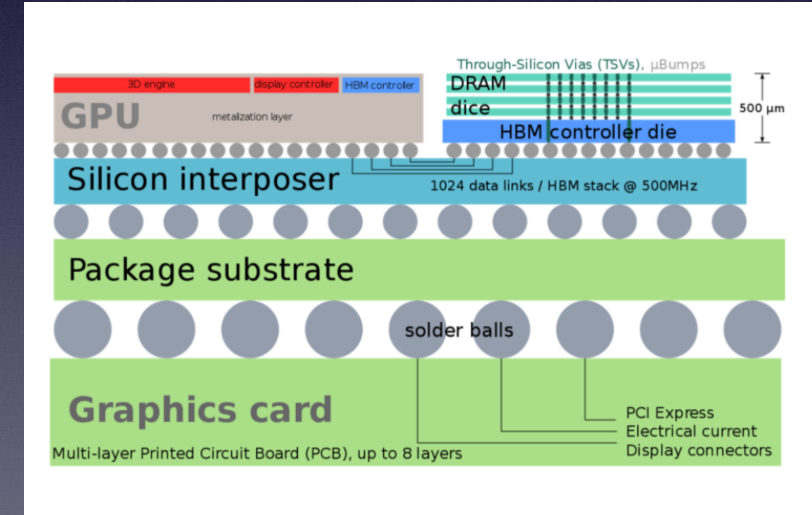
Generate
Reset
Save
Setup Device Assembly from GDS File

Calibre 3DSTACK Assembly Connect Command

```
die -die_name Crystal_35 -package \
    -layout {
        -primary TOP
        -path    ./Crystal_35.gds
        -type    gdsii
    } \
    -thickness 500 \
    -layer_info {
        -type   101
        -name   101
        -layer  10:1
        -top
        -ext_connect
    } \
    -layer_info {
        -type   101_102
        -name   101_102
        -layer  20:12
    } \
    -layer_info {
```

Ready | XSI Project: /home/xpi/DemoInventory/Crystal_35/Crystal_35/Crystal_35.xpf | XSI Calibre 3DSTACK Wizard | v1.4





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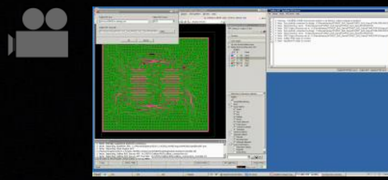
XPD – Calibre 3DSTACK Integration

Sign-Off & Verification



XPD

Calibre

Real-time integration between Xpedition and Calibre

Package Utilities | RTP AATK | Draw | Analysis | Output | Smart Ut

Setup
Import
Export
Pathfinding
Report
Calibre Integration
Launch File Explorer
About Package Utilities

Acute Angle Check
Layer Density Check
Run Calibre Rule Deck
Calibre RVE Server

Integrated with Xpedition Package Designer, Calibre provides final mask signoff

- Inter-tool communication enables dynamic cross-probing
- Independently verify manufacturing output with Calibre
- Physical DRC including 3D interfaces
- Multi-domain connectivity checking (LVS) from die through package
- Quickly identify and resolve issues with direct Xpedition/Calibre integration
- Works across Windows /Linux

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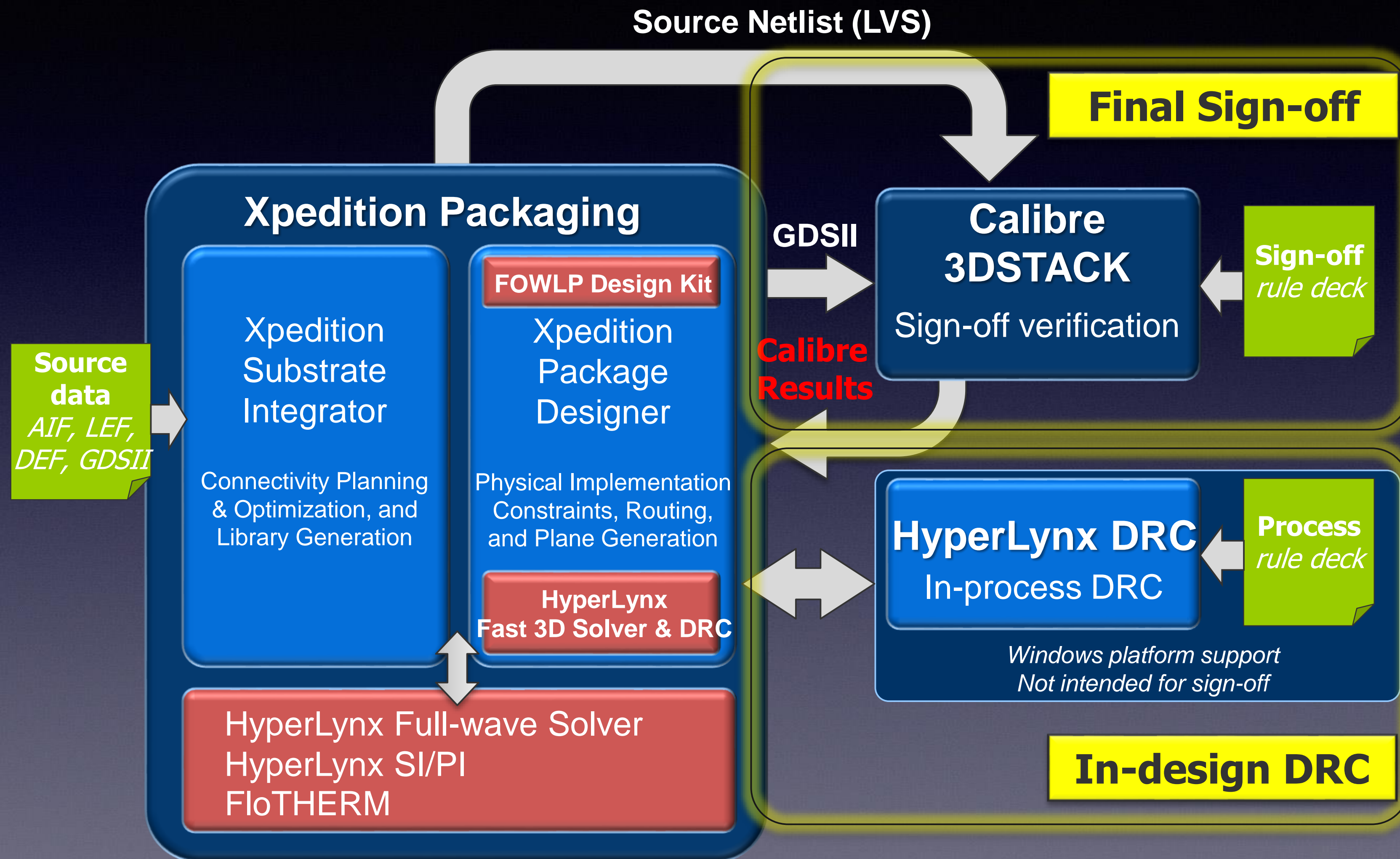
SUMMARY

Summary

3D IC-Package Verification & Implementation



- Substrate management and system connectivity planning with **Xpedition Substrate Integrator** (XSI)
- Package implementation with **Xpedition Package Designer** (XPD) supported by vendor specific FOWLP design kit
- Work-in-progress (WIP) design verification with **HyperLynx DRC** using vendor specific HLDRC rules
- Final sign off with **Calibre DRC**, **LVS** and **3DSTACK** using vendor specific rule deck(s)

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