



INTRODUCING THE FPGA FOR THE DATA-CENTRIC WORLD

Webinar



Today's Discussion

Markets are Transforming

A New Class of FPGA (with a New Name)

Solving Big Market Challenges

Massive Data Driving Market Change

**RAPID MARKET
TRANSFORMATION**

**MASSIVE
INNOVATION**

**HIGHLY
CUSTOMIZED
HW & SW**

BY 2020¹

AVERAGE INTERNET USER	1.5GB DATA/DAY
SMART HOSPITAL	3TB DATA/DAY
AUTONOMOUS AUTOMOBILE	4TB DATA/DAY

CONNECTED AIRPLANE	40TB DATA/DAY
SMART FACTORY	1PB DATA/DAY

¹ Amalgamation of analyst data and Intel® analysis

Rapid Market Transformation Driving Innovation

**EMBEDDED /
EDGE**

NEC

ZTE

**COMMUNICATIONS
INFRASTRUCTURE**

Rakuten

**China
Mobile**

**CLOUD /
ENTERPRISE**

Microsoft

Alibaba

New Demands Driving Customization Needs

**EMBEDDED /
EDGE**

**Real-Time Actionable
Intelligence**

**COMMUNICATIONS
INFRASTRUCTURE**

**High-Bandwidth
Aggregation & Processing**

**CLOUD /
ENTERPRISE**

**Managing, Organizing &
Processing the Explosion
of Data**



Introducing Intel® Agilex™ FPGAs

**Intel innovation for ultimate
agility and flexibility**



HIGH-PERFORMANCE COMPUTE

10nm Process

Memory-Coherent Intel® Xeon®
Processor Acceleration

Massive Bandwidth

ANY-TO-ANY INTEGRATION

Memory, Analog, Logic

Any Node, Supplier, IP

Rapid Intel® eASIC™
Devices Optimization

ANY DEVELOPER

Intel® Quartus® Prime
Design Tool for
Hardware Developers

One API for Software
Developers

The FPGA for the Data-Centric World

PROCESS DATA

2ND GENERATION
INTEL[®]
HYPERFLEX[™]
ARCHITECTURE

UP TO
40%
HIGHER
PERFORMANCE^{1,3}

UP TO
40%
LOWER
POWER^{1,3}

UP TO
40 TFLOPS
DSP PERFORMANCE^{2,3}

STORE DATA

DDR5 &
HBM

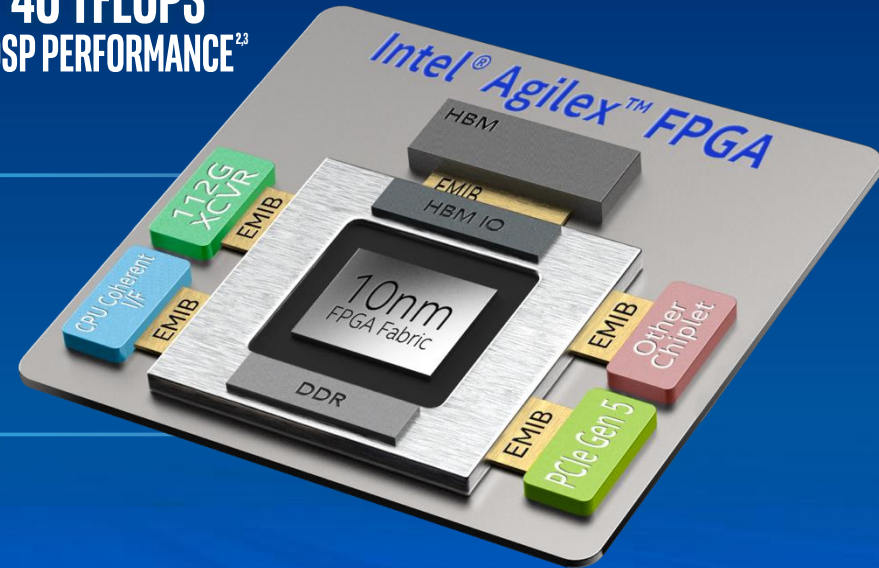
INTEL[®] OPTANE[™] DC
PERSISTENT MEMORY SUPPORT

MOVE DATA



INTEL[®] XEON[®] PROCESSOR COHERENT
CONNECTIVITY & PCIe GEN5

112G
TRANSCIVER
DATA RATES



¹ Compared to Intel[®] Stratix[®] 10 FPGAs

² With FP16 configuration

³ Based on current estimates, see slide 23 for details

Any-to-Any Heterogenous 3D Integration

EMBEDDED MULTI-DIE INTERCONNECT BRIDGE

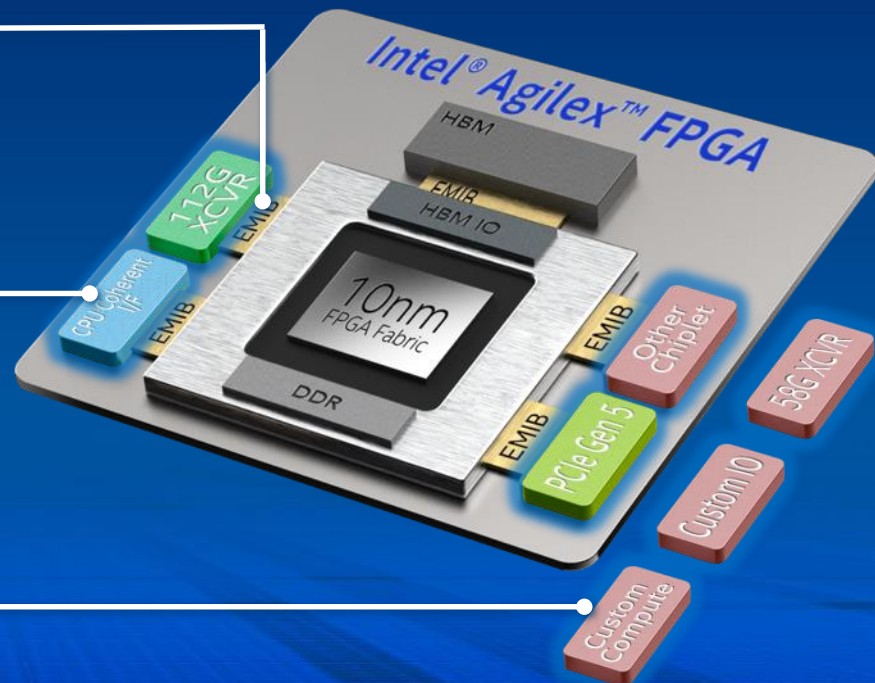
No-compromise die-to-die
3D packaging interconnect

CHIPLET-BASED ARCHITECTURE

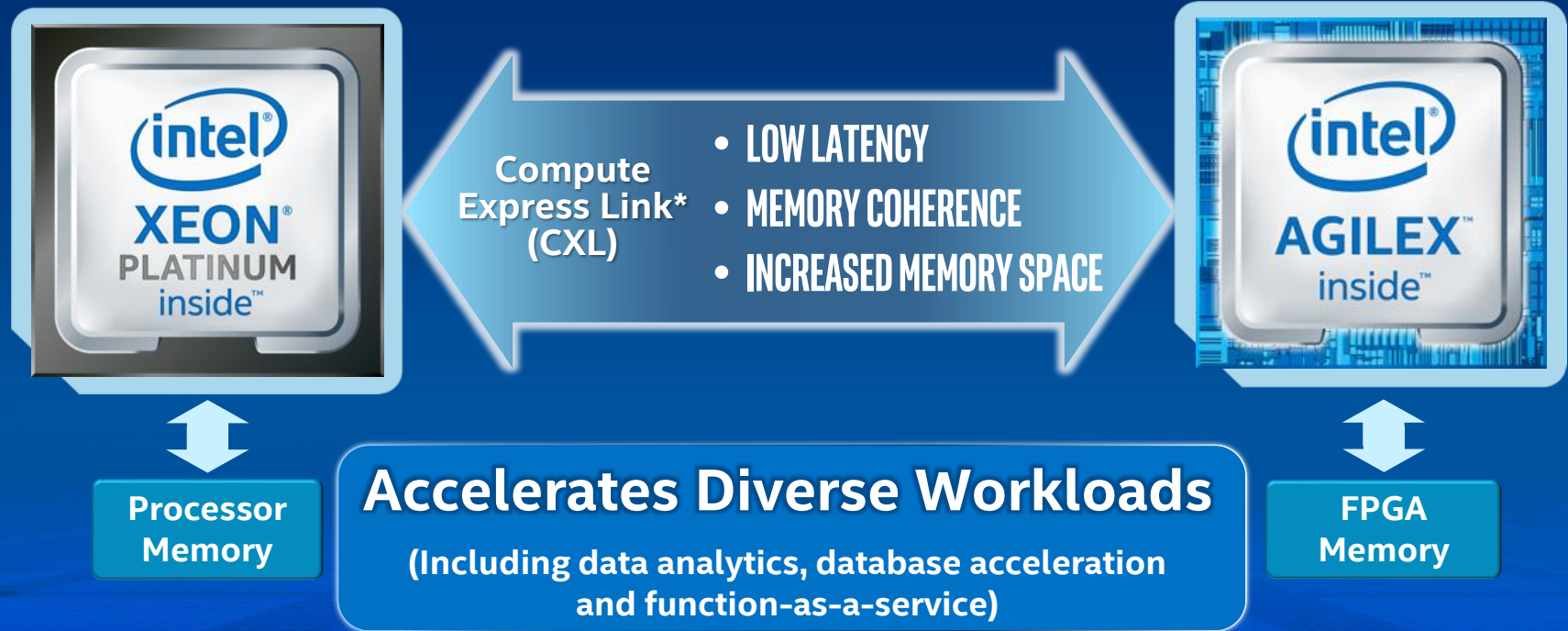
Library of chiplets:
transceivers, custom I/O &
custom compute tiles

INTEL® eASIC™ TILE CUSTOMIZATION

Ultimate customization with
integrated Intel® eASIC™ tile



First Memory-Coherent Accelerator for Intel® Xeon® Scalable Processors

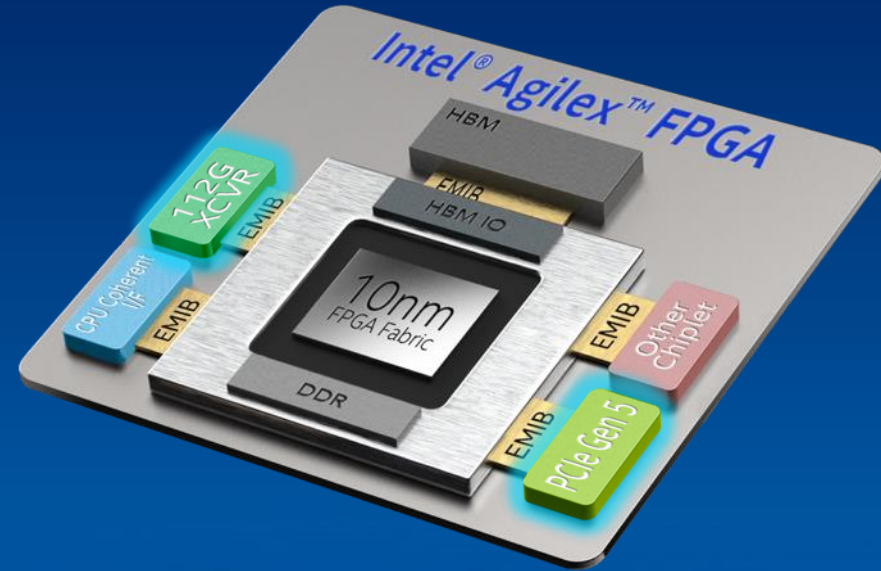


Transceiver Leadership

112G



PCIe^{*} GEN5



**High Bandwidth for Applications Including
400G Networks, Edge Analytics, Data Center Workloads**

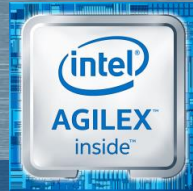
Well Suited for Artificial Intelligence Applications

UP TO
40 TFLOPS³
FP16 PERFORMANCE

UP TO
92 TOPS⁴
INT8 PERFORMANCE

Configurable DSP

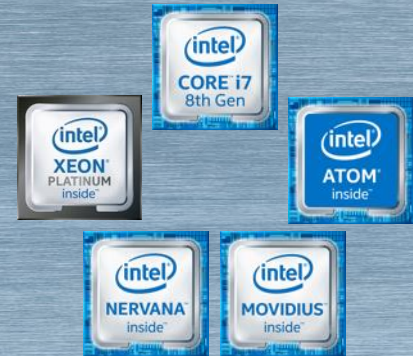
- FP32
- BFLOAT16
- FP16
- INT8 through INT2



AI+ Usage Model:
Flexibility for evolving workloads and multi-function
integration (networking, ingest, security, etc.)

Only FPGA supporting hardened
BFLOAT16 & FP16

Complementary to:



OpenVINO™ toolkit

One API

^{3,4} based on current estimates, see slide 23 for details

Intel® Agilex™ FPGA Tools for Developers



ONE API

Hardware Developers

- Higher productivity:
 - 30% improvement in compile times⁵
 - New productivity flows and usability features for faster design convergence
- Higher efficiency: 15% improvement in memory utilization⁵

Software Developers

- Single source, heterogeneous programming environment
- Support for common performance library APIs
- FPGA support with Intel software development tools including Intel® VTune™ Amplifier & Intel® Advisor



⁵See slide 23 for details

Intel® Agilex™ FPGA Family

F - SERIES

For wide range of applications

Up to 58G transceivers

PCIe* Gen4

DDR4

Quad-Core ARM* Cortex*-A53
SoC Option

I - SERIES

For high-performance
processor interface and
bandwidth-intensive applications

Up to 112G transceivers

PCIe* Gen5

DDR4

Quad-Core ARM* Cortex*-A53

Coherent attach to Intel® Xeon®
Scalable Processor option (CXL)

M - SERIES

For compute-intensive applications

Up to 112G transceivers

PCIe* Gen5

DDR4, DDR5 and Intel® Optane™
DC Persistent Memory support

Quad-Core ARM* Cortex*-A53

Coherent attach to Intel® Xeon®
Scalable Processor option (CXL)

HBM Option

**Intel® Quartus® Prime Design Software Support April 2019;
First Device Availability Q3 2019**

Massive Market Demand

2023 SILICON TAM* > \$20B

Edge Inference
Industrial
Military/AERO

**EMBEDDED /
EDGE**

5G
NFV
Optical Networks

**COMMUNICATIONS
INFRASTRUCTURE**

Financial
Database
AI
Genomics

**CLOUD /
ENTERPRISE**



Efficient Network Transformation

DATAPATH ACCELERATION

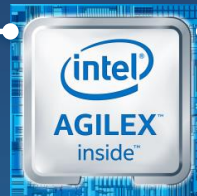
VNF PERFORMANCE OPTIMIZATION

Load Balancing | Data Integrity
Network Translation

SIGNIFICANT IMPROVEMENTS¹

Throughput | Jitter | Latency

28G-112G
per channel



PCIe Gen 4/5



INFRASTRUCTURE OFFLOAD

OPTIMIZED ARCHITECTURE

vSwitch | vRouter | Security

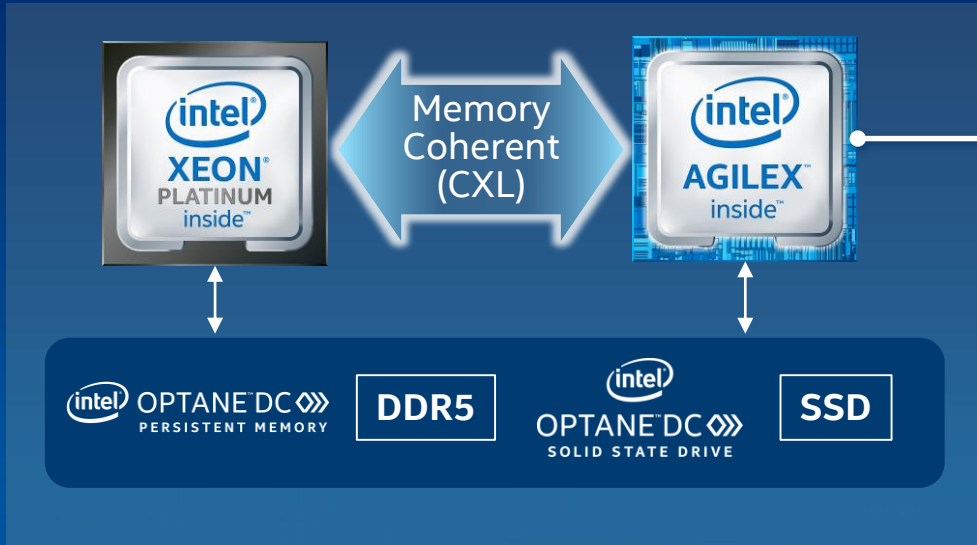
SMALL FORM FACTOR & LOW POWER

Wide Range of Servers

First FPGA Providing Flexibility and Agility From 100Gbps to 1Tbps

¹ Compared to Intel® Stratix® 10 FPGAs

Converged Workload Acceleration for the Datacenter



INFRASTRUCTURE ACCELERATION

Network | Security | Remote Memory Access

APPLICATION ACCELERATION

AI | Search | Video Transcode | Database
40 TFLOPs of DSP Performance¹

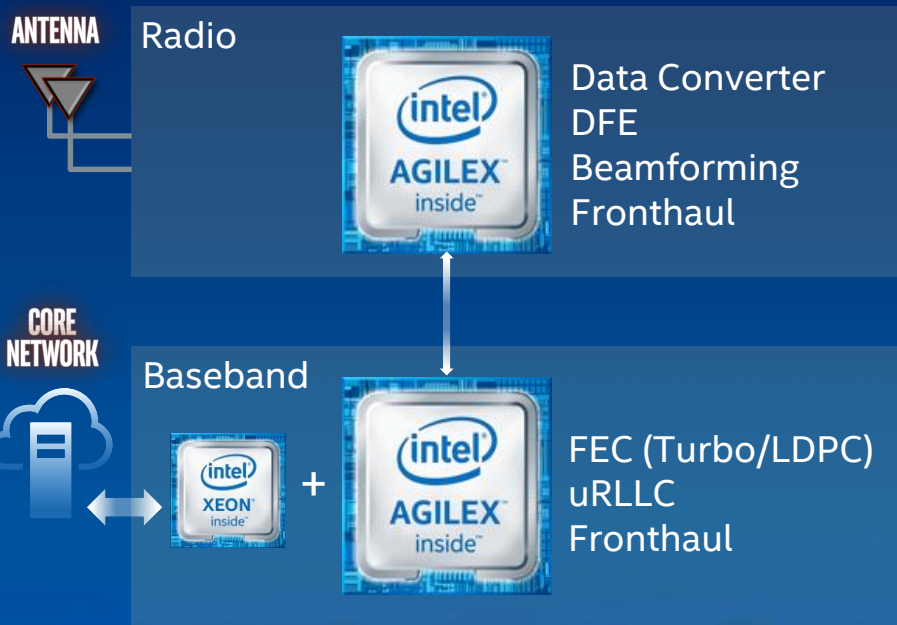
STORAGE ACCELERATION

Compression | Decompression | Encryption
Memory Hierarchy Management

First FPGA with Comprehensive Memory Support and Coherent Attach to Intel® Xeon® Scalable Processors

¹ with FP16 configuration, based on current estimates, see slide 23 for details

Agility & Flexibility for All Stages of 5G Implementation



CUSTOM LOGIC CONTINUUM

FPGA FLEXIBILITY

High Flexibility | Short Time-to-Market

RAPID INTEL® eASIC™ DEVICE OPTIMIZATION

Power & Cost Optimization

FULL CUSTOM ASIC OPTIMIZATION

Best Power¹ | Best Performance¹ | Best Cost¹

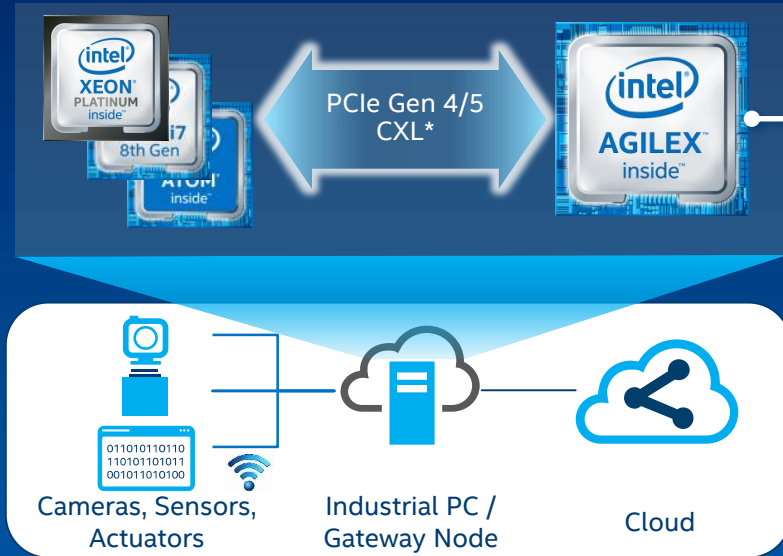
APPLICATION-SPECIFIC TILE OPTIONS

Data Converter | Vector Engine | Custom Compute

Only Intel® Provides All of These Customization Options

¹ Compared to the other customization options shown

Smart, Safe, Secure Factory Acceleration



ACCELERATION AND ANALYTICS

In-Line Protocol Acceleration
Look-Aside Application Acceleration

SAFETY AND SECURITY

Secure Boot | Encryption | Authentication

CUSTOMIZED CONNECTIVITY

Time Sensitive Networks | Flexible IO

**First FPGA Enabling Real-Time Analytics with
Optimized Interfaces to Intel® Processors**

*Compute Express Link

Intel® Agilex™ FPGAs for the Data-Centric World

Intel® Agilex™ FPGAs for transformative applications in edge computing, embedded, networking (5G/NFV) and data centers



Any-to-Any integration enables Intel® FPGAs with application-specific optimization and customization, delivering new levels of flexibility & agility

First FPGAs leveraging Intel's unmatched innovation:
10nm process, 3D integration, Intel® Xeon® Scalable Processor memory coherency (CXL), 112G XCVRs, PCIe* Gen 5, Intel® eASIC™ devices, One API, Intel® Optane™ DC Persistent Memory support

