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The Hidden Cost of Your Isolated System Design

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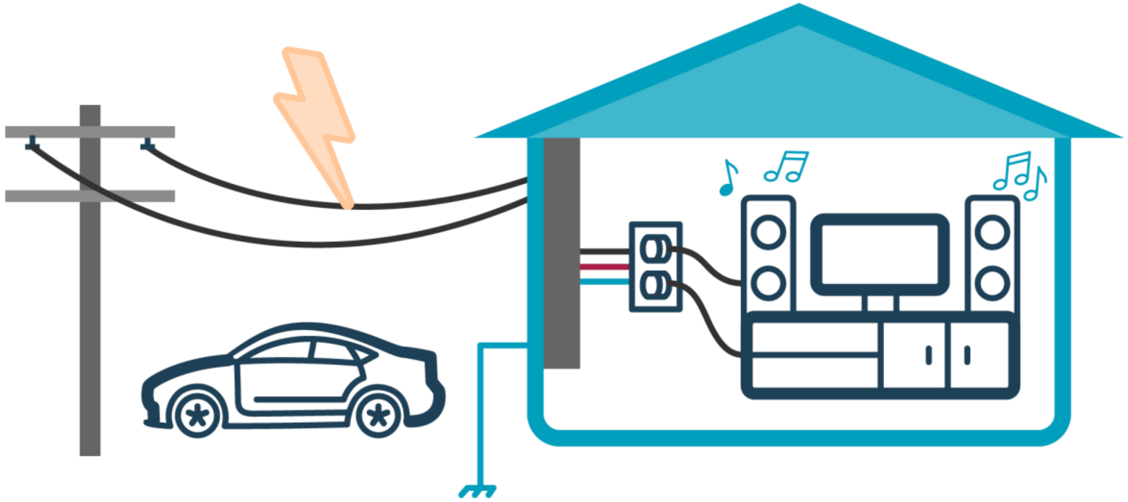
Agenda

- Introduction
- Market Trends Driving Isolated System Design Requirements
- Latest Isolation Trends
- Hidden Costs—How the New Trends Impact Project Risk and Time to Market
- Available Solutions and Shortcomings
- A New Solution for Isolated Power Delivery
- Conclusions

The Need for Isolation

- Electrical isolation is required in many applications
  - Safety—Governed by standards
    - Protect users from shock
    - Protect equipment from shock
  - Performance—No standards compliance
    - Eliminate ground loops
    - Provide fault tolerance
    - Segregate noise

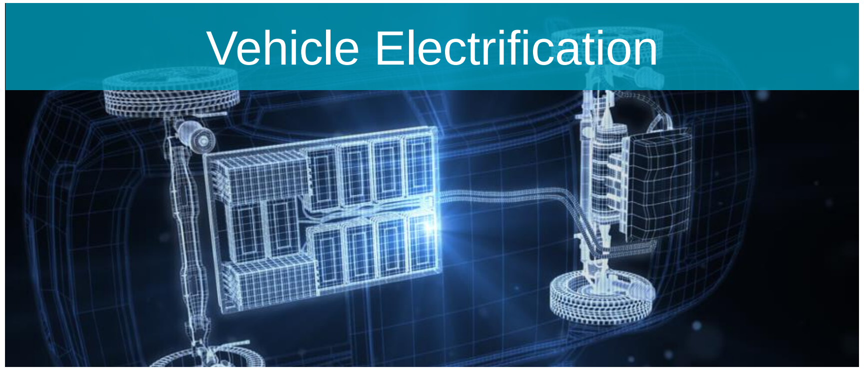


- Circuitry must communicate and/or provide power across an isolation barrier
  - Maintain isolation
    - No current flow (or very little)
  - High performance
    - Voltage ratings, power, timing, reliability

- Hazardous voltages exist at many points within industrial and consumer locations
- People and equipment must be protected from long-term potential differences and temporary overvoltage conditions (faults)
- Local and global regulations mandate safety

Market Trends

- ▶ Smaller and lighter electrical systems
- ▶ Higher voltages—for example, 400 Vdc battery stacks
- ▶ Sensing and connectivity—more sensors and nodes
- ▶ Increased performance and product compatibility


Vehicle Electrification

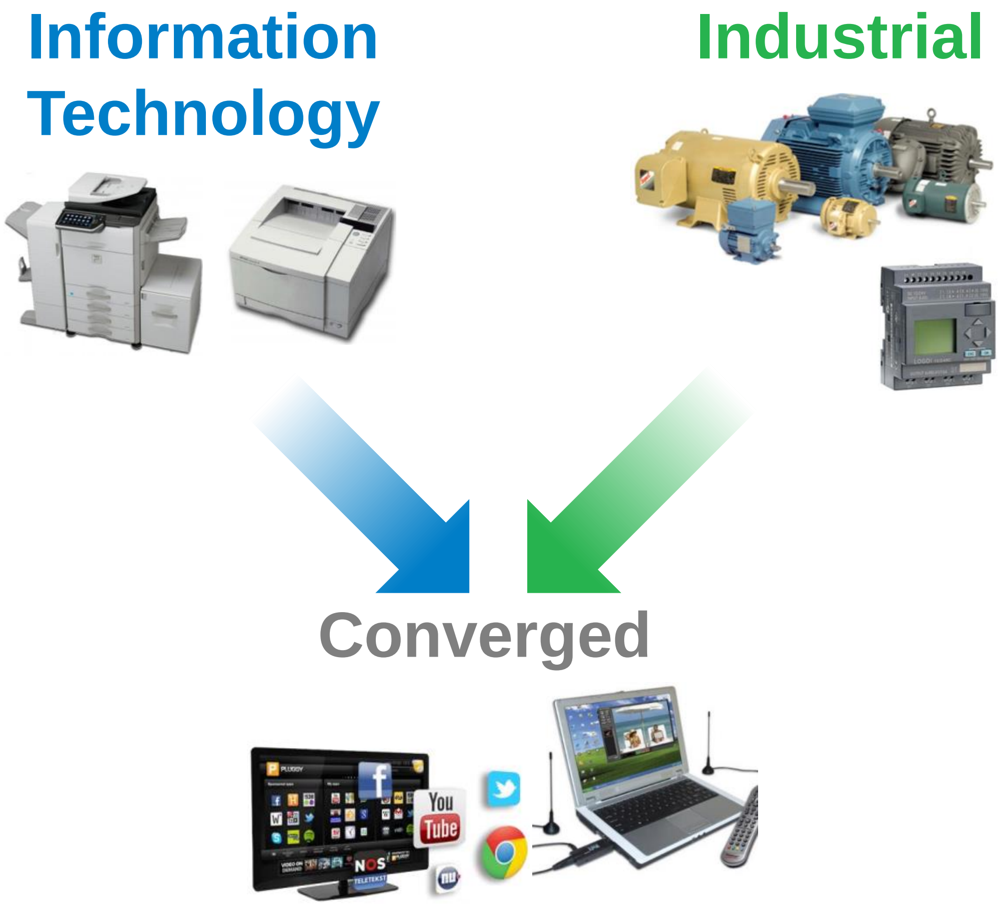
Industry/Industrie 4.0

Convergence of Technology


Consumer IoT

Isolation Trends: EMC (Convergence of Radiated Emissions Specifications)

- Convergence of technology forcing changes in electromagnetic compatibility (EMC) standards
- Standards evolving to combine equipment types—superset of requirements are more difficult to meet
- Example: CISPR32 combines requirements of CISPR22 (information technology) and CISPR11 (industrial, scientific, and medical equipment)
- Example: IEC 60601-1-2 Ed. 4 (medical electronics) considers threats outside traditional controlled healthcare environment
  - EMS, home, aircraft
  - EMC is considered a “normal” event similar to temperature, humidity, and pressure
  - Requirements become more challenging to meet



Isolation Trends: EMC (Convergence of Radiated Emissions Specifications)

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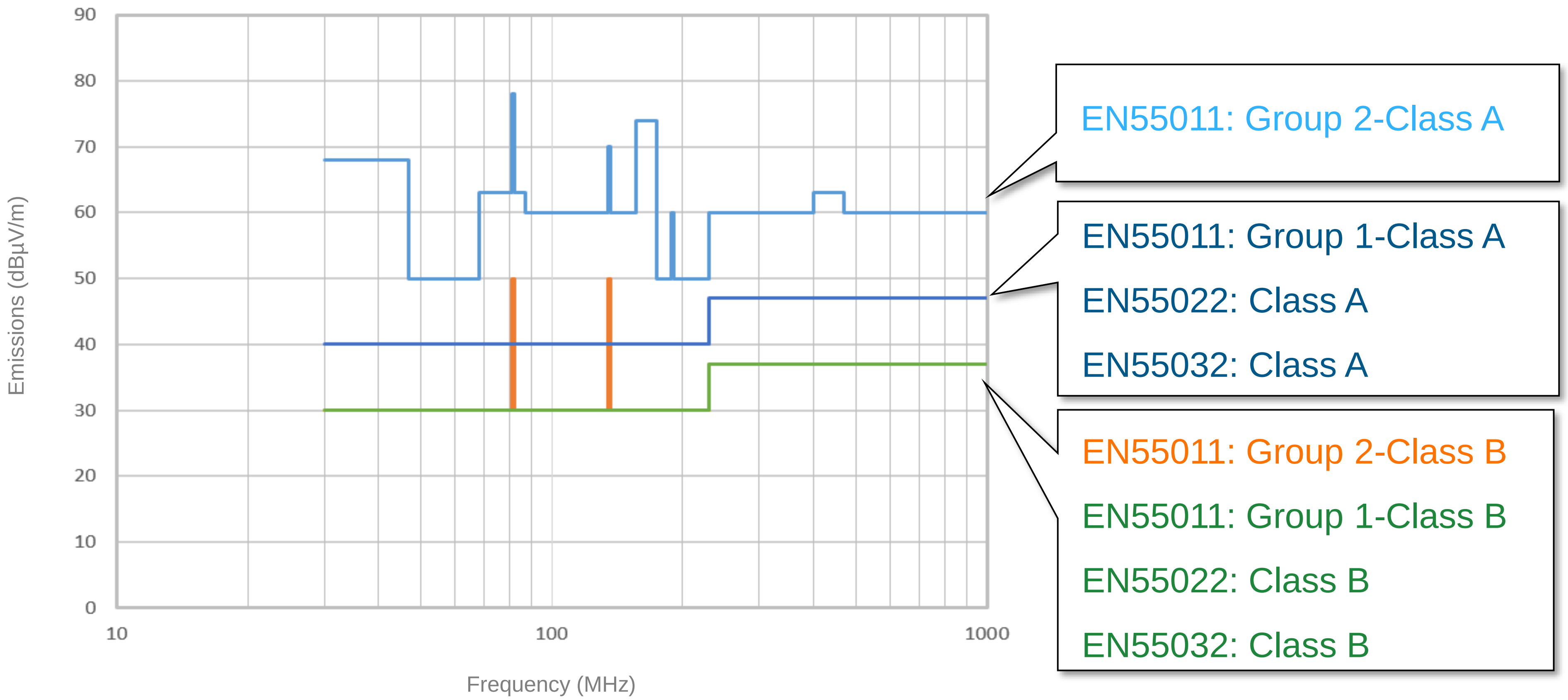

Hidden Cost # 1: Safety Certification

Multiple system-level and component-level safety certifications add additional complexity, even with known or previously certified systems and circuits

- Differing geographic requirements
- Various agencies involved—sometimes with different interpretations of standards

- Standards bodies develop the master standard for a system or component
  - IEC—International Electrical Commission—Worldwide
  - UL—Underwriters Laboratories—North America
  - VDE—in Europe
  - For electrical safety, rules seem to be harmonizing with IEC
- Regional standards bodies
  - Interpret worldwide standards for application to the local region
    - Local line voltage requirements
    - Infrastructure specific modifications (power quality)
    - Environmental differences (altitude in China, humidity in Brazil)
    - Political leverage

Hidden Cost # 2: Increased Density

Forces trade-offs in performance and functionality, may impact schedule due to limited availability of solutions

- Increased density in factory automation
- Electronics must shrink
  - More integration
  - Smaller packaging
  - Smaller PCBs, higher density
- Similar trend in instrumentation
  - More functionality
  - Smaller packaging/housings

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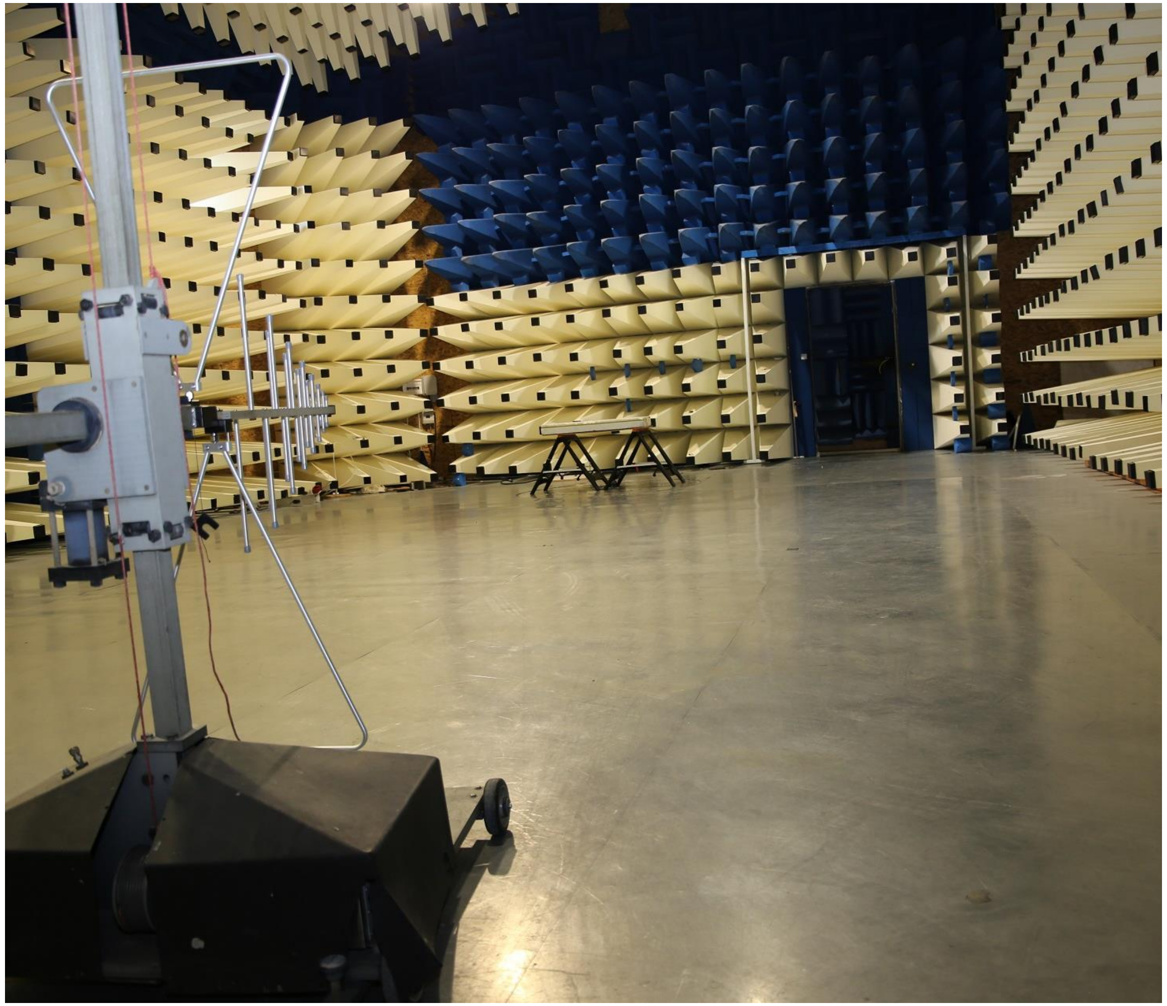
Hidden Cost # 3: Reducing Radiated Emissions

EMI mitigation techniques add to component count, extend the design, and may require multiple board spins to meet targets

- Classic EMC mitigation techniques
  - Ferrites
  - Capacitors (decoupling and cross-barrier)
  - Beads
  - Metal shields/enclosures
- Smaller and more dense PCBs
  - Less space for mitigation
- Mitigation is often implemented by trial and error
  - Tests are lengthy and expensive



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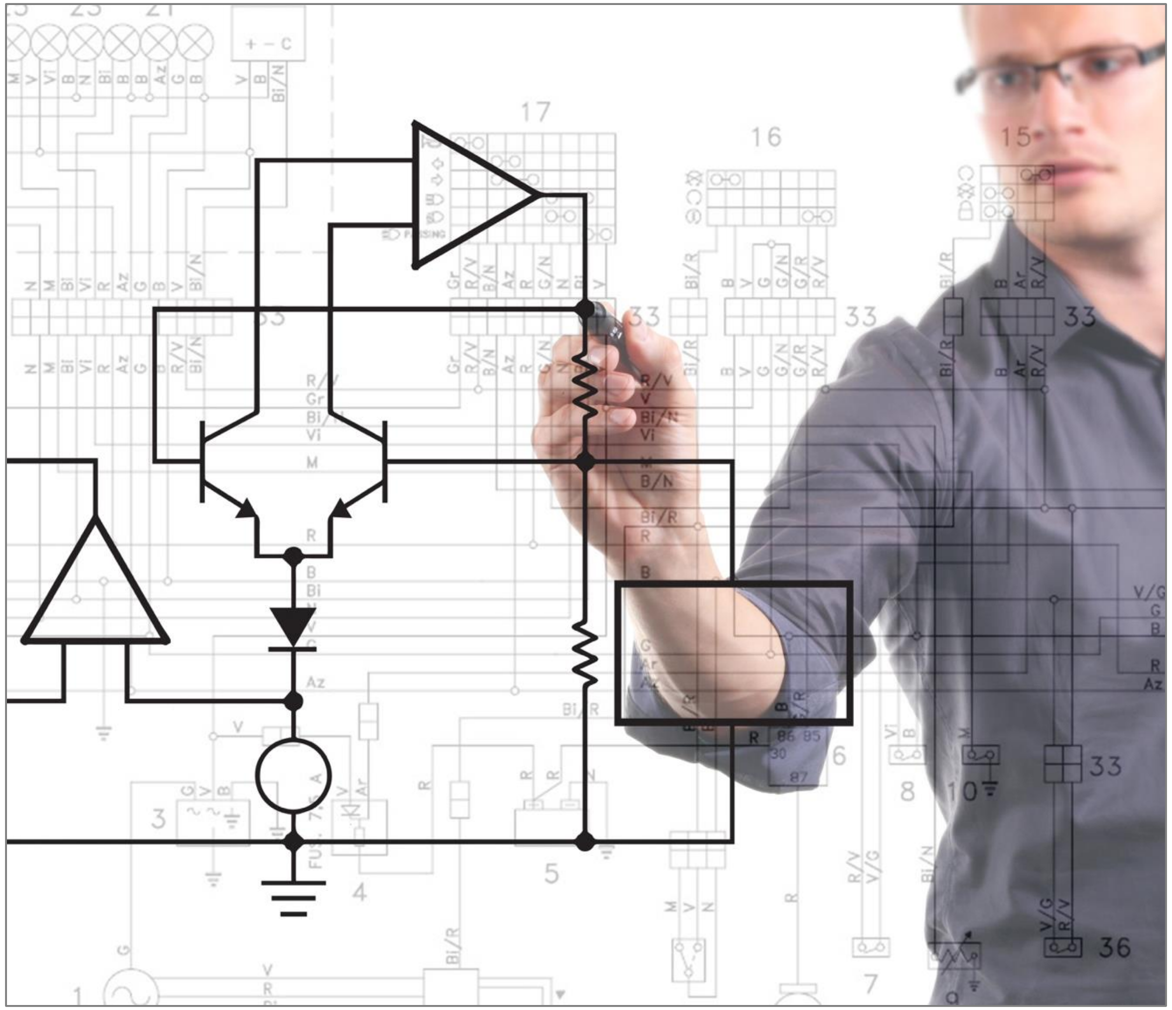
Hidden Cost # 4: Isolation Complexity

May require specialized expertise and add to project cost and time

- Transferring power and data across the isolation barrier
- Using multiple power sources



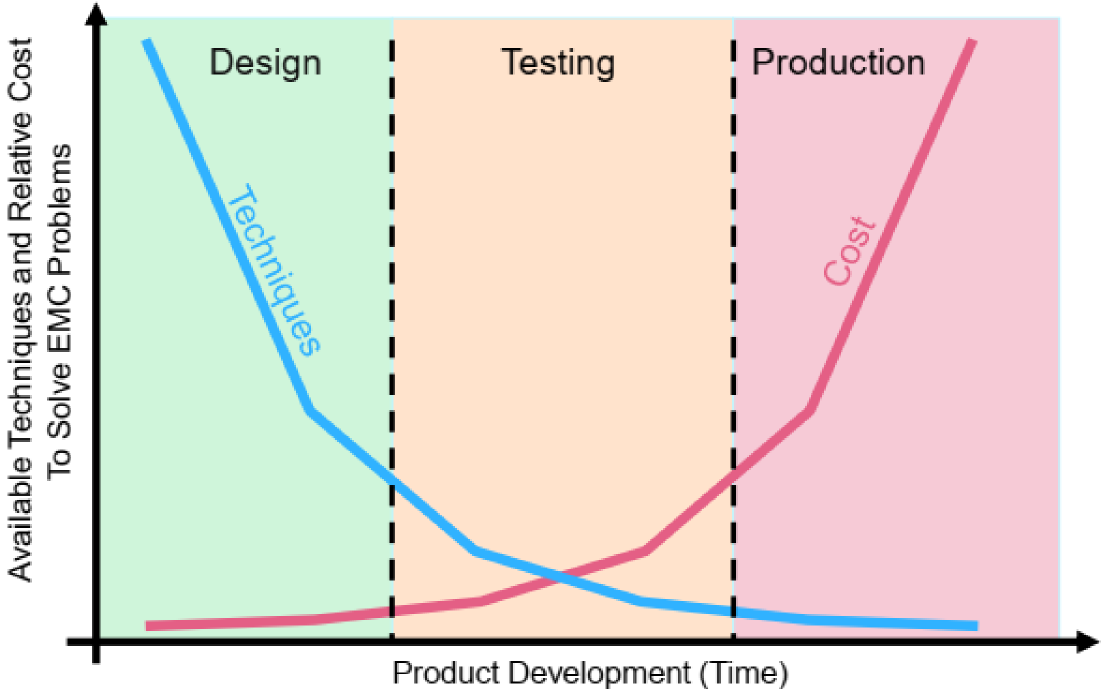
The Need for a New Solution: Managing Project Cost and Risk

Typical Isolation Design Trade-offs

- Keeping your application small **vs.**
- Meeting EMC targets **vs.**
- Meeting deadlines with fewer board spins **…**

Need a solution that will help speed time to market, reduce evaluation time, mitigate risk, and decrease project cost

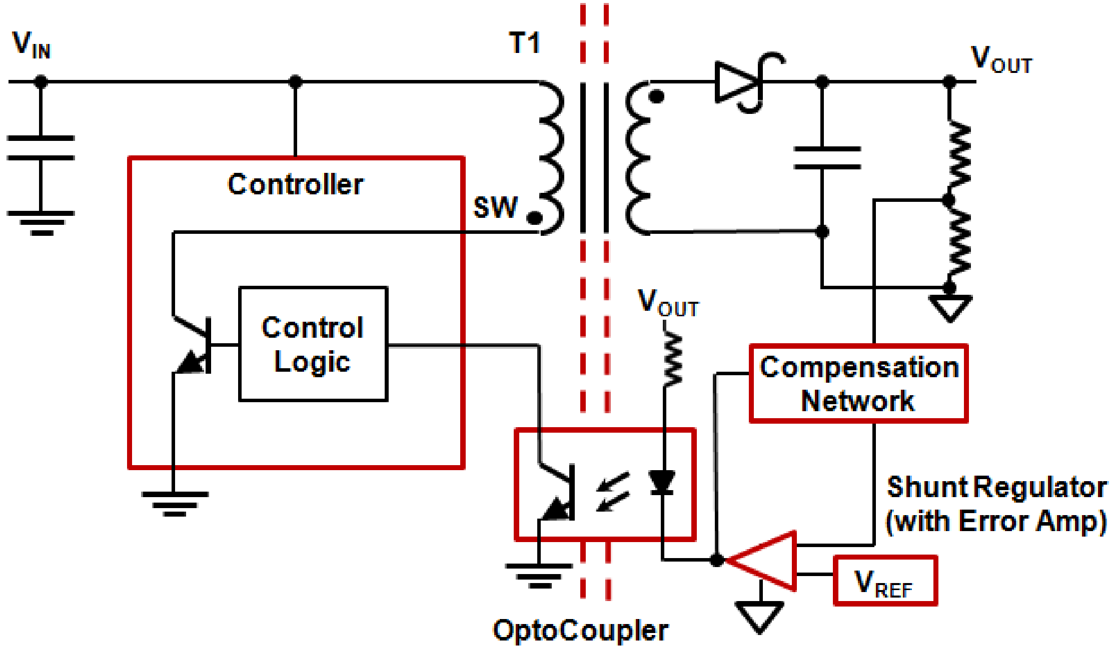
- More integrated components
- Pretested and precertified functions
- EMC mitigation techniques enacted earlier in the project
- Simplified design



Source: Electromagnetic Compatibility Engineering 1st Edition by Henry W. Ott

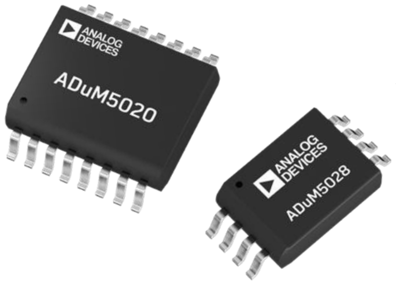
Traditional Isolated Power Solution: Discrete Implementation

- Isolated Flyback converters are a common approach for isolated power needs
- They have some benefits, including a low bill of material cost, but there are drawbacks
- The error amplifier requires engineering effort to develop a compensation network to stabilize the voltage loop
  - Dependent on optocoupler performance variability
  - Variation in current transfer ratio limits performance and the operating temperature range
- This approach seems better from a cost point of view, but there's a trade-off in engineering effort and technical risk
- This also introduces risk in EMC performance and the ability to achieve safety certifications



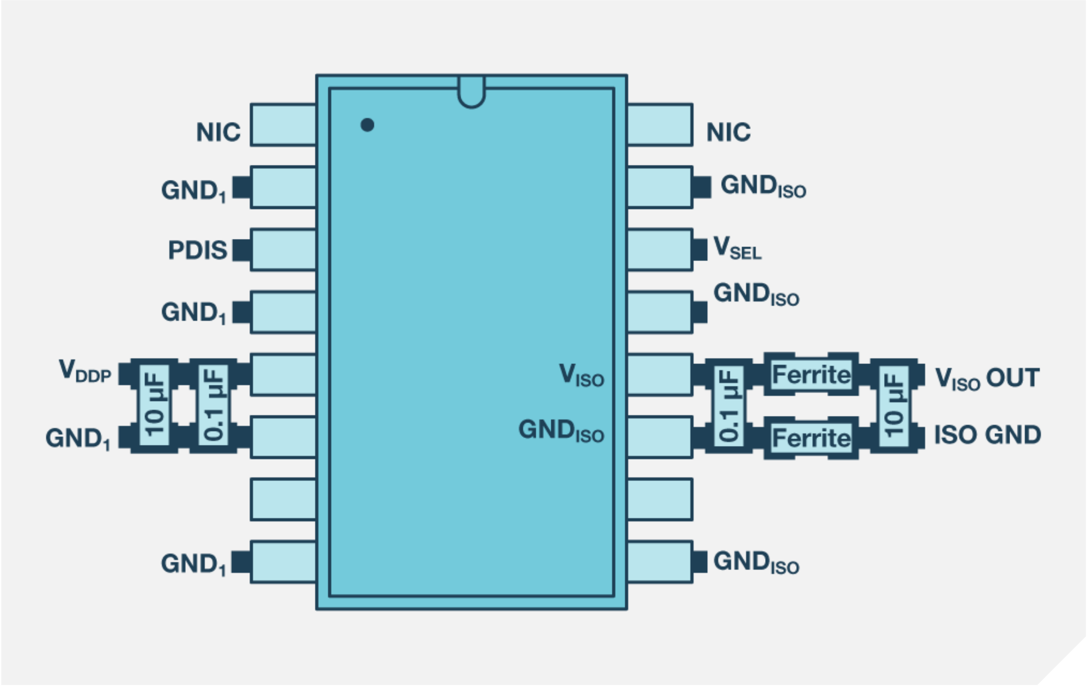
A New Solution

Low Emissions *iso*Power® Integrated, Isolated DC-to-DC Converters

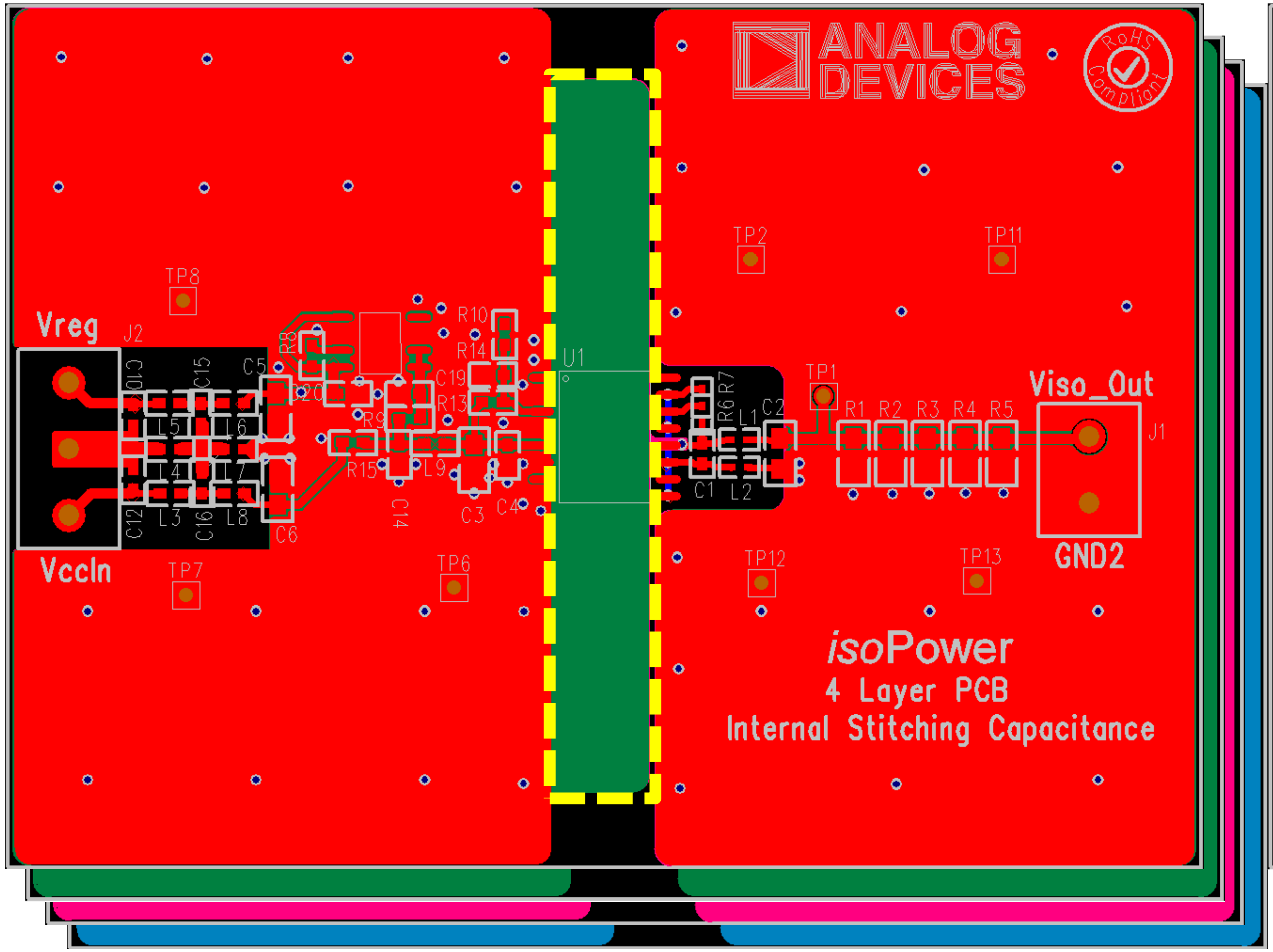


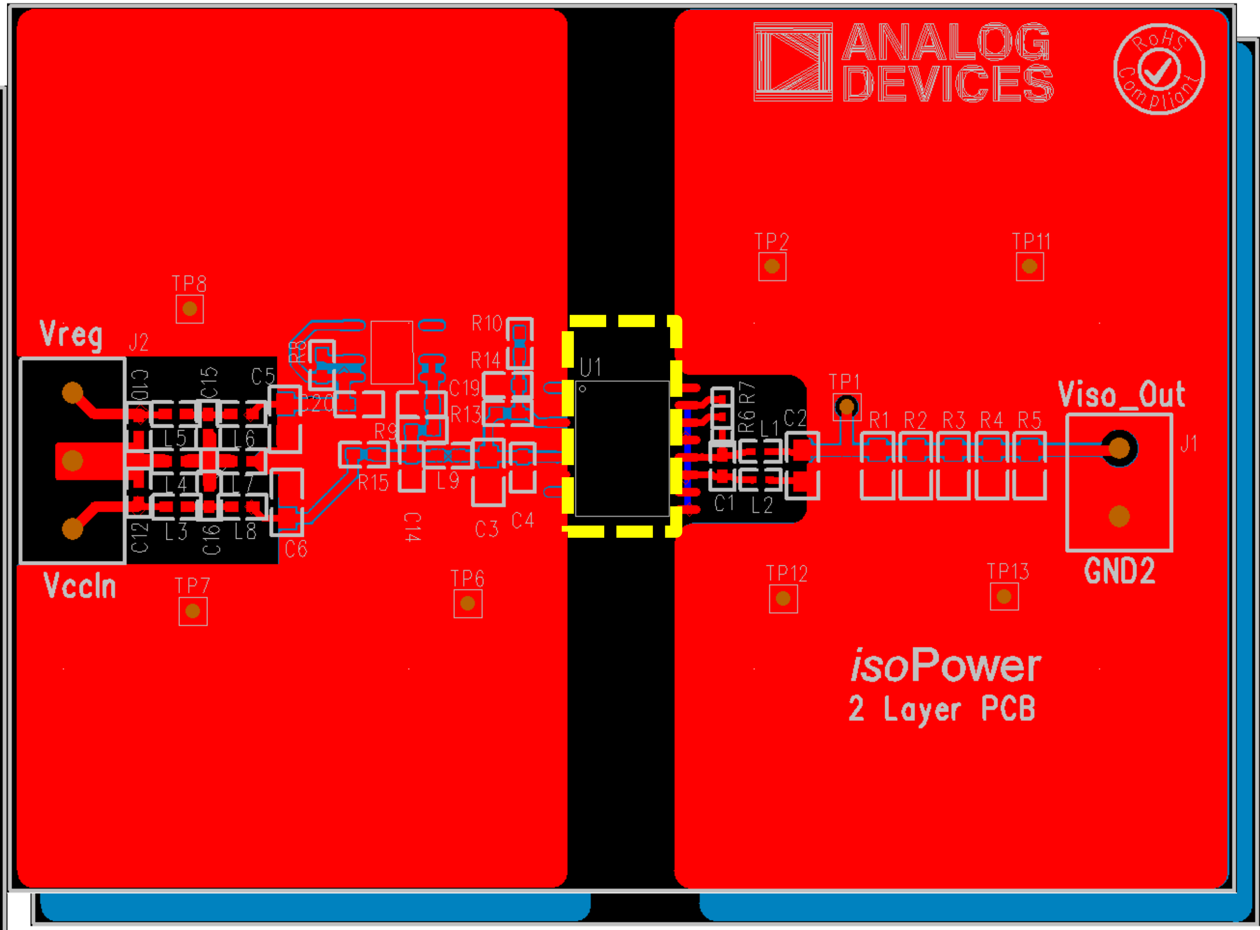
The ADuM5020/ADuM5028 and ADuM6020/ADuM6028 build upon ADI's pioneering expertise in digital isolated power solutions

- Simplified EMC certification
  - Below EN 55022/CISPR 22 Class B emissions limits at full load on a 2 layer PCB
- Smallest package size
  - 8-lead SOIC_IC package with 8.3 mm minimum creepage and 300 mW isolated output power
- 500 mW integrated isolated output power
  - ADuM5020 16-lead SOIC_W package with 7.8 mm creepage
  - ADuM6020 16-lead SOIC_IC package with 8.3 mm creepage
- Safety Certifications



The Advantage: Simple and Small 2-Layer PCB





More than 70% PCB area savings

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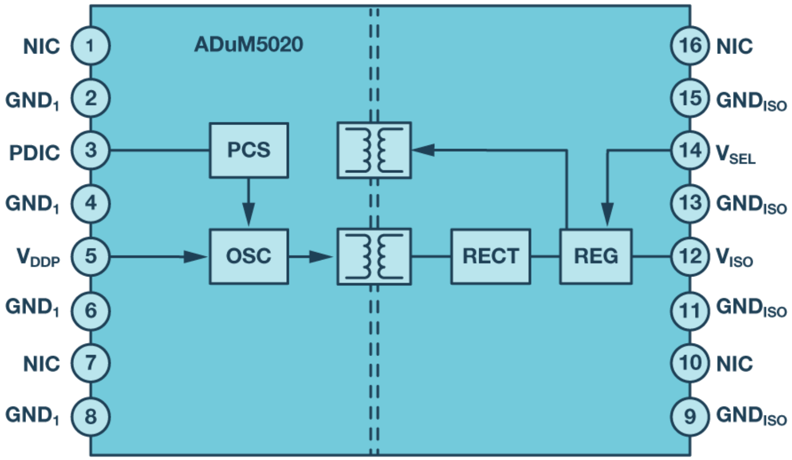
Measuring Radiated Emissions with *iso*Power®

ADuM5020

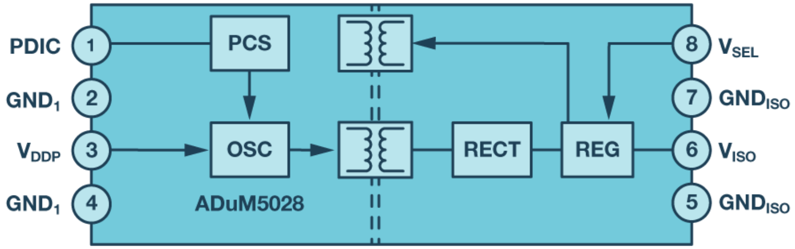


16-lead SOIC_W 100 mA max load

CISPR 22/EN 55022 Class B tests

10 m chamber at CEI, Ireland

ADuM5028



8-lead SOIC_IC 60 mA max load

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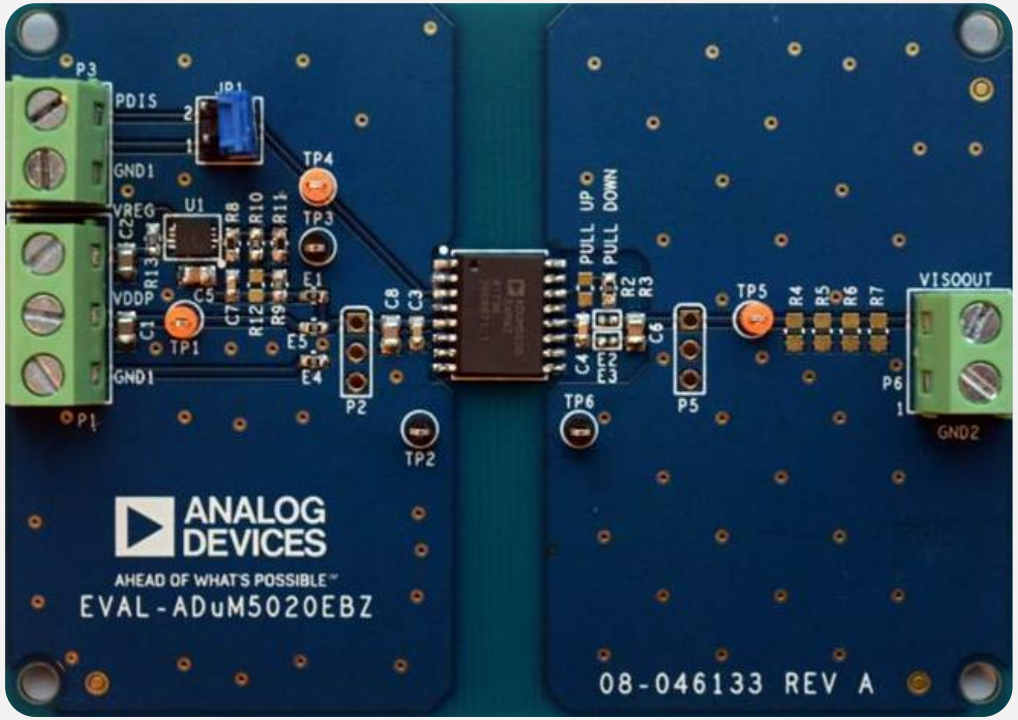
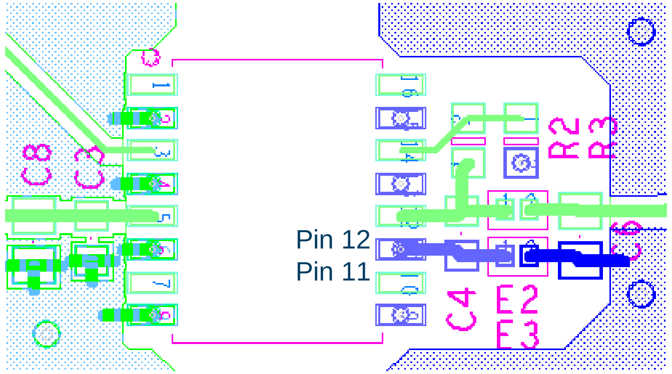
Simplified 2 Layer PC Board Layout

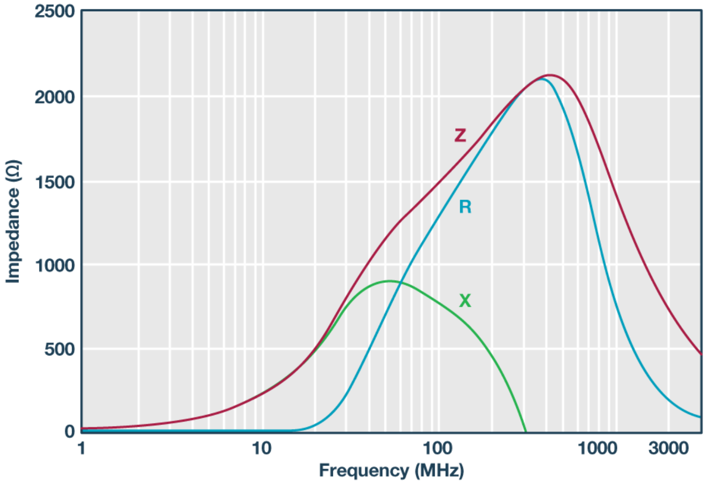
ADuM5020 and **ADuM5028** evaluation boards with 2 layer PCB, meet CISPR 22 Class B using ferrites on V_{ISO} and GND_{ISO}, but without stitching capacitance





Example of ADuM5020 16-lead SOIC Zoomed In on Pin 11 GND_{ISO} and Pin 12 V_{ISO}

Ferrites E2, E3 and Bypass Capacitors C4, C6



Ferrites E2, E3

Murata BLM15HD182SN1

Impedance of 1800 Ω at 100 MHz to 1000 MHz

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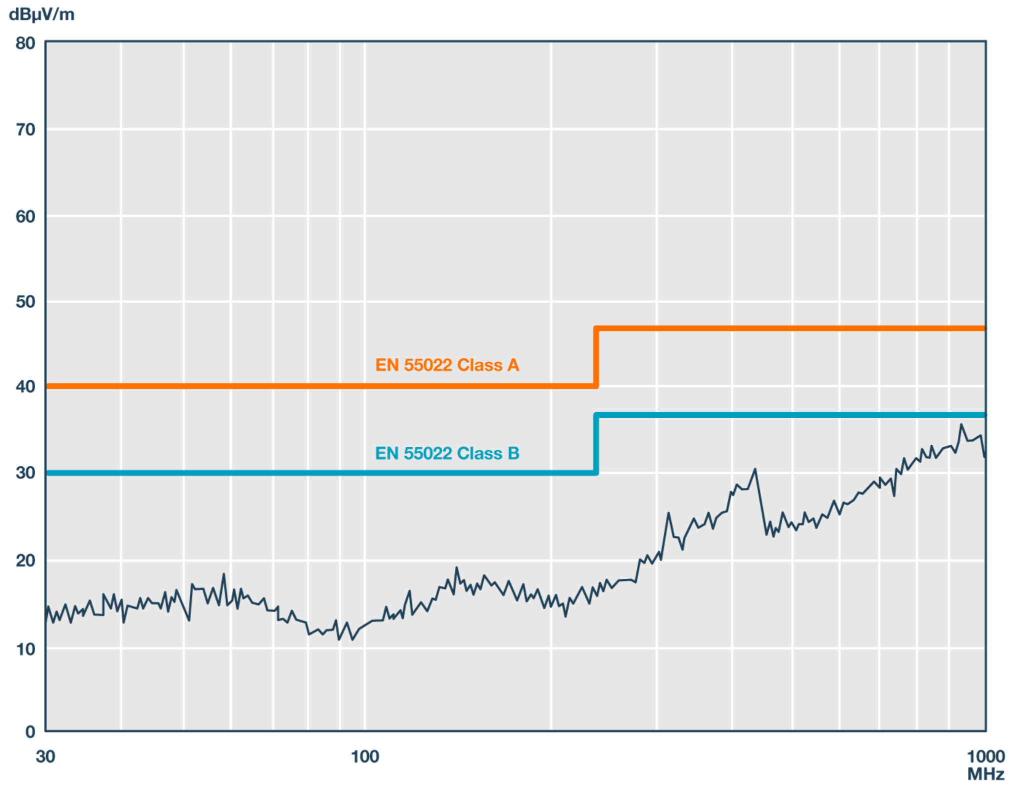
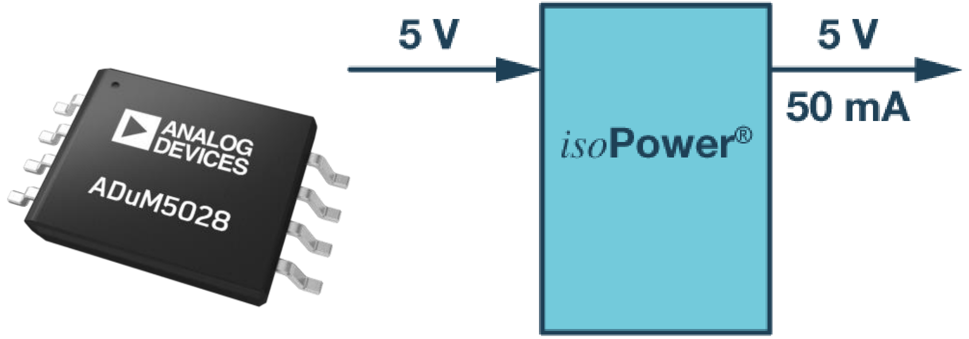
ADuM5028: Meeting CISPR 22 Class B

ADuM5028 with 50 mA Load





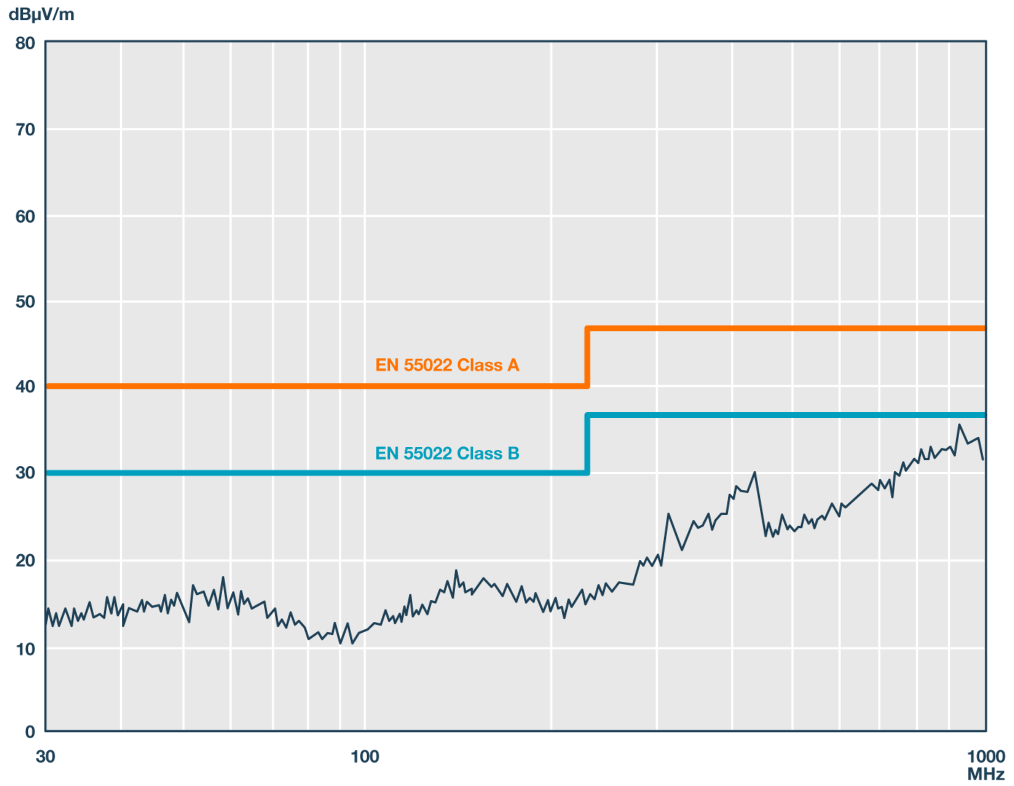
30 MHz to 1000 MHz Results

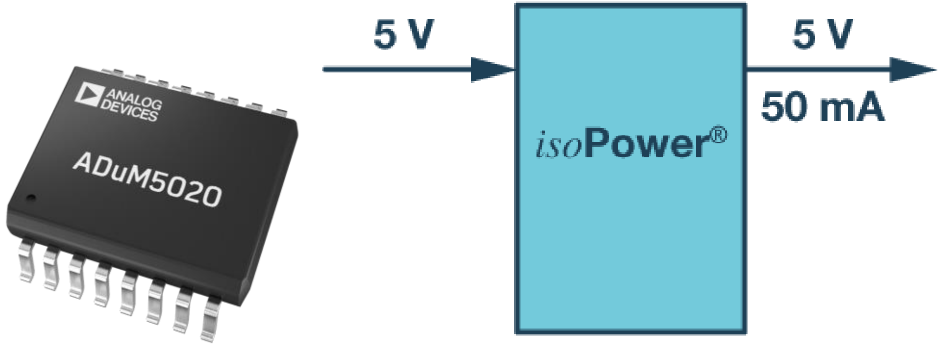
Frequency (MHz)	Angle (°)	Height (m)	Quasi-Peak Measurement (dBμV/m)	Class B Limit (dBμV/m)	Quasi-Peak Margin from Class B Spec (dB)
308.9	180	3.5	25.3	37	–11.7
396.956	0	2	27.7	37	–9.3
428.668	0	2	27	37	–10
920.04	0	1	30.7	37	–6.3

Using 2 Layer PCB: Quasi-peak meets CISPR 22 Class B by –6.3 dBμV margin @ 920 MHz

ADuM5020: Meeting CISPR 22 Class B

ADuM5020 with 50 mA Load





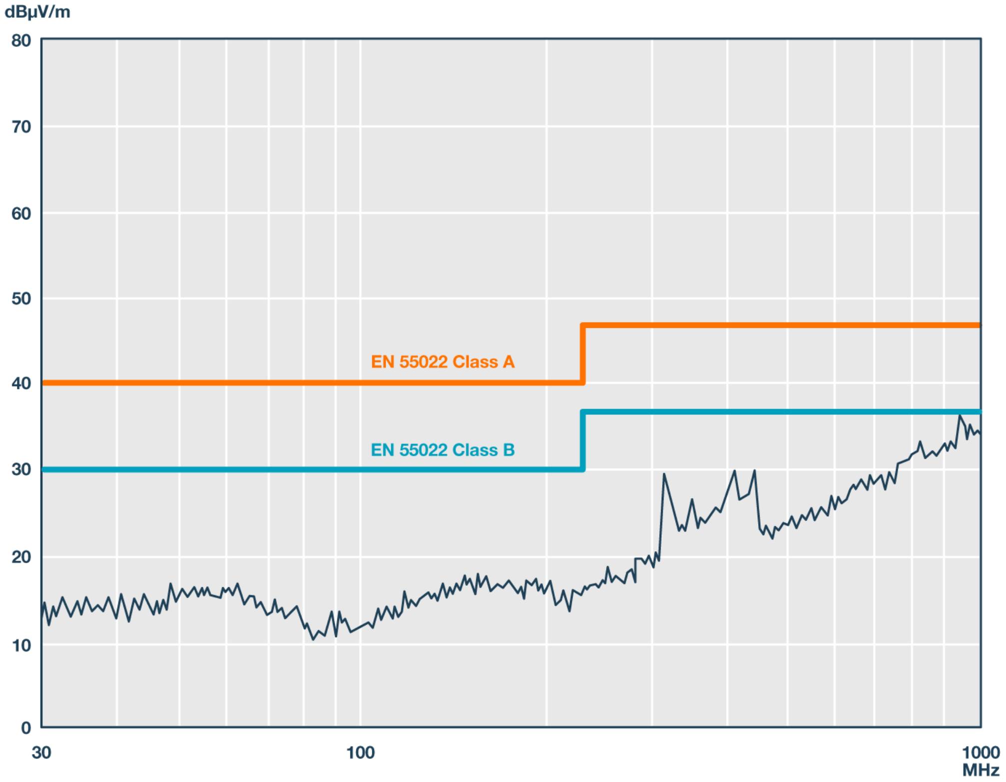
30 MHz to 1000 MHz Results

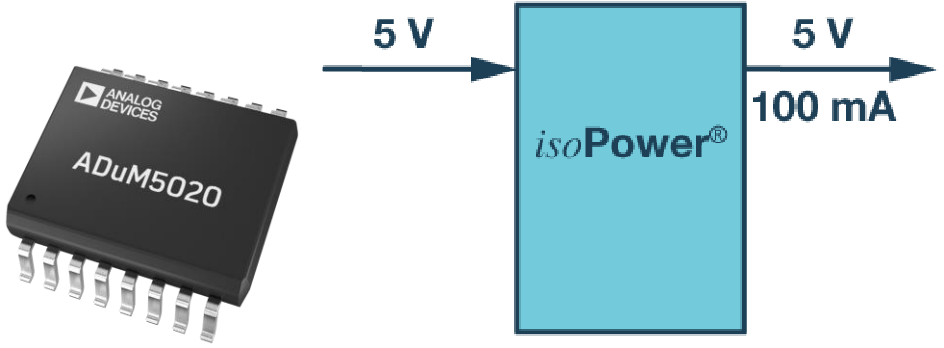
Frequency (MHz)	Angle (°)	Height (m)	Quasi-Peak Measurement (dBµV/m)	Class B Limit (dBµV/m)	Quasi-Peak Margin from Class B Spec (dB)
310.2	180	3	24.1	37	–12.9
426.256	0	3	26.7	37	–10.3
359.004	180	1	23.7	37	–13.3
935.76	0	1	30.1	37	–6.9

Using 2 Layer PCB: Quasi-peak meets CISPR 22 Class B by –6.9 dBµV margin @ 935 MHz

ADuM5020: Meeting CISPR 22 Class B with 100 mA Load

ADuM5020 with 100 mA Load





30 MHz to 1000 MHz Results

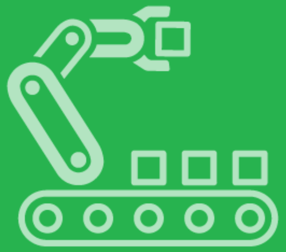
Frequency (MHz)	Angle (°)	Height (m)	Quasi-Peak Measurement (dBµV/m)	Class B Limit (dBµV/m)	Quasi-Peak Margin from Class B Spec (dB)
305.656	180	3	28.3	37	–8.7
336.892	180	2.5	27.3	37	–9.7
396.532	180	2	28.5	37	–8.5
426.456	180	2	25.3	37	–11.7
915.264	0	1	31.9	37	–5.1

Using 2 Layer PCB at 100mA : Quasi-peak meets CISPR 22 Class B by –5.1 dBµV margin @ 915 MHz

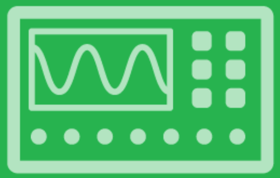
Compact, High Density, High Voltage Emerging Applications

- **Regulatory Compliance**
  Meet CISPR 22 Class B standards

Battery Monitoring and Inverters



Programmable Logic Controller (PLC)



Precision Measurement

Vital Signs Monitoring

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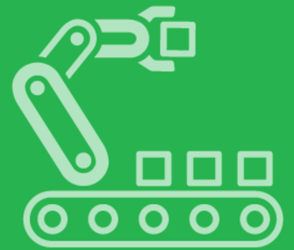
Compact, High Density, High Voltage Emerging Applications

- **Reduced Complexity**
  No stitching capacitance needed

Battery Monitoring and Inverters



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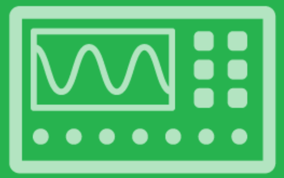

Precision Measurement

Vital Signs Monitoring

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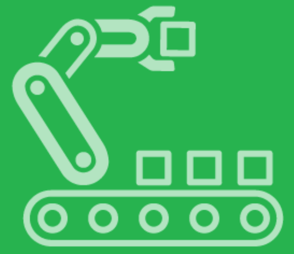
Compact, High Density, High Voltage Emerging Applications

- **Lower Material Cost**
  Up to 30% on a
  2-layer PCB

Battery Monitoring and Inverters



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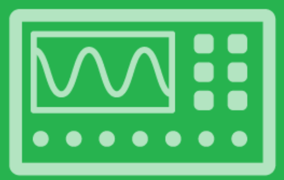


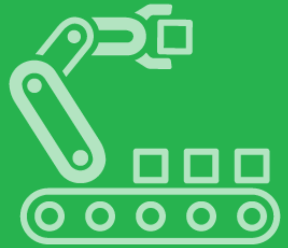
Precision Measurement

Vital Signs Monitoring

Compact, High Density, High Voltage Emerging Applications

- **Smaller Application Size**
  Up to 70% PCB space savings

Battery Monitoring and Inverters



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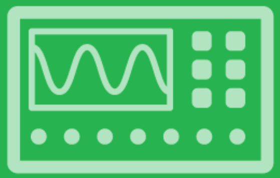


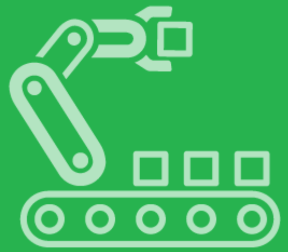
Precision Measurement

Vital Signs Monitoring

Compact, High Density, High Voltage Emerging Applications

- **Faster Time to Market**
  Reduced PCB design and test time

Battery Monitoring and Inverters



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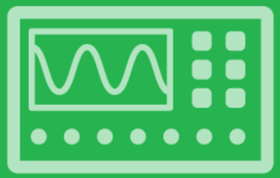

Precision Measurement

Vital Signs Monitoring

Conclusions

- Market trends such as vehicle electrification and Industry 4.0 are creating increased electrical content in many applications
  - This is driving an upsurge in the need for high performance, high density isolated circuitry
- Technical trends are making isolated system design more difficult and risky
- EMC specifications are becoming more difficult, while equipment types are converging
- Global system-level and component-level safety certification requirements add another layer of complexity and risk
- Fully integrated and safety-certified isolated dc-to-dc converters with documented EMC performance offer systems designers a better solution
- They can dramatically reduce design complexity and ensure better EMC testing and compliance
- With less time devoted to redesign, recharacterization, and retesting, designers can reduce board space, lessen risk, lower costs, and improve time to market

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