

 **ADI** *iCoupler*<sup>®</sup>

Got EMI! Fix it with  
the latest *isoPower*



# Presenter



## **James Scanlon**

EMC Applications Engineering  
Interface and Isolation Products

# Agenda

- ▶ The Problem with EMI
- ▶ Isolation landscape — integrated power and data
- ▶ The EMI challenge and current methods to solve it
- ▶ The need for a new approach
- ▶ Next-generation *isoPower*® and isolated data technology overview
- ▶ What is EMI testing
- ▶ EMI results for *isoPower*® and isolated data
- ▶ Expected Benefits and Next Steps
- ▶ Q&A

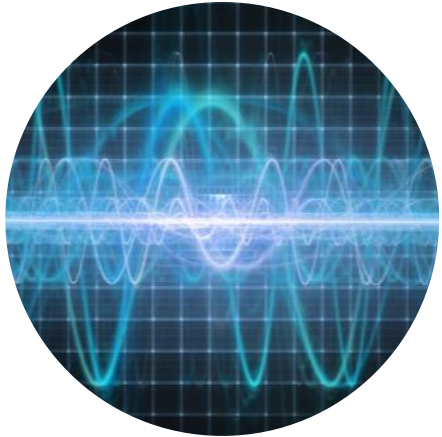
# Market Trends: Smaller and Lighter Electronic Systems

Forces trade-offs in performance and functionality, may impact schedule due to limited availability of solutions

- ▶ Increased density in factory automation, instrumentation and medical
- ▶ Electronics must shrink
  - More functionality
  - More integration
  - Smaller packaging
  - Smaller PCBs, higher density



# The Problem with EMI







- ▶ EMI issues
  - Regulatory compliance
  - RF spectrum pollution
  - Compatibility within circuits
  - System disturbance or malfunction
  - Damage and liability



- ▶ Designing for compliance can have a steep learning curve
  - Components
  - PCB (printed circuit board) layout
  - Signal integrity
  - Cables
  - Enclosure and shielding
  - Software and firmware

**~50%** of designs fail EMI tests the first time

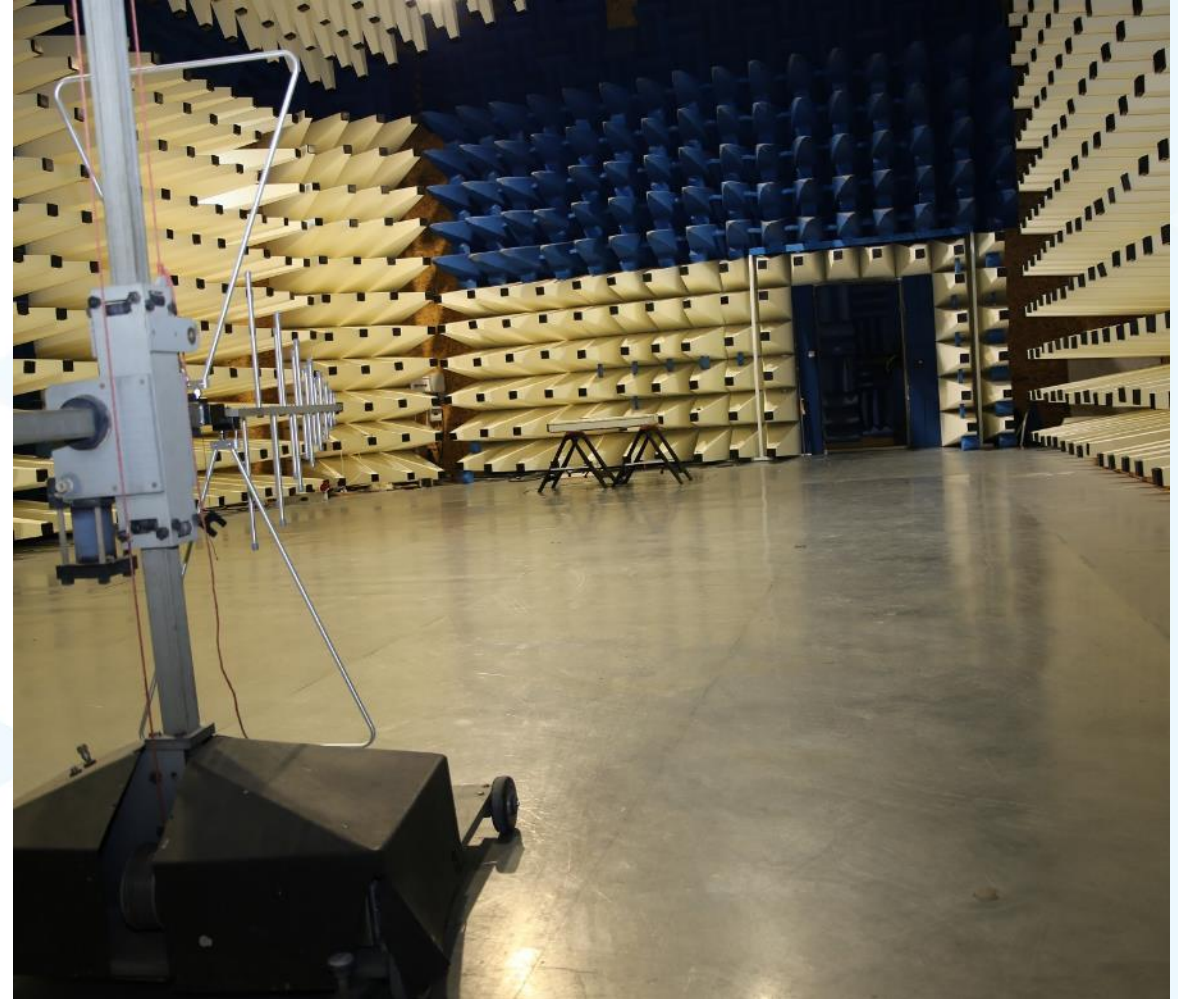
Source: Intertek

	USA	EU+
Emissions Increase ↑	<b>Class A</b>  Nonresidential	 Industrial
	<b>Class B</b>  Residential	 Residential, Commercial, Light Industrial

# A Hidden Cost: EMI

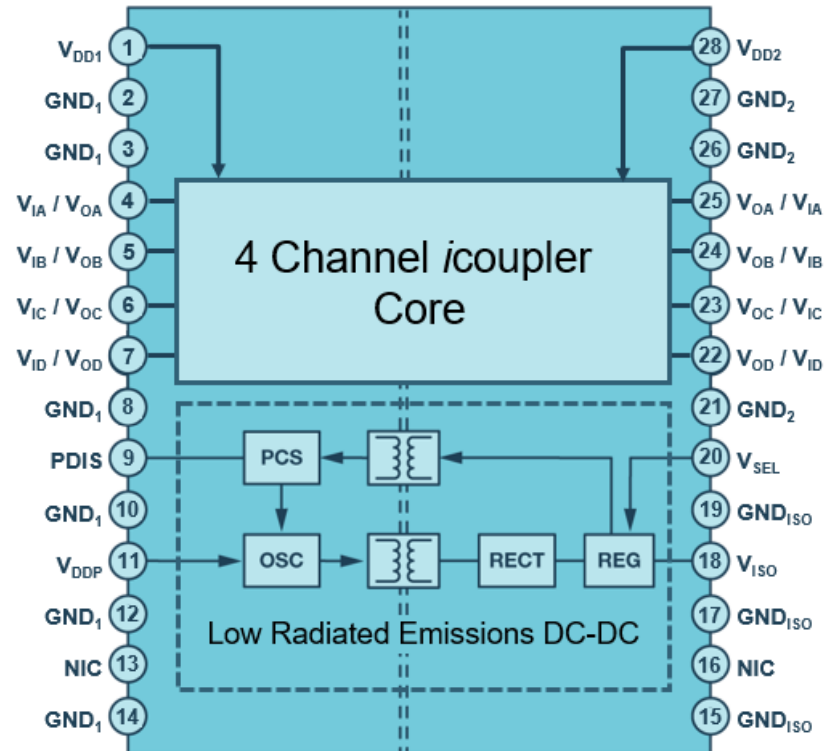
EMI mitigation techniques add to component count, extend the design, and may require multiple board spins to meet targets

- ▶ Classic EMC mitigation techniques
  - Clamp Ferrites
  - Capacitors (decoupling and cross-barrier)
  - Ferrite Beads
  - Metal shields/enclosures
- ▶ Smaller and more dense PCBs
  - Less space for mitigation
- ▶ Mitigation is often implemented by trial and error
  - Tests are lengthy and expensive
  - Reduces Time to Revenue



# Isolation Landscape: *isoPower*<sup>®</sup> with Isolated Data

## Small, Simplified Design for Reduced Component Count



Small 28-Lead Fine Pitch  
Wide-Body SOIC

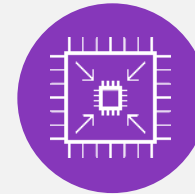
Analog Devices—  
first to market

#1

## Advantages



**Optimized solutions**—no need to design a power supply



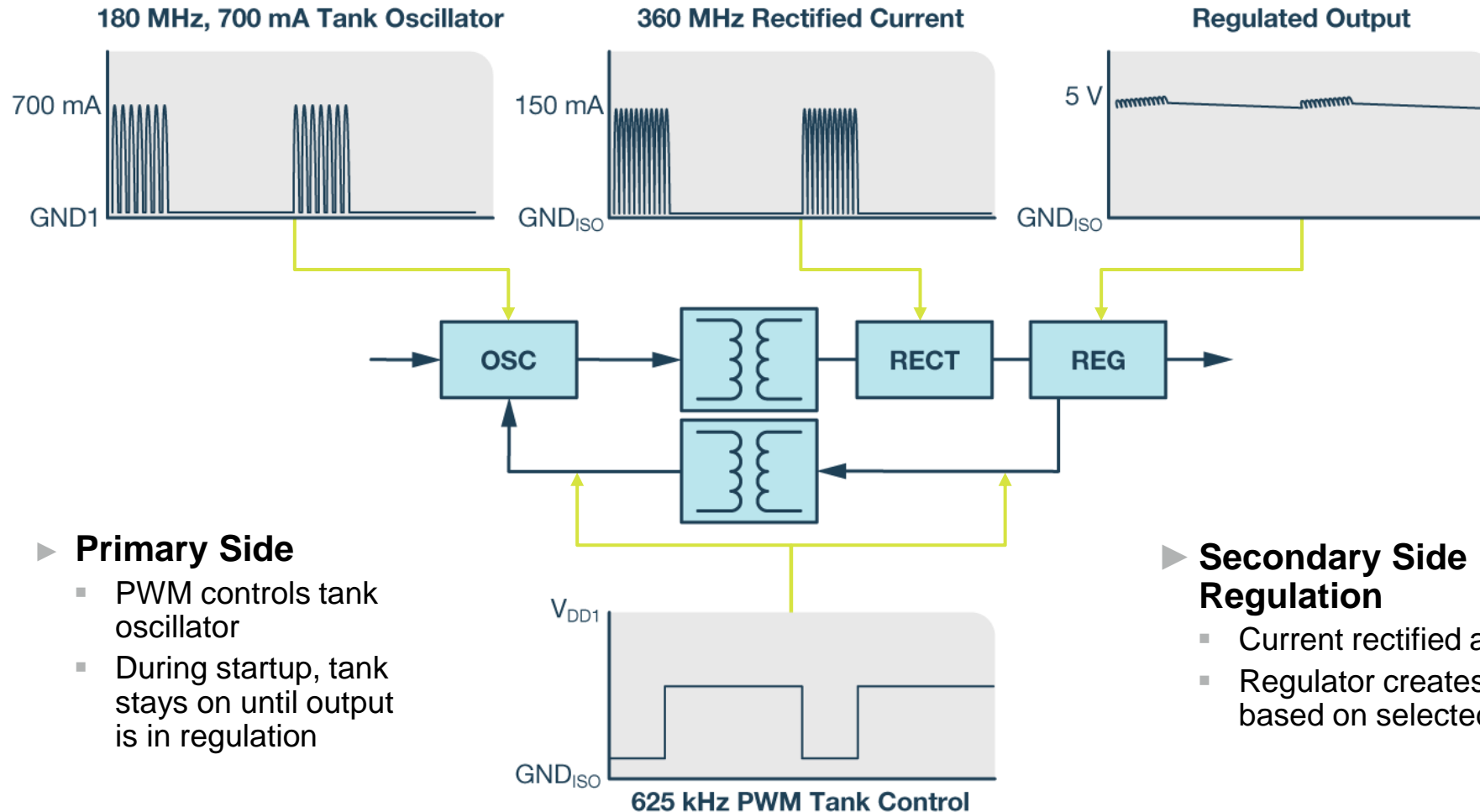
**Reduced size**—with small component count



**Innovation**—space constrained applications can pack more isolated supplies in a small system

# Isolated Power Technology: How It Works

## High frequency operation for small size of transformer coils



### ► Primary Side

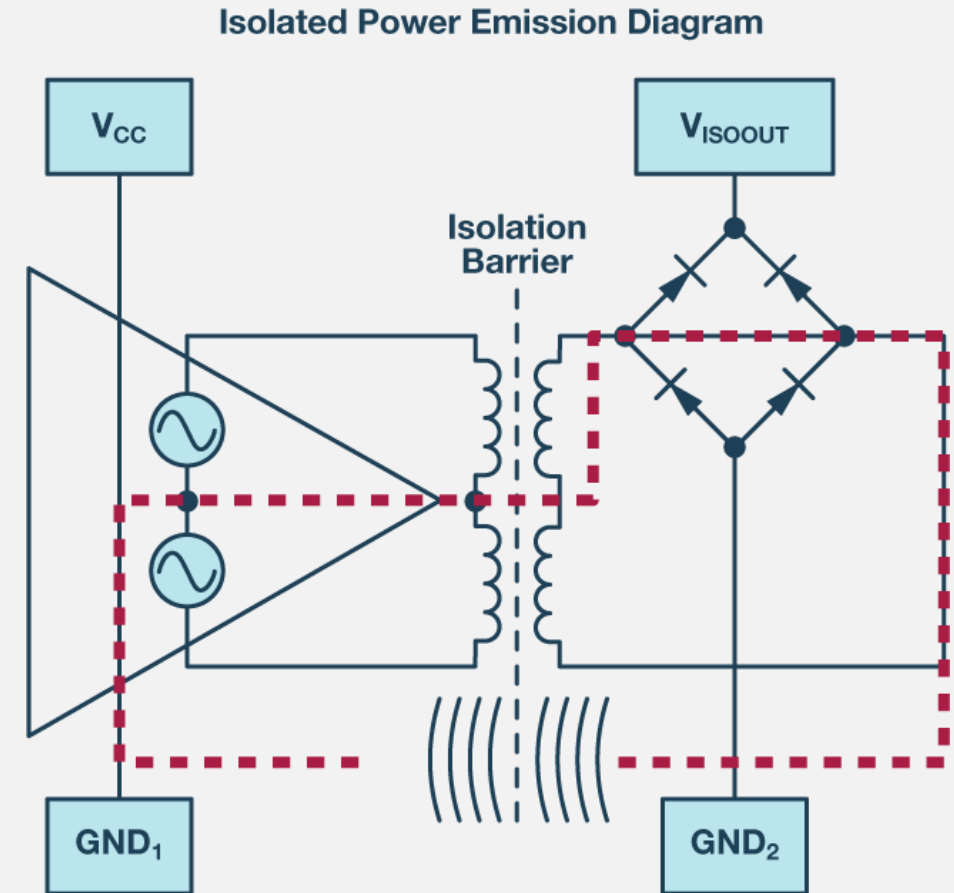
- PWM controls tank oscillator
- During startup, tank stays on until output is in regulation

### ► Secondary Side Regulation

- Current rectified and filtered
- Regulator creates PWM based on selected set point

# The Challenge: Increased Radiated Emissions


- ▶ Using 50 MHz to 200 MHz frequencies to obtain small transformer size comes with increased radiated emissions
  - **Common-Mode Current:** Parasitic currents are coupled through the transformer to the secondary side
  - **No Return Path:** No physical path across the isolation barrier for these currents to return creates a dipole antenna that can radiate
  - **Loop Area:**  $V_{ISO\ OUT}$  and  $GND_2$  pins connected to planes increase the loop area and the emissions
  - **Stitch Capacitance:** To reduce the dipole emissions, a low impedance return path for the high frequency common-mode currents is needed



# Current Solutions: Mitigate EMI at the Board Level

Tackling emissions at the **board/applications level**, various methods can be effective, but may be difficult or costly to implement

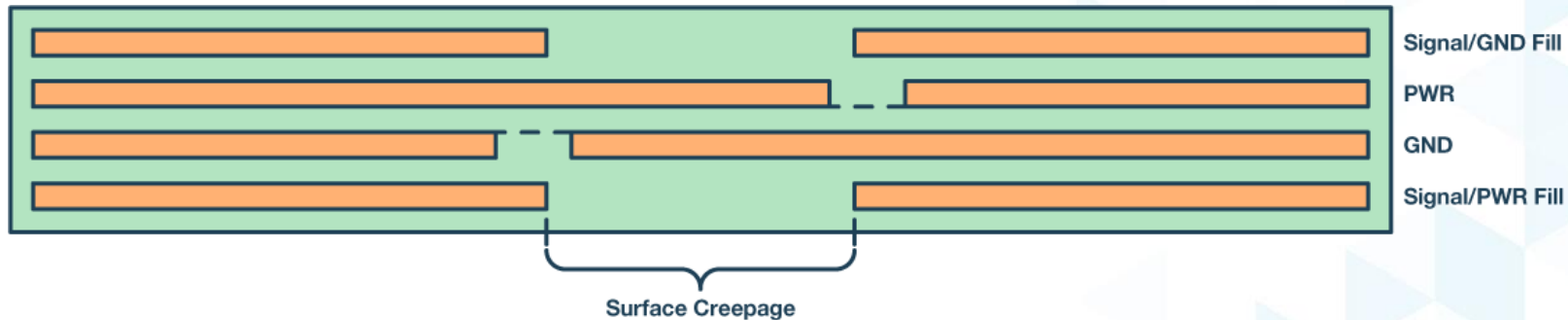
 **Solution**  
Stitching Capacitance

 **Disadvantages**  
Multiple layers, more cost  
Difficult to lay out  
Increased design/test time  
Adds unwanted leakage current

Discrete Stitching Capacitor

Large and expensive

## Overlap Stitching Capacitor for Multilayer PCB 2 Layers of Power plus 2 Layers of Signal



## High Voltage Discrete Stitching Capacitor

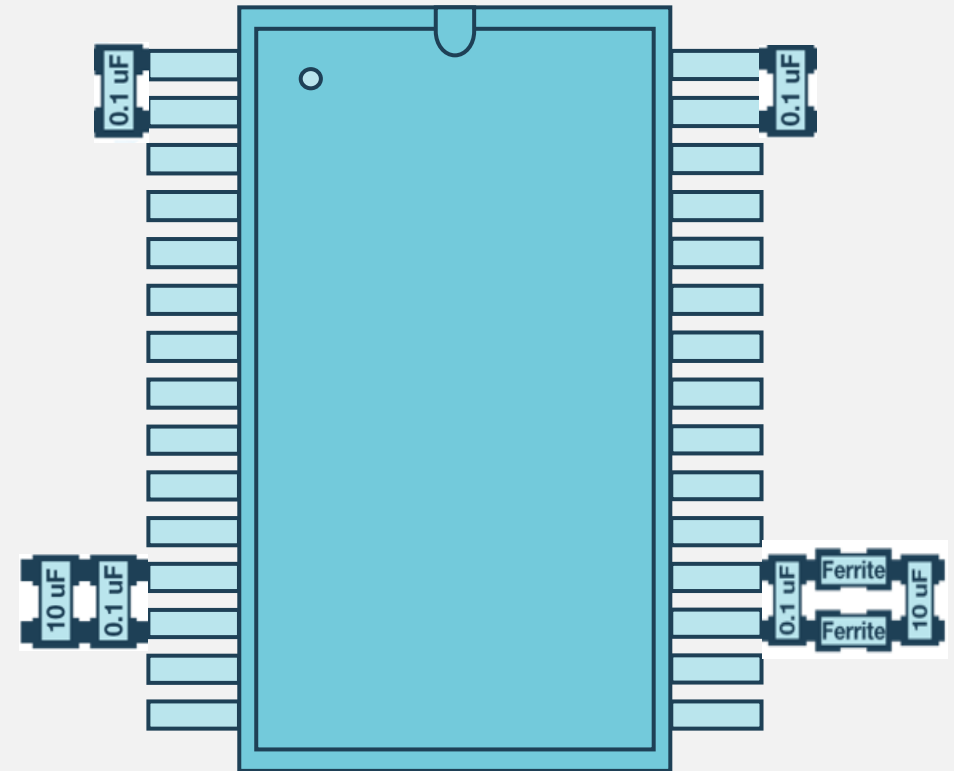


# A New Solution – ADuM6421A

- ▶ We need a solution **at the component level** that avoids generating high emissions
  - Improved coil design and coil driver circuits
  - Spectrum techniques to reduce the quasi-peak levels
  - Small inexpensive ferrite beads are used to block the high frequency common-mode currents on the secondary supply connections in order to reduce the dipole emissions further

Capable of passing CISPR 22 Class B emissions standard without the use of stitching capacitance on a 2 layer PCB

## The New *isoPower*® with 4-Channels of Isolated Data



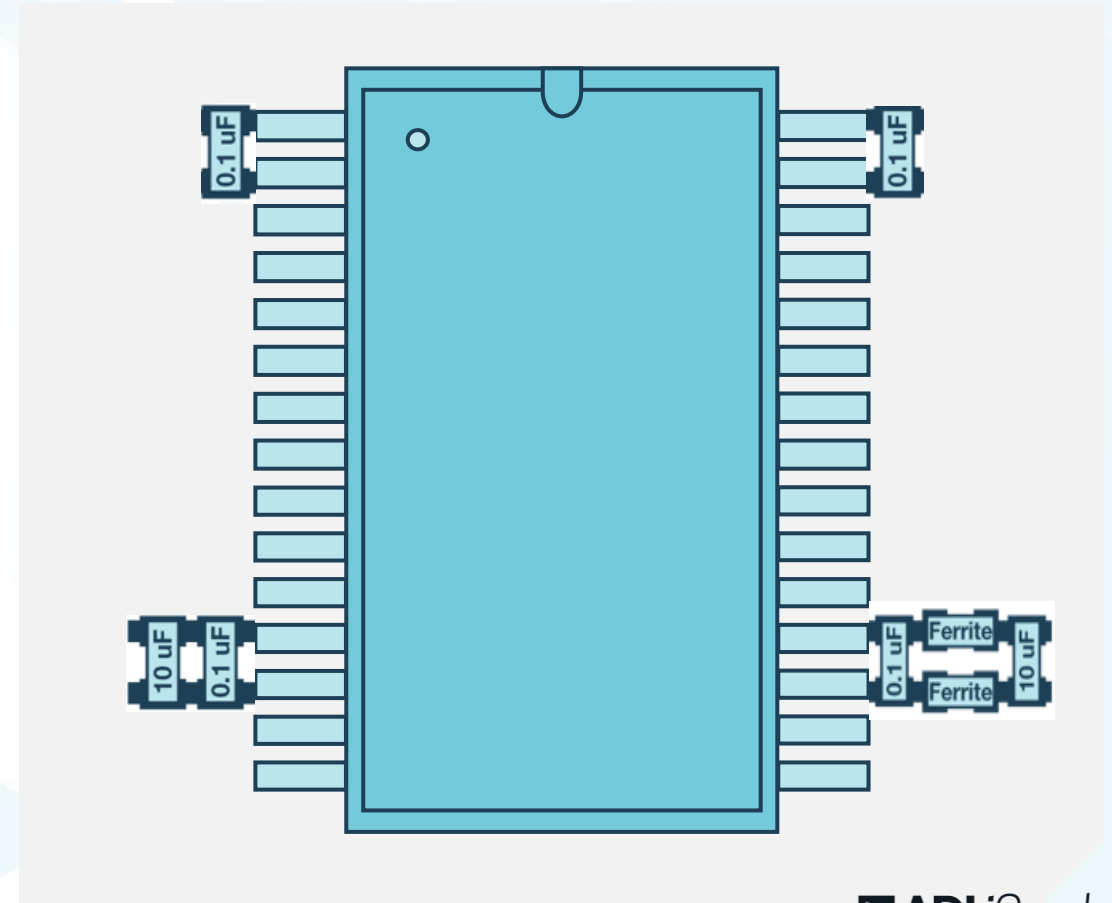
# A New Solution – ADuM6421A

Low Emissions *isoPower*® Integrated,  
Isolated DC-to-DC Converters  
With 4 – Channels of Isolated Data

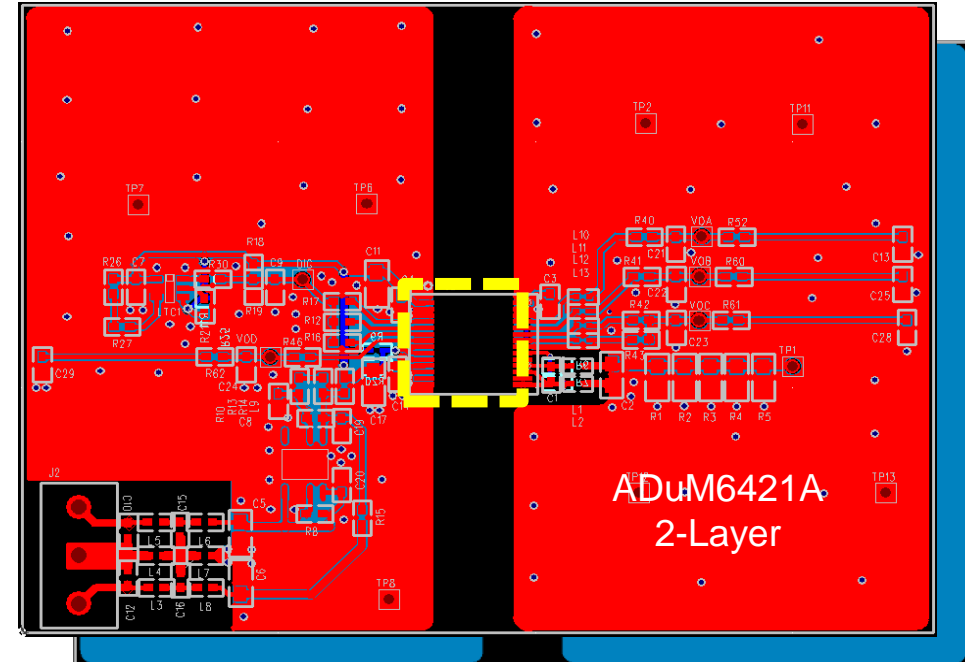
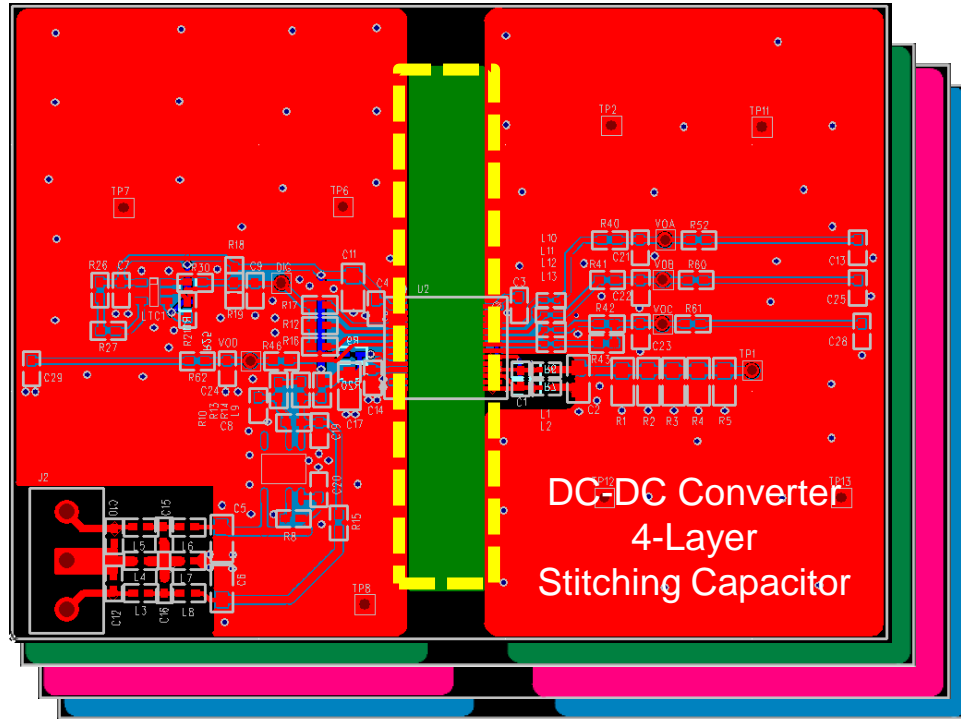


The ADuM6421A builds upon ADI's  
pioneering expertise in isolated data and  
power solutions

- ▶ Simplified EMC certification
  - Below EN 55022/CISPR 22 Class B emissions limits at full load on a 2 layer PCB
- ▶ Chip-scale package size
  - 28-lead Fine Pitch SOIC package with 8.3 mm minimum creepage
  - Same PCB real estate as 16 pin SOIC\_W
- ▶ 500 mW integrated isolated output power
- ▶ Data isolation
  - Four High Speed Data Channels with high 100 kV/μs CMTI and high immunity to electrical noise and magnetic interference for robust performance in harsh environments
- ▶ Safety Certifications



# The Advantage: Simple and Small 2-Layer PCB



## Space Savings

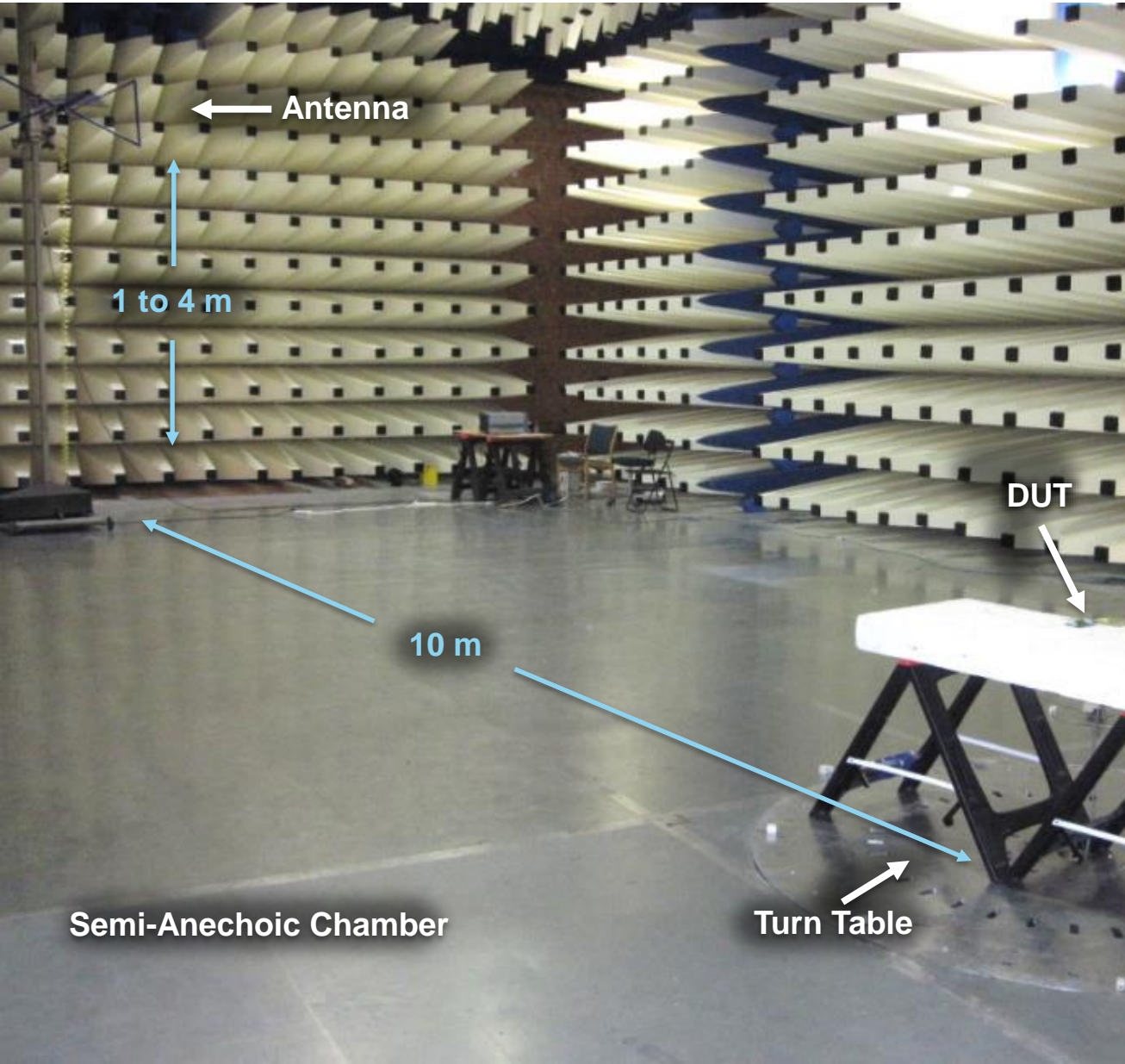
More than 70% PCB area savings

## Lower Material Cost

Up to 30% on a 2-layer PCB

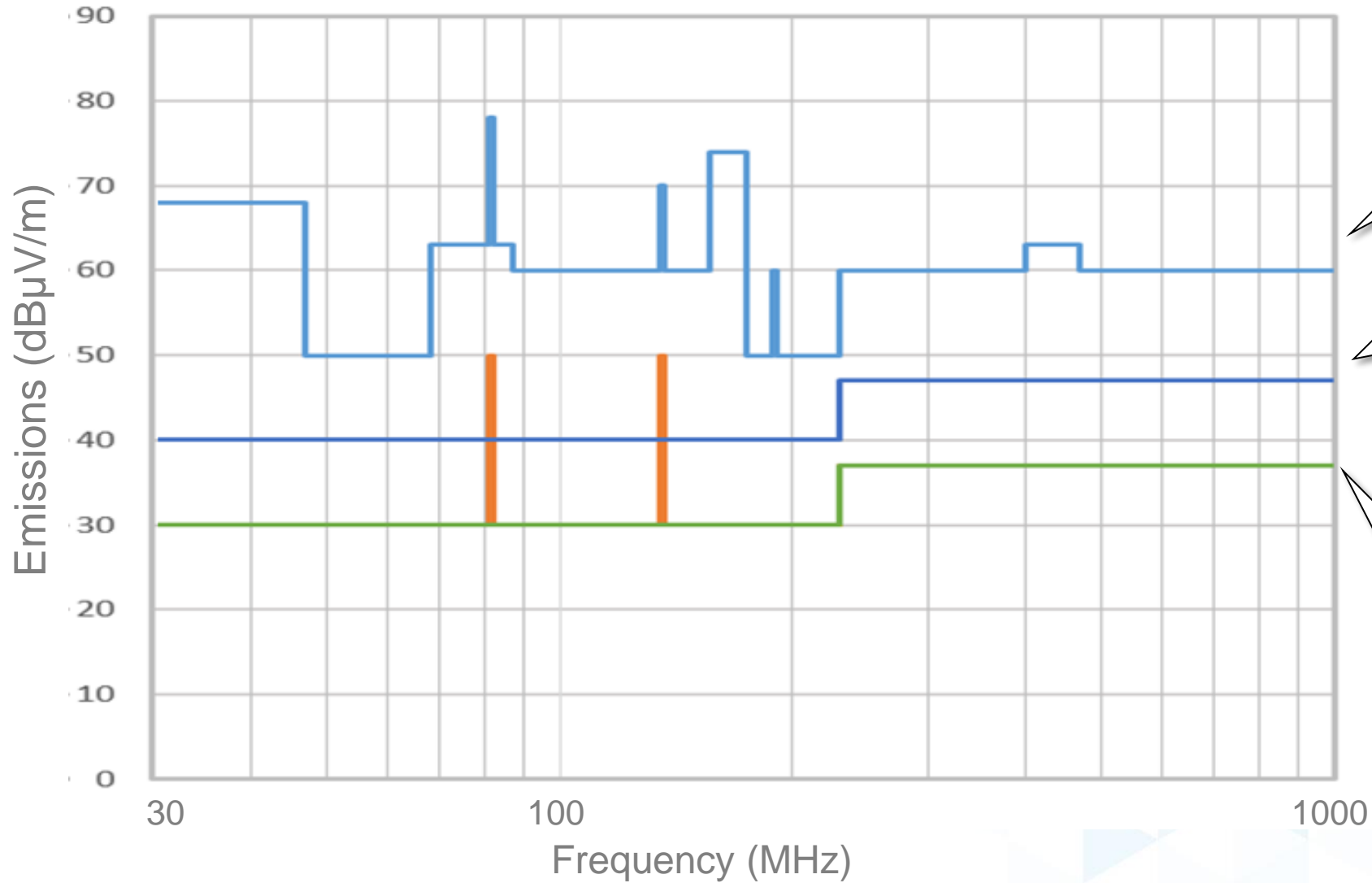
# CISPR 32 Test Set-up

# CISPR 32: Test Chamber Setup



- ▶ **Device under test (DUT)** in semi-anechoic chamber
  - Our evaluation board or
  - Customer board/module
- ▶ DUT/PCB on a nonconductive turntable
  - Non-floor standing DUTs must be 0.8 m above the horizontal ground reference plane
- ▶ Antenna detects emissions
  - 10 m from DUT
  - 1 m to 4 m height
  - Horizontal or vertical
- ▶ Auxiliary equipment placed outside the chamber

# Summary of Radiated Emissions Limits



CISPR 11 - Group 2 - Class A

CISPR 11 - Group 1 - Class A

CISPR 22 - Class A

CISPR 32 - Class A

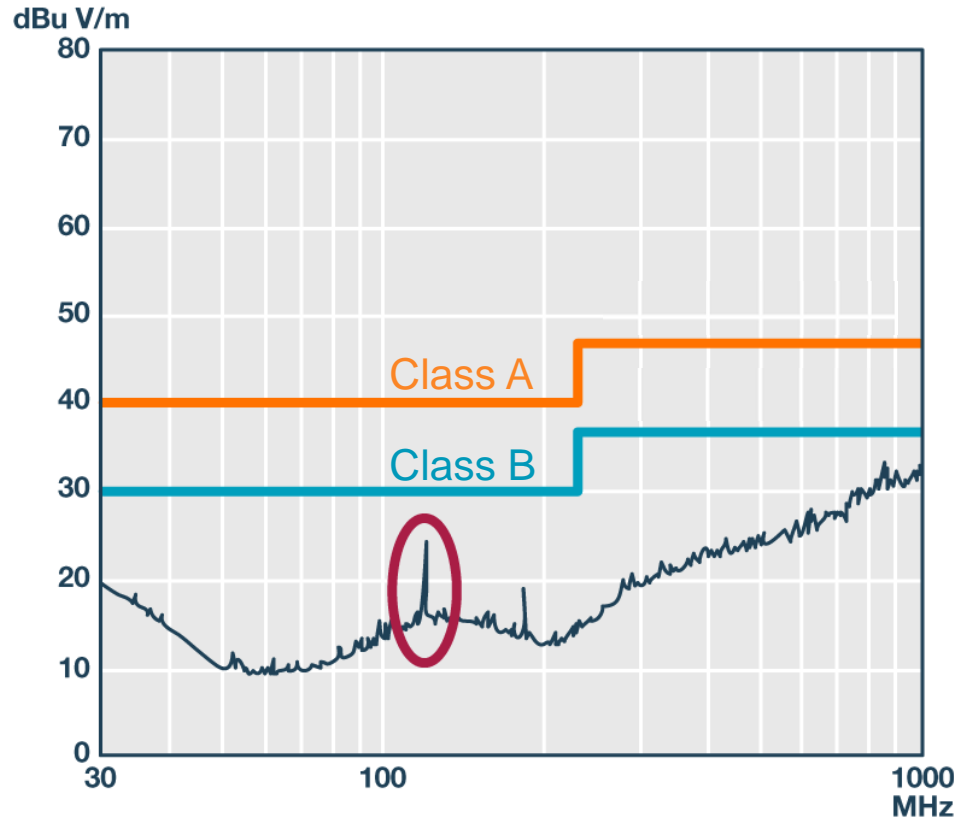
CISPR 11 - Group 2 - Class B

CISPR 11 - Group 1 - Class B

CISPR 22 - Class B

CISPR 32 - Class B

# CISPR 32: Test Procedure

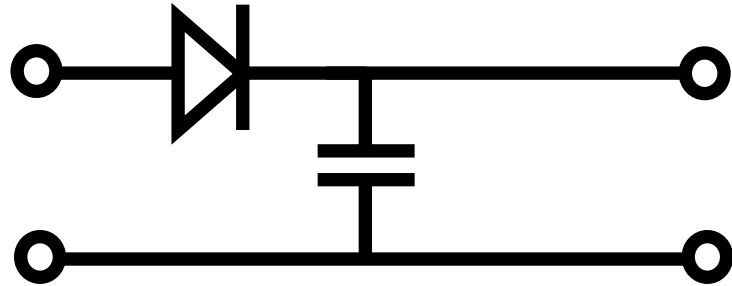


**CISPR 32 Class A and Class B  
Limits from 30 MHz to 1 GHz**

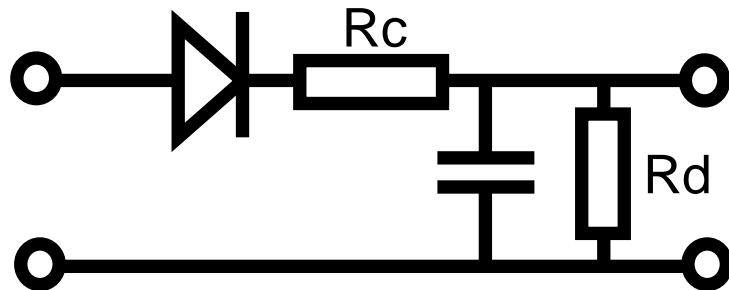
- Step 1: Find the peak emissions with a spectrum analyzer
- Step 2: Capture quasi-peak measurement
- Step 3: Use a full rotation of turntable and vary antenna height from 1 m to 4 m
- Step 4: Antenna used in horizontal and vertical orientations

# Peak versus Quasi-Peak?

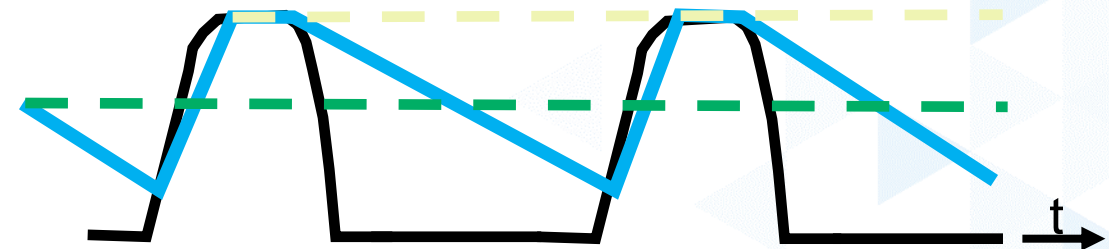
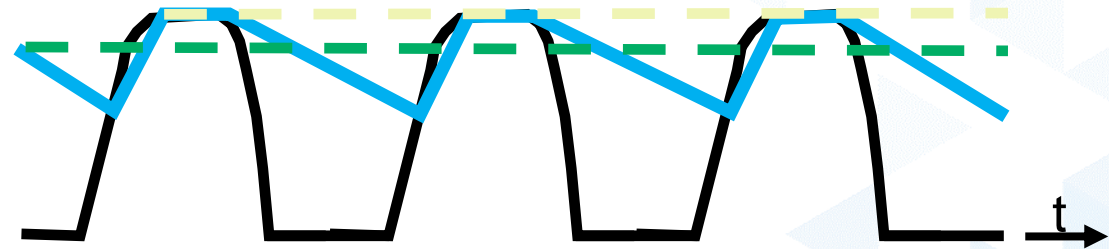
## Peak Detector



## Quasi Peak Detector



## Peak and Quasi-peak versus impulse rate



- Peak Detector Output
- Quasi Peak Response
- Quasi Peak Detector Output

Both Peak and Quasi peak measurements allow compliance to CISPR 32

# Why do you Need Margin for Radiated Emissions?

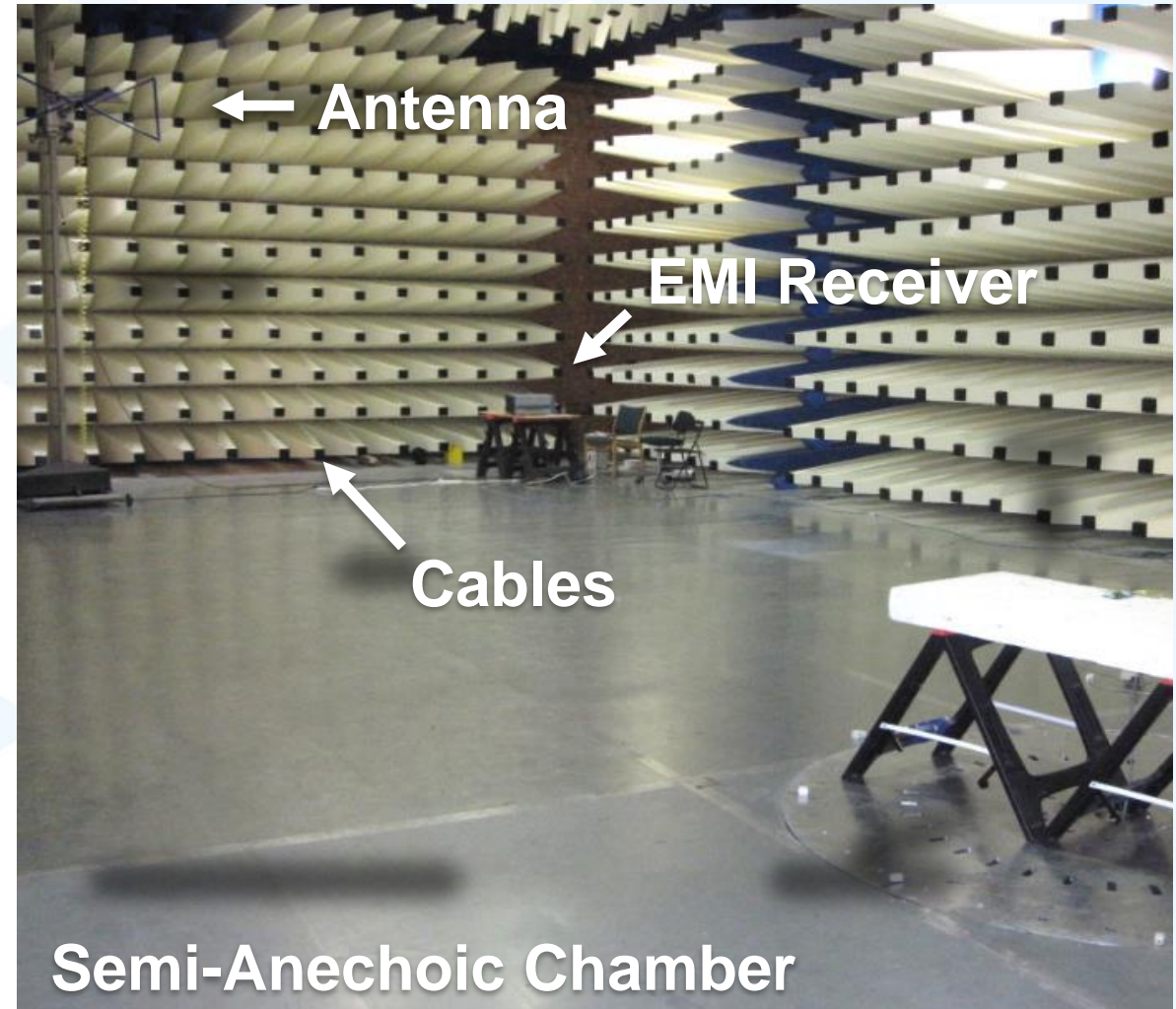
## 1. Quality of Semi Anechoic Chamber

The quality of the ground plane and how well reflections are controlled, Uncertainty:  $\pm 2$  dB

## 2. Accuracy and Calibration of Equipment

- a) Spectrum analyser, Uncertainty:  $\pm 1.5$  dB
- b) Antenna calibration, Uncertainty:  $\pm 2$  dB
- c) Cable inaccuracies, Uncertainty:  $\pm 0.5$  dB
- d) Use of a pre-Amplifier, Uncertainty:  $\pm 1.5$  dB

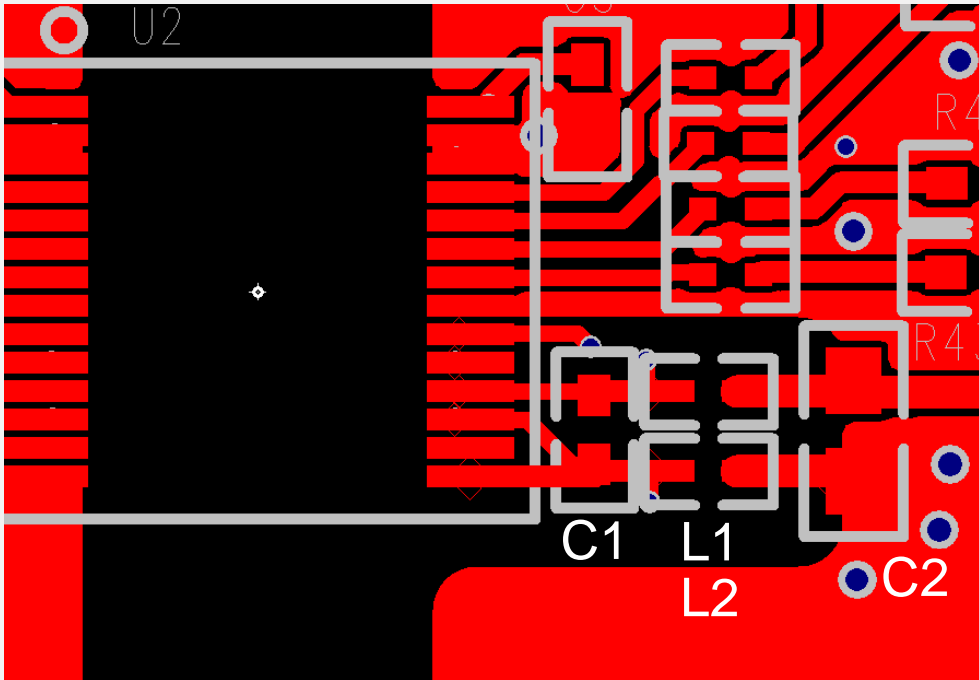
Uncertainty Approximately  $\pm 3$  dB



# EMI Test Results

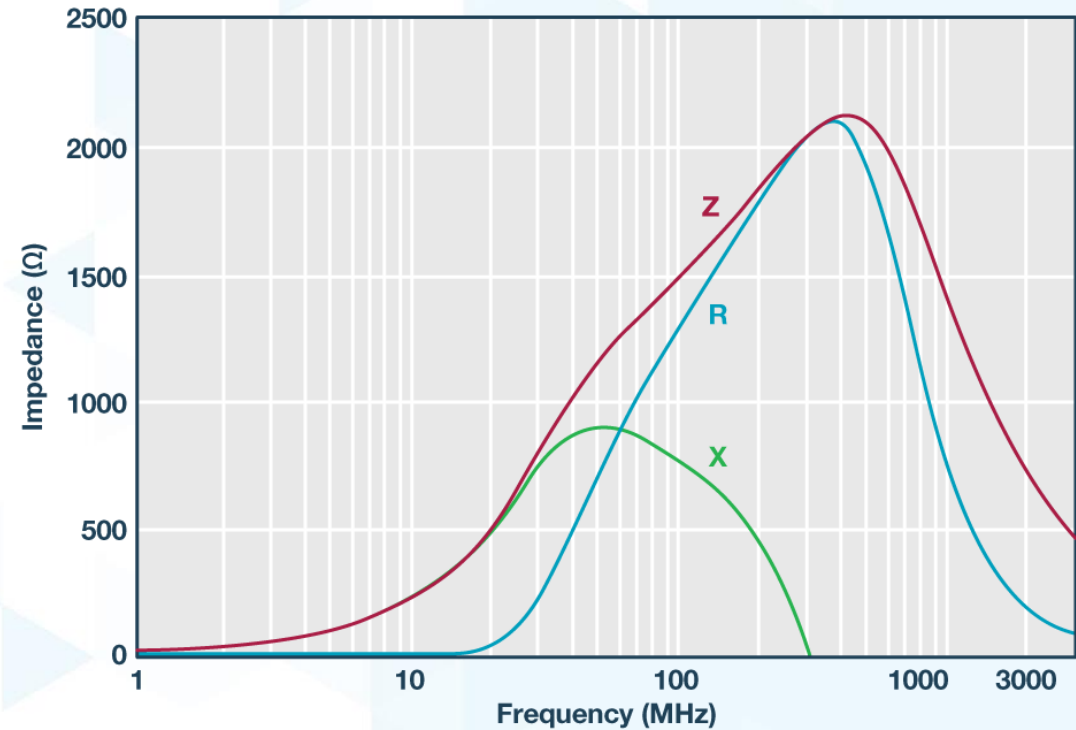
# Simplified 2 Layer PC Board Layout

ADuM6421A populated on a 2 layer PCB, meets CISPR 32 Class B using ferrites on  $V_{ISO}$  and  $GND_{ISO}$ , but without stitching capacitance



Example of ADuM6421A 28-lead Fine Pitched SOIC Layout around the integrated circuit

Ferrites L1, L2 and Bypass Capacitors C1, C2

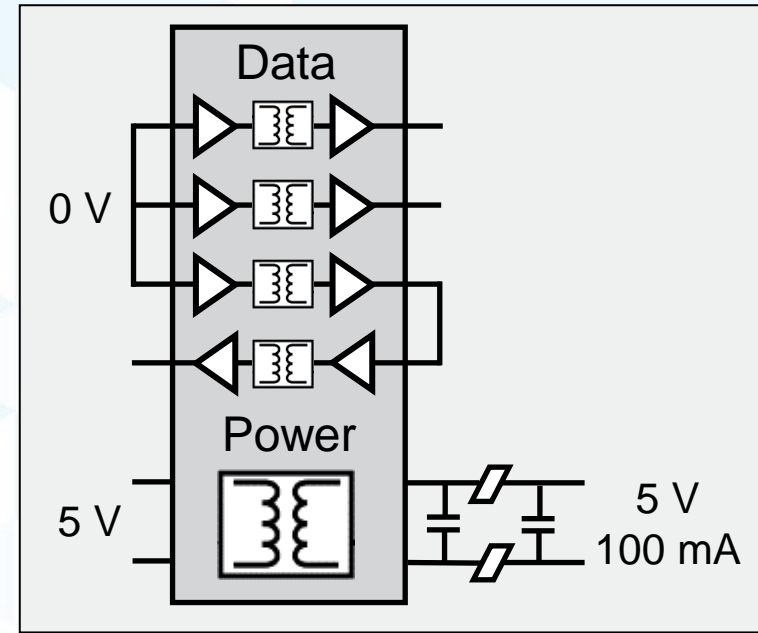
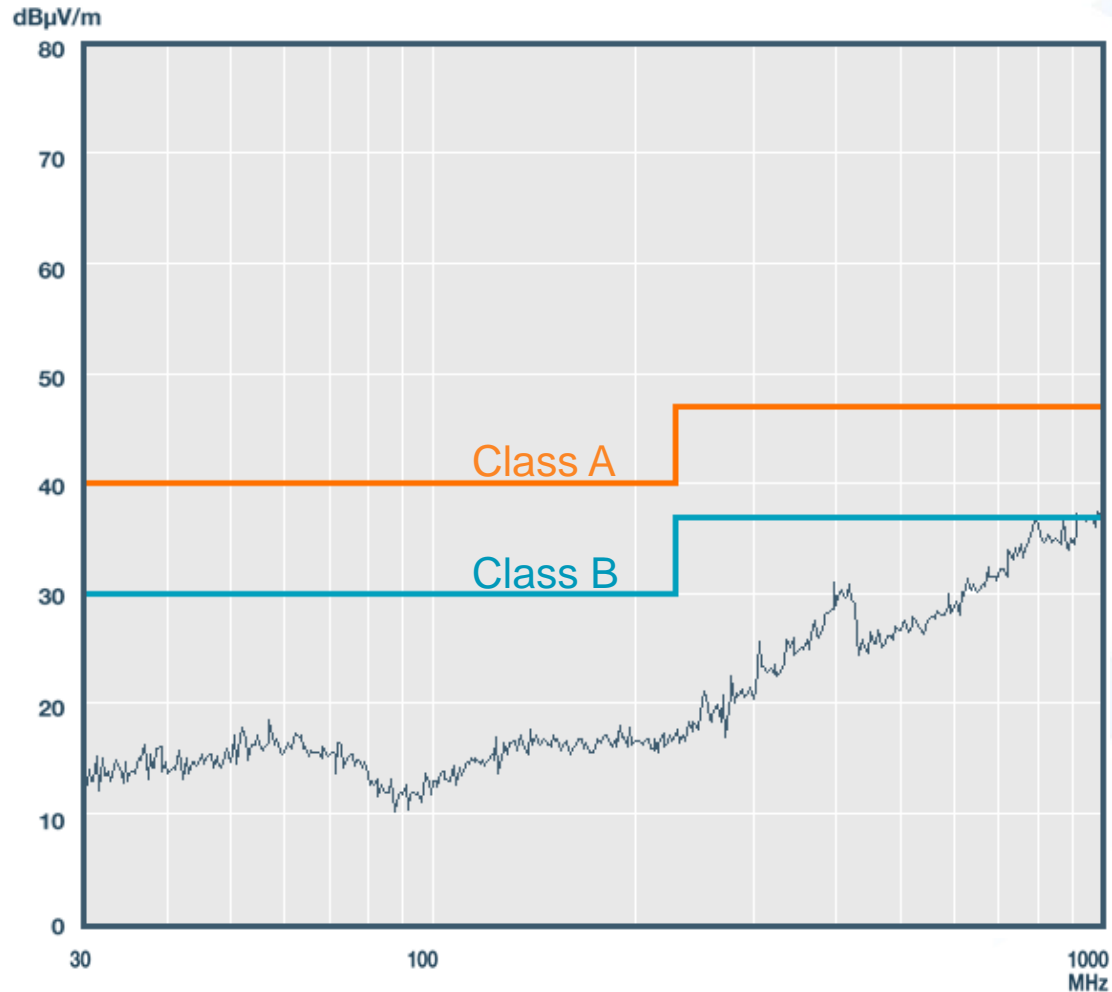


Ferrites L1, L2

Murata BLM15HD182SN1

Impedance of 1500 Ω from 100 MHz to 1000 MHz

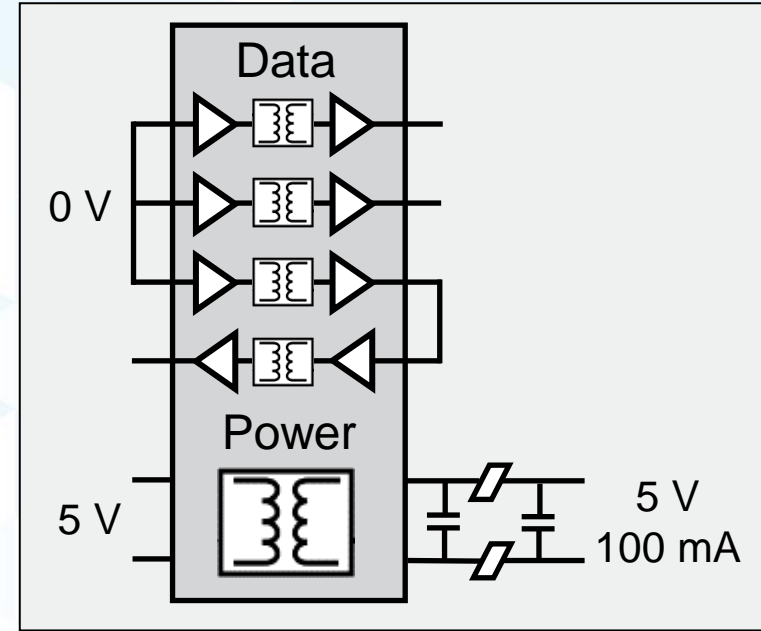
# ADuM6421A: Meeting CISPR 32 Class B



Frequency (MHz)	Quasi Peak (dBµV/m)	Margin to Class B (dB)
307.224	27.3	-9.7
397.09	30.2	-6.8
417.9	26.5	-10.5
791.467	32	-5
919.068	33.4	-3.6

Using 2 Layer PCB: Quasi-peak meets CISPR 32 Class B by 3.6 dB Margin

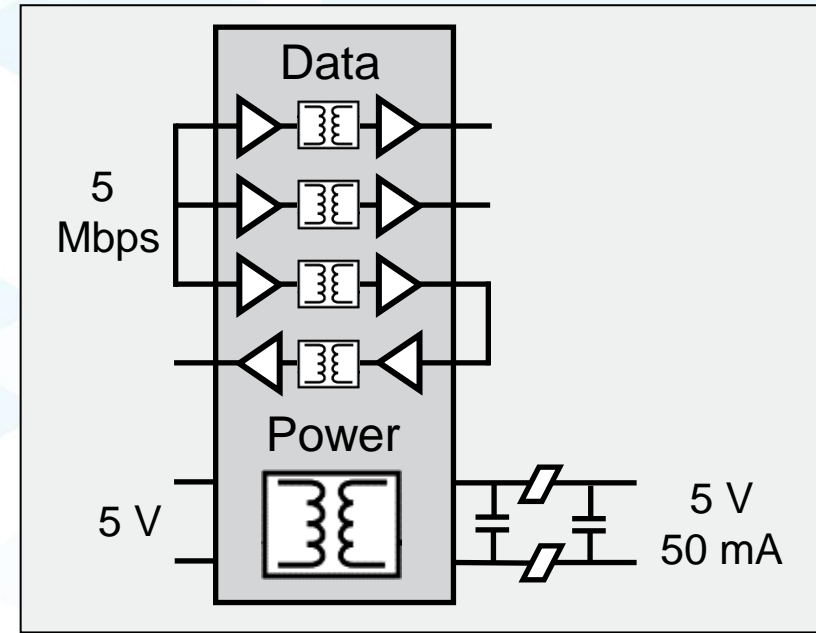
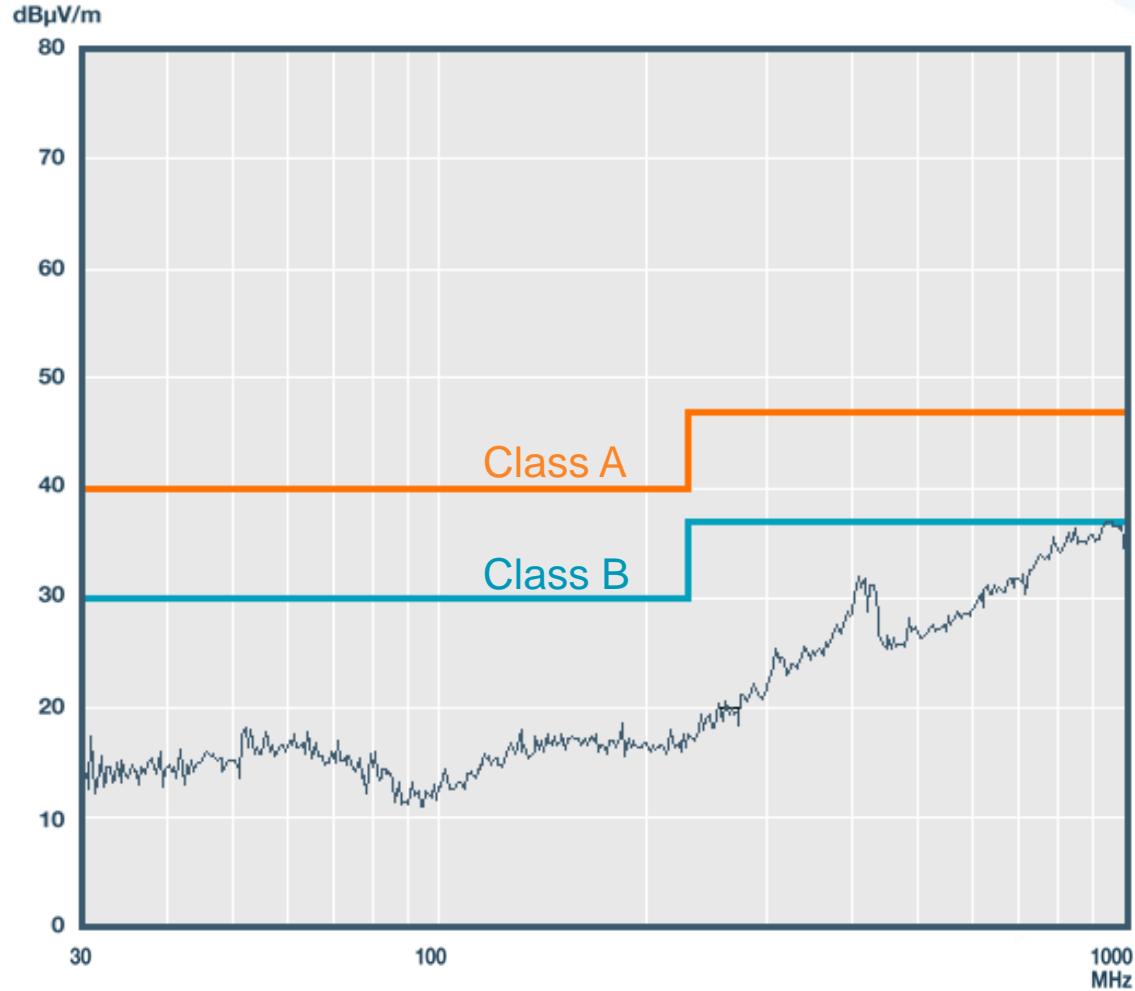
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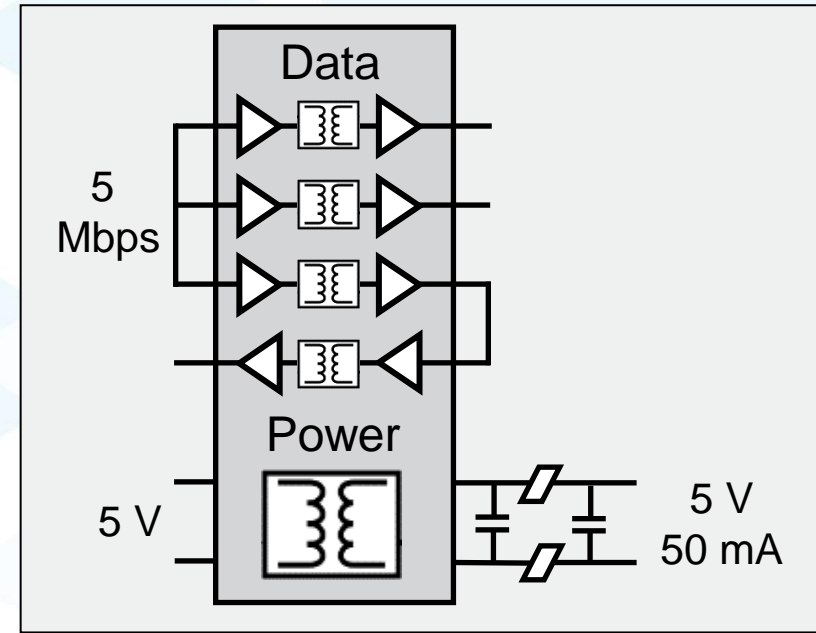
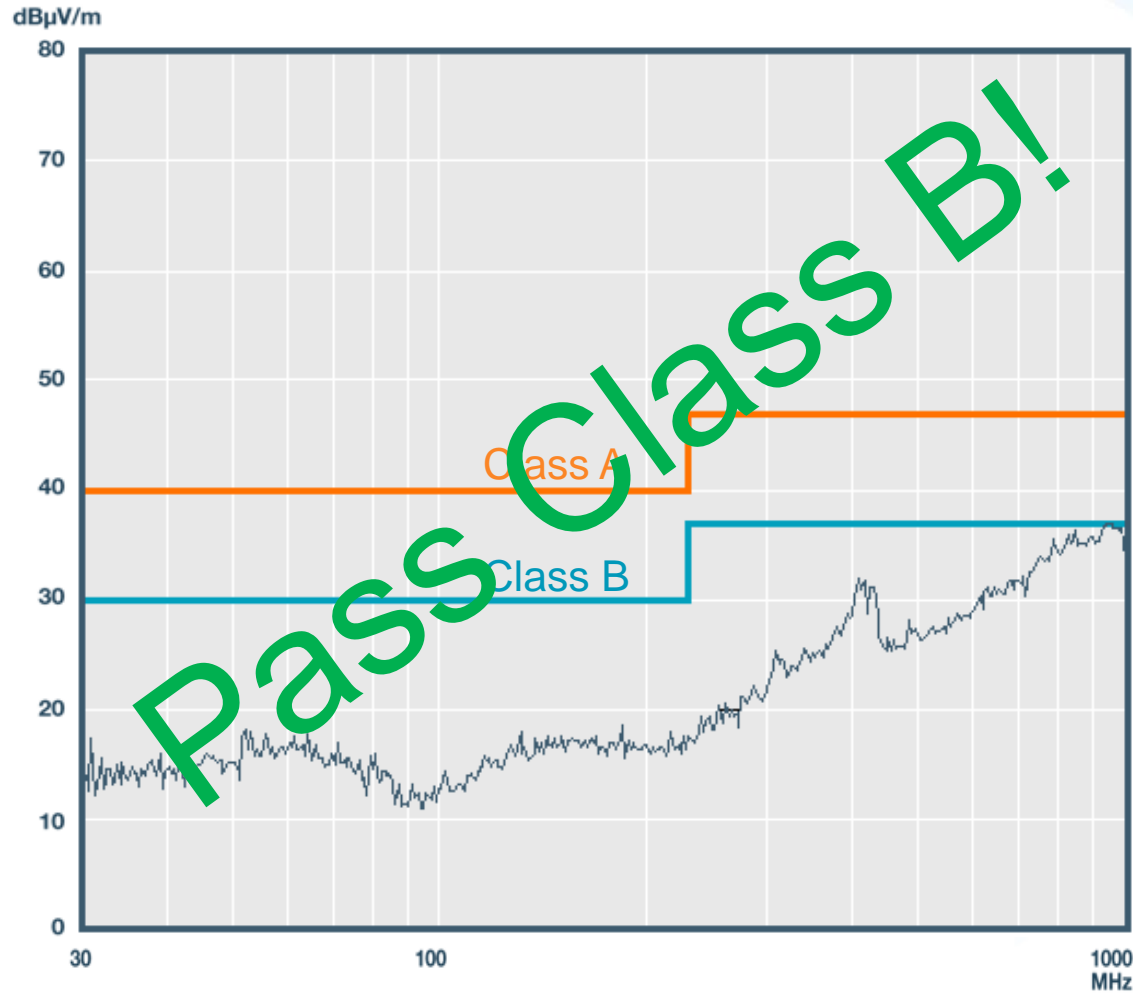
# ADuM6421A: Meeting CISPR 32 Class B



Frequency (MHz)	Quasi Peak (dBuV/m)	Margin to Class B (dB)
183.224	13.3	-16.7
310.9	28	-14.8
410.68	28.5	-8.5
429.564	27.8	-9.2
847.032	31	-6

**Using 2 Layer PCB: Quasi-peak meets CISPR 32 Class B by 6 dB Margin**

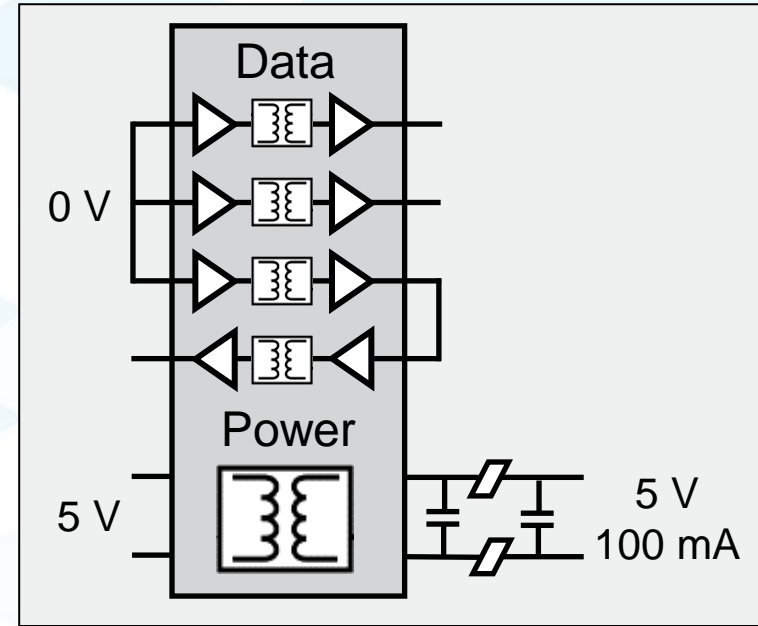
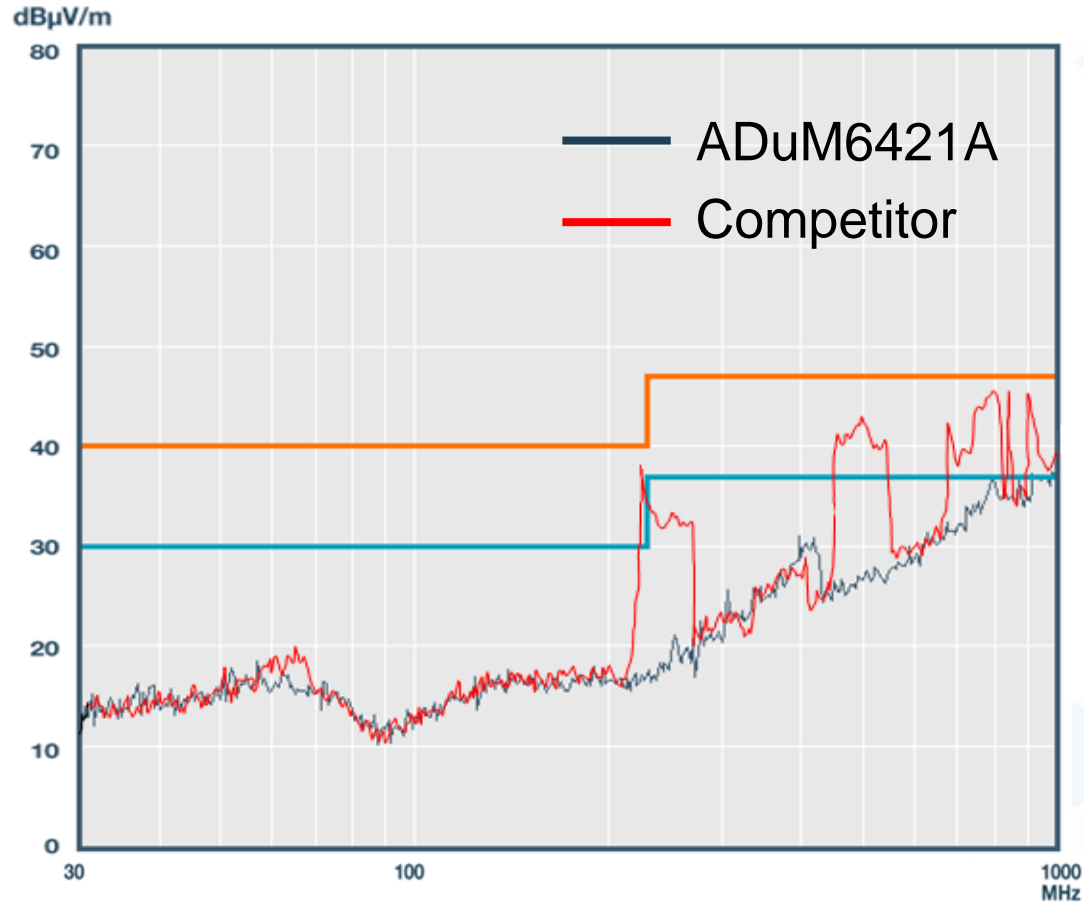
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Using 2 Layer PCB: Quasi-peak meets CISPR 32 Class B by 6 dB Margin

# ADuM6421A: Best in Class EMI Performance



- ▶ Comparison of chip scale solutions available in the market.
- ▶ Both devices tested under same conditions.

**Using 2 Layer PCB:  
ADuM6421A superior performance  
over chip scale competitor devices**

	Frequency (MHz)	Quasi Peak (dBµV/m)	Worst Case Margin to Class B (dB)
Competitor	225.58	42	+12
ADuM6421A	919.068	33.4	-3.6

# Expected Benefits and Next Steps

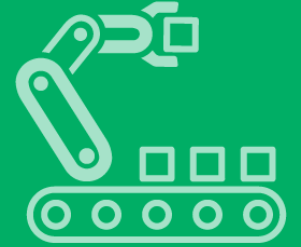
# New *isoPower*® with 4-channels of Isolated Data

## Compact, High Density, High Voltage Emerging Applications

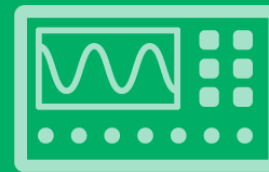
- ▶ **Regulatory Compliance**  
Meets CISPR 22 Class B  
standards



Battery Monitoring  
and Inverters



Programmable Logic  
Controller (PLC)



Precision  
Measurement



Vital Signs  
Monitoring

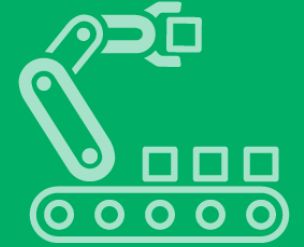
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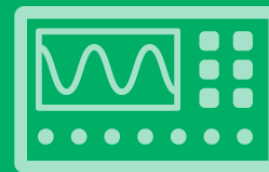
- ▶ **Reduced Complexity**  
No stitching capacitance  
needed



Battery Monitoring  
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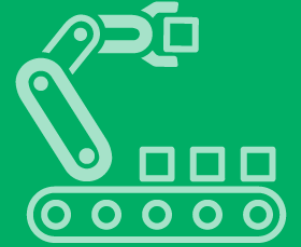
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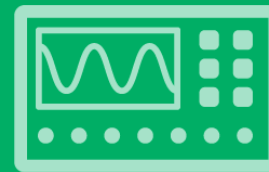
- ▶ **Lower Material Cost**  
Up to 30% on a  
2-layer PCB



Battery Monitoring  
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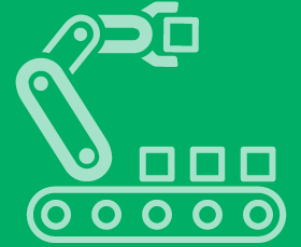
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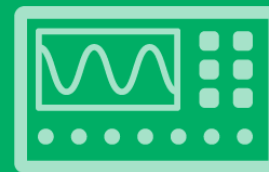
- ▶ **Smaller Application Size**  
Up to 70% PCB space  
savings



**Battery Monitoring  
and Inverters**



**Programmable Logic  
Controller (PLC)**



**Precision  
Measurement**



**Vital Signs  
Monitoring**

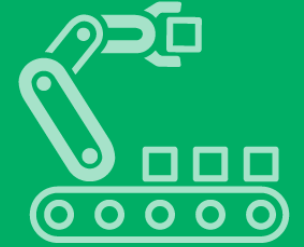
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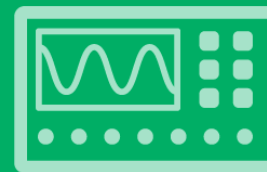
- ▶ **Faster Time to Market**  
Reduced PCB design  
and test time



Battery Monitoring  
and Inverters



Programmable Logic  
Controller (PLC)



Precision  
Measurement

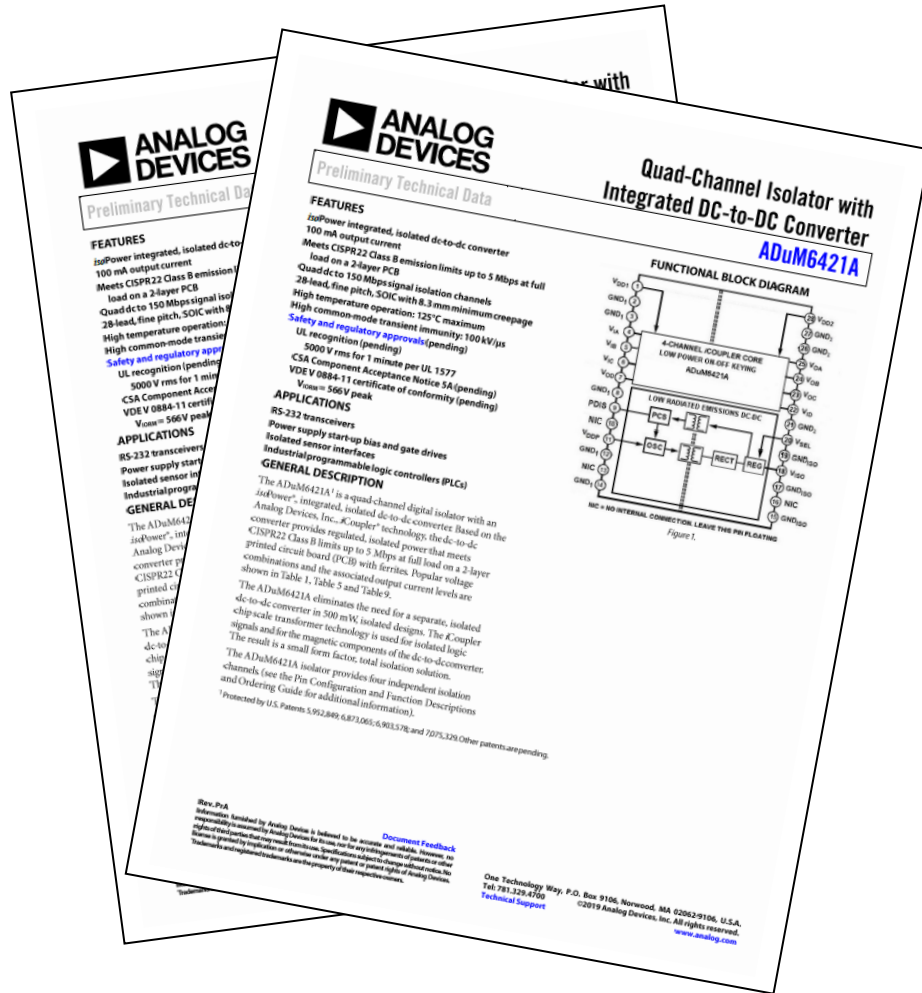


Vital Signs  
Monitoring

# Next Steps with ADuM6421A

Visit [analog.com/ADuM6421A](http://analog.com/ADuM6421A) for more resources

Order an eval board EVAL-ADuM6421AEBZ with user guide containing layout and emissions data



# ADI iCoupler®

