SPC5 Studio

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FOTA Develop with SPC5-STUDIO

Targeting SPC58 Chorus MCU

Neo JUNG

Agenda

1. SPC58 Chorus Family
2. SPC5-STUDIO
3. Background : FOTA
4. AFLS + FOTA

SPC58 Chorus Family

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SPC58 Chorus Advantage

Ready Now

SECURITY

Best Subsystem Separation

Fast data decryption capability

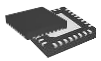
Evita Medium and Full

ISO CAN FD & Ethernet

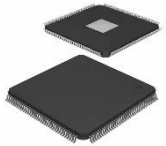
100% Can FD

SW & Pin to PIN scalability

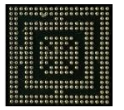
Unprecedented Scalability



QFN 7x7



eTQFP 64-176



BGA292/302/386

Ready for on the fly reprogr.

SW and HW modes, eMMC, USB, Hyper-bus

New Low power Modes

ADC monitoring capability in Stand By

RAM up to 1.376Mbyte

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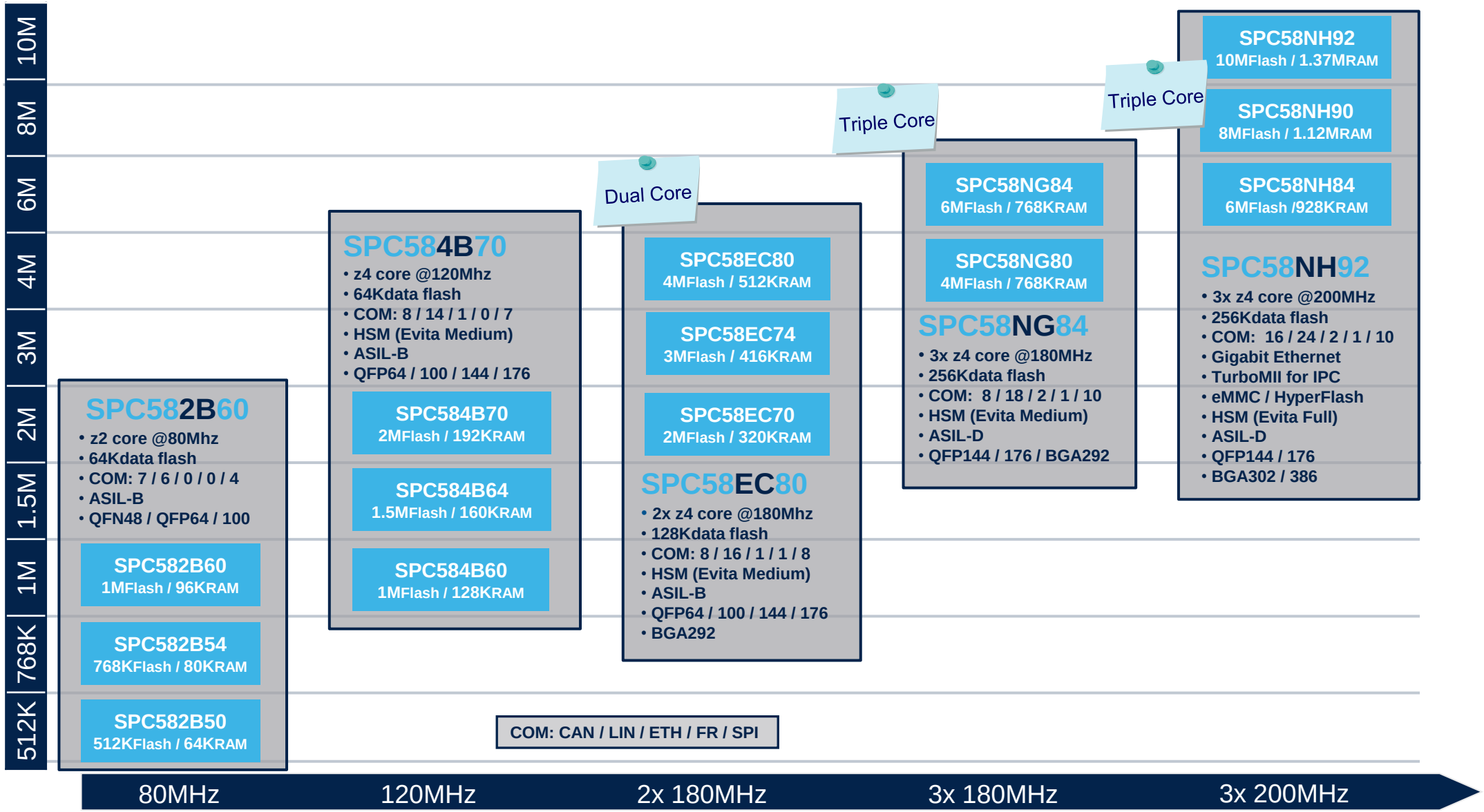
SPC58 Chorus Family



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Chorus 2M SPC584B

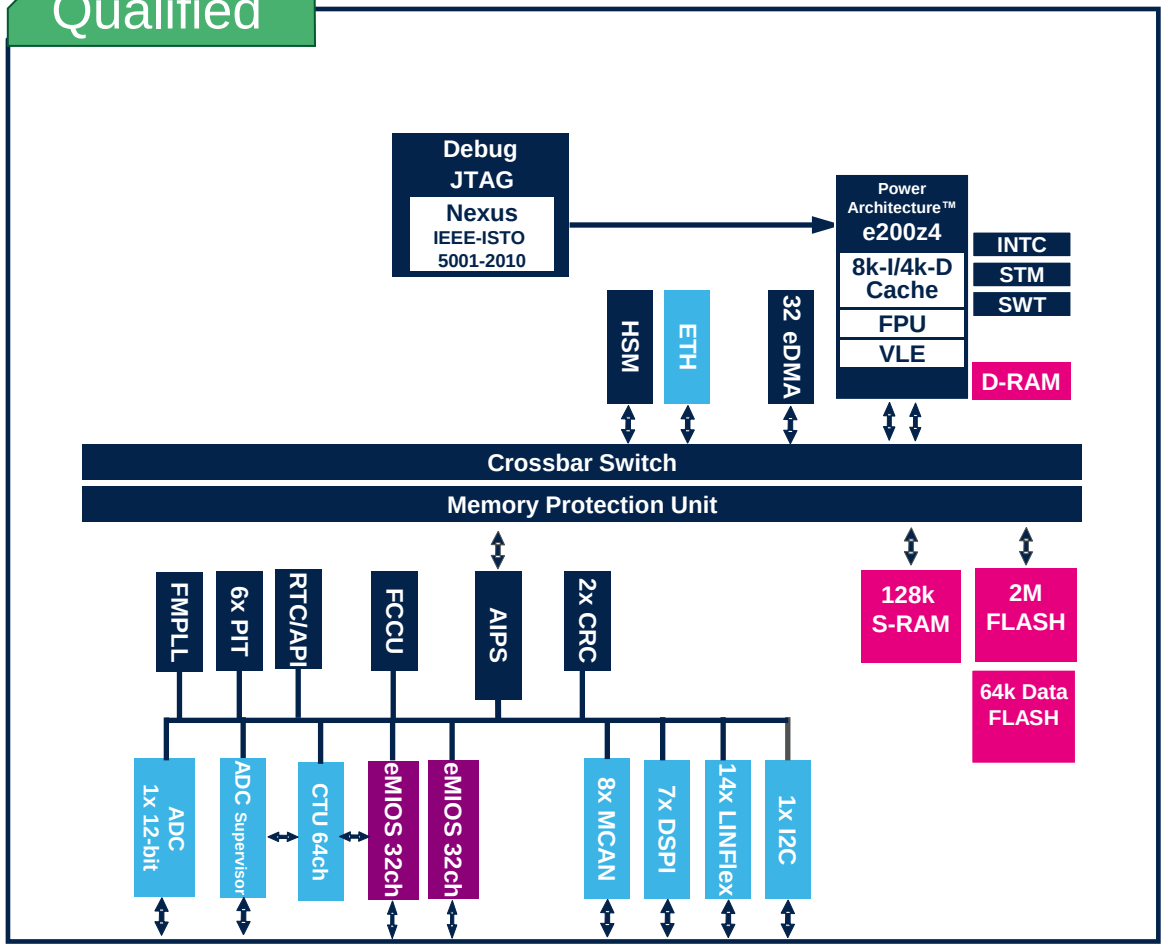
Core
- **120 MHz Power Architecture™ ISA e200z4 Core (VLE)**
  - Dual Issue Core with Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 64k Local d-RAM

Memory
- **2M byte RWW Flash with ECC**
- **4x16k Data Flash with ECC**
- **192k RAM** (128k SRAM, 64k Local d-RAM) **with ECC**

I/O
- **8 x MCAN / FD-CAN**
- **14 x LINFlex**
- **1 x Ethernet** (100Mb/s, time stamping, AVB, IPv4 Checksum)
- **7 x DSPI**
- **1 x I2C**
- **2x 32ch eMIOS**
- **64ch CTU (Cross Triggering Unit)**
- **64 channel ADC**
  - 2x 12-bit ADC
  - 1x 12-bit ADC Supervisor
  - 1x 10-bit Standby ADC

System
- **SSWU** (Smart Standby Wake-up)
- **Security Module: HSM** (Evita Medium)
- **FM-PLL**
- **MPU**
- **32 Channel eDMA Controller**
- **2 x CRC Unit**
- **Fault Collection & Control Unit**
- **6 x PIT / 1x STM / 1x RTC/API**
- **Nexus IEEE-ISTO 5001-2010 Class 3+**

Qualified



System Platform | Memory | Timer | Peripherals

Freq. Max	Voltage	Temp.	ASIL	I/O	Package
120MHz	5V / 3.3V	-40 / +125°C	B	150	64/100/144/176

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Chorus 4M SPC58EC

Core

- **180MHz Power Architecture™ ISA e200z4 Core (VLE)**
  - Dual Issue Core with Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 64k Local d-RAM

- **180MHz Power Architecture™ ISA e200z4 Core (VLE)**
  - Dual Issue Core with Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 64k Local d-RAM

Memory

- **4M byte RWW Flash with ECC**
- **4x32k Data Flash with ECC**
- **512k RAM** (384k SRAM, 2x 64k Local D-RAM) **with ECC**

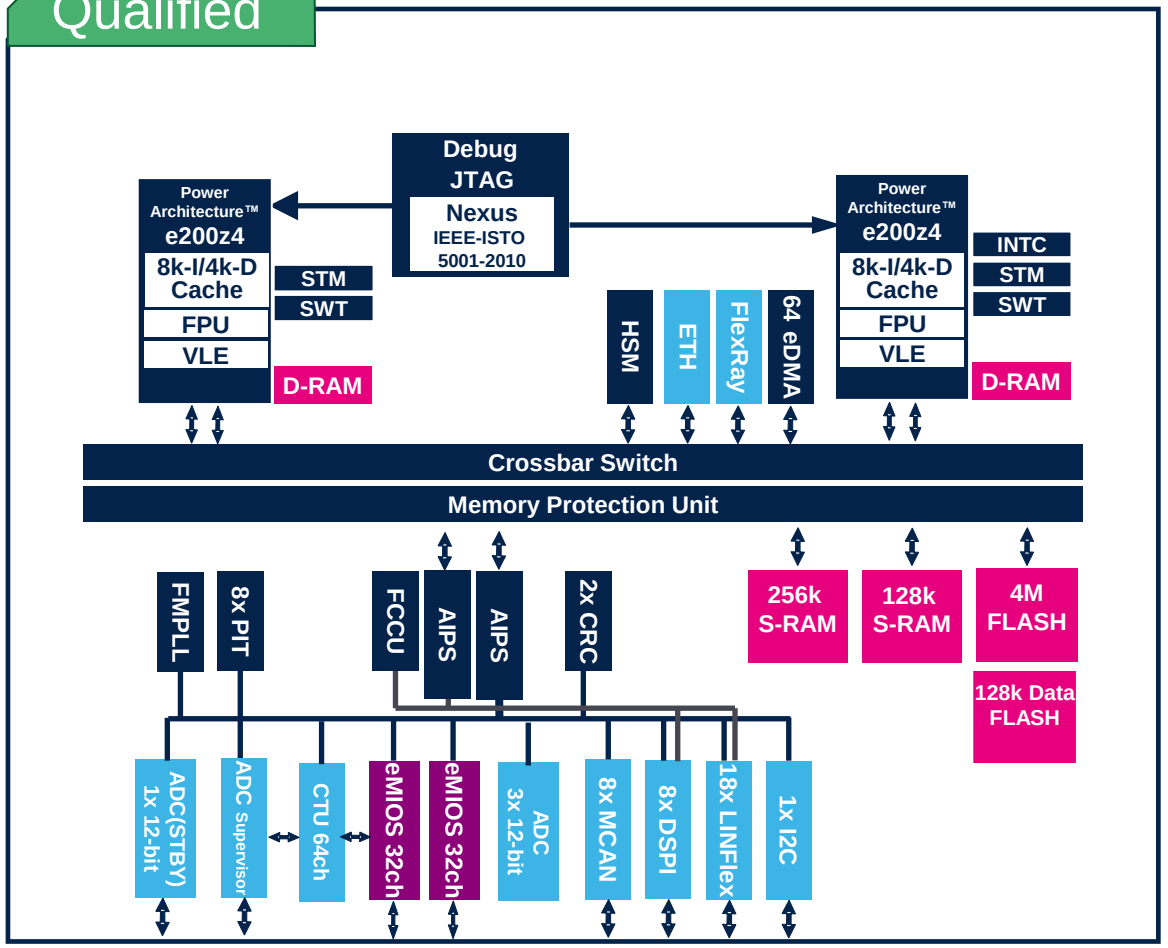
I/O

- **8 x MCAN / FD-CAN**
- **18 x LINFlex**
- **1 x Ethernet** (100Mb/s, time stamping, AVB, IPv4 Checksum)
- **Dual Channel FlexRay (**10MB/s, 128 buffers **)**
- **8 x DSPI, 1 x I2C 2x 32ch eMIOS**
- **64ch CTU (Cross Triggering Unit)**
- **95 channel ADC**
  - 3x 12-bit ADC
  - 1x 12-bit ADC Supervisor
  - 1x 10-bit Standby ADC

System

- **SSWU** (Smart Standby Wake-up)
- **Security Module: HSM** (Evita Medium)
- **FM-PLL**
- **MPU**
- **64 Channel eDMA Controller**
- **2 x CRC Unit**
- **Fault Collection & Control Unit (incl. error pin)**
- **8x PIT / 1x STM / 1x RTC/API**
- **Nexus IEEE-ISTO 5001-2010 Class 3+**

Qualified



System Platform | Memory | Timer | Peripherals

Freq. Max	Voltage	Temp.	ASIL	I/O	Package
180MHz	5V / 3.3V	-40 / +125°C	B	215	64/100/144/176/292

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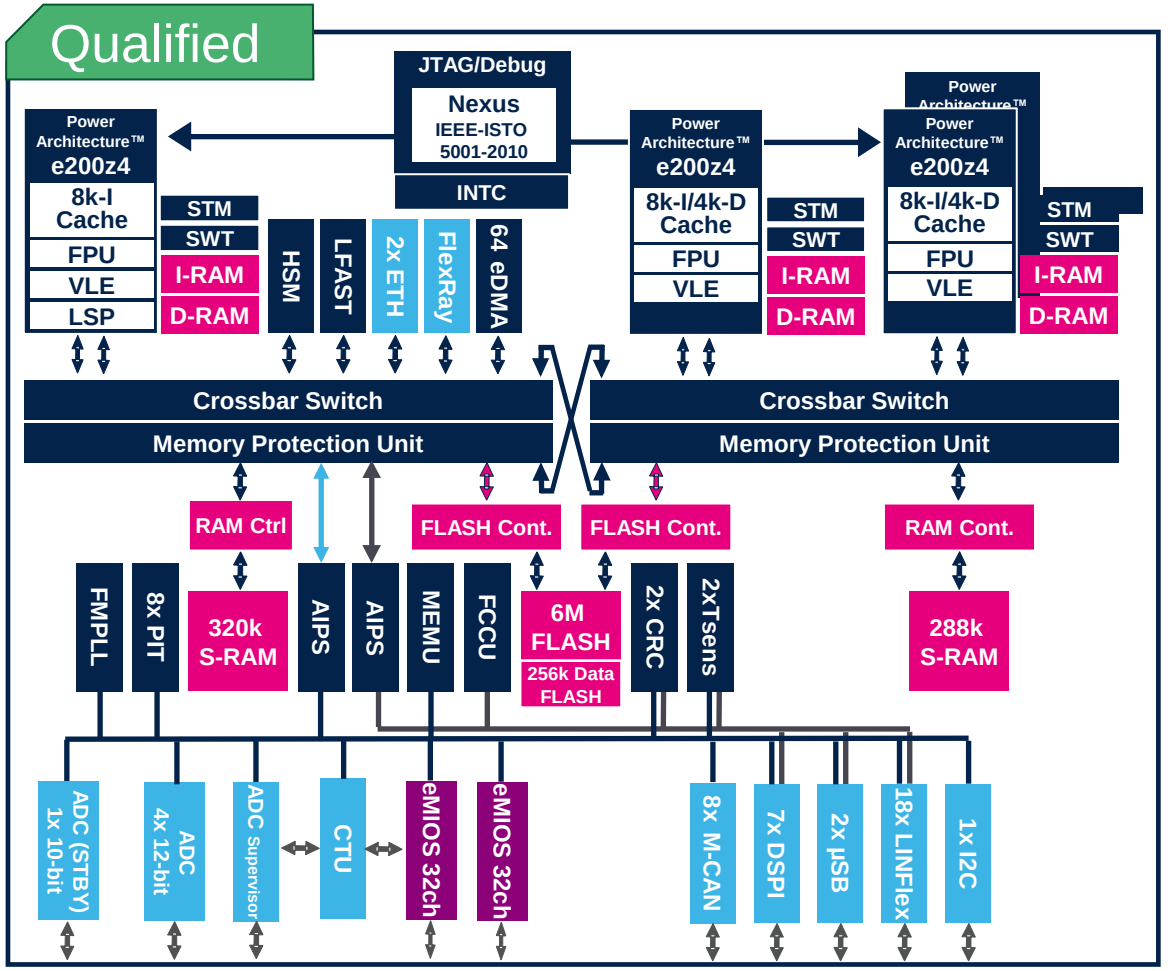
Chorus 6M SPC58NG

Core
- **180MHz Power Architecture™ ISA e200z4 Core (VLE)**
  - Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 16k Local i-RAM, 64k Local d-RAM
  - Lock Step (optional)
- **180MHz Power Architecture™ ISA e200z4 Core (VLE)**
  - Floating Point Unit
  - 8k-Instruction Cache, 4k-Data Cache
  - 16k Local i-RAM, 64k Local d-RAM
- **180MHz Power Architecture™ ISA e200z4 Core (VLE)**
  - Floating Point Unit & LSP(DSP)
  - 8k-Instruction Cache
  - 16k Local i-RAM, 32k Local d-RAM

Memory
- **6M byte RWW Flash with ECC**
  - 4x64k Data Flash with ECC
- **768kRAM** (608k SRAM + 160k d-RAM) **with ECC**
  - Including 256k Standby

I/O
- **8 x MCAN / FD-CAN**
- **18 x LINFlex**
- **2 x Ethernet** (100Mb/s, time stamping, AVB, IPv4 Checksum)
- **Dual Channel FlexRay** (10MB/s, 128 buffers)
- **10 x DSPI, 1 x I2C**
- **2x 32ch eMIOS**
- **64ch CTU** (Cross Triggering Unit)
- **86 channel ADC**
  - 4x 12-bit ADC
  - 1x 12-bit ADC Supervisor
  - 1x 10-bit Standby ADC

System
- **SSWU** (Smart Standby Wake-up)
- **Security Module: HSM** (Evita Medium)
- **FM-PLL**
- **MPU**
- **64 Channel eDMA Controller**
- **2 x CRC Unit**
- **Fault Collection & Control Unit (incl. error pin)**
- **8 x PIT / 1x STM / 1x RTC/API**
- **1x LFAST (Interprocessor bus)**
- **Nexus IEEE-ISTO 5001-2010 Class 3+** (Aurora interface)



System Platform | Memory | Timer | Peripherals

Freq. Max	Voltage	Temp.	ASIL	I/O	Package
180MHz	5V / 3.3V	-40 / +125°C	D	205	144/176/292

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SPC5-STUDIO

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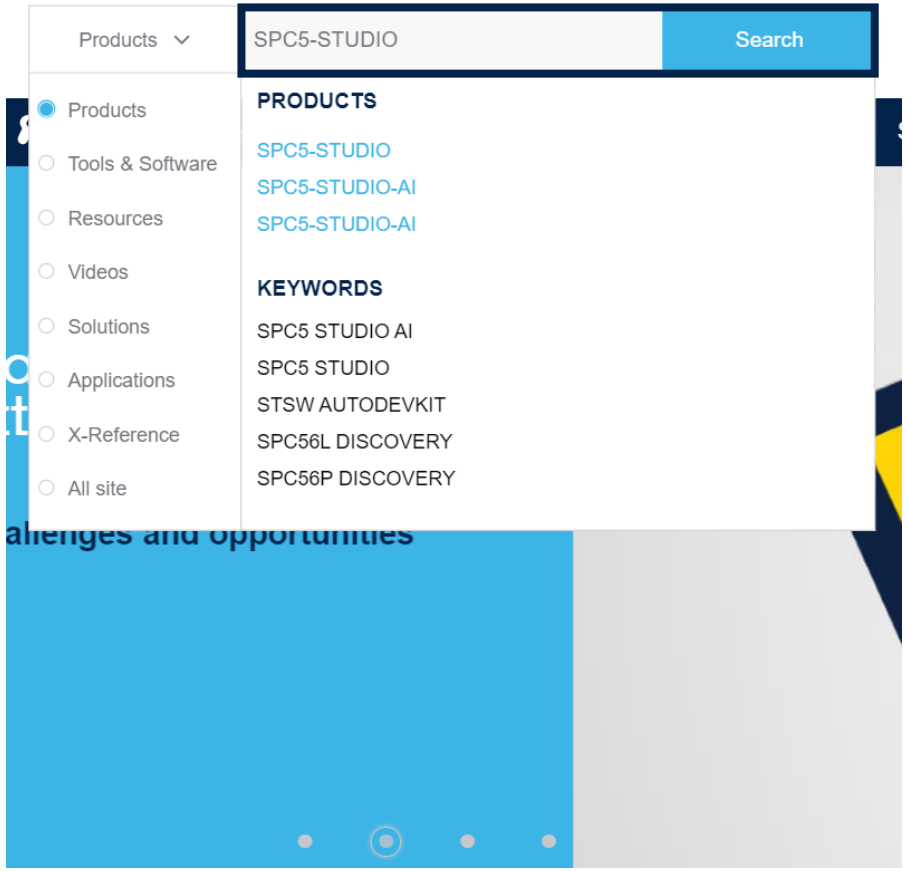
SPC5-STUDIO

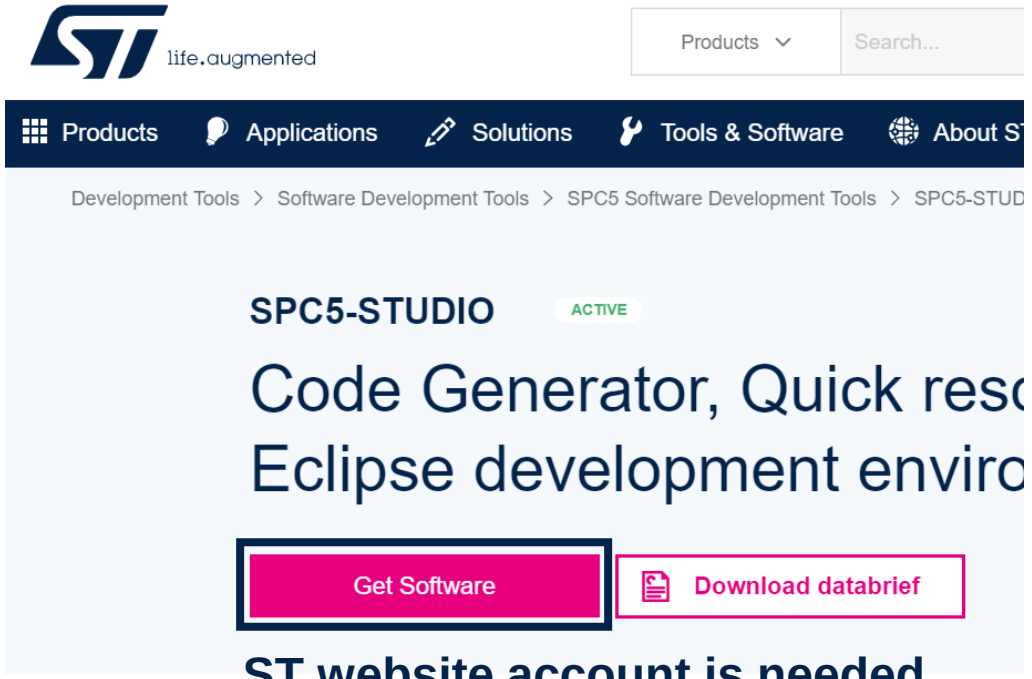
- Features
  - OpenSource Integrated Development Environment (IDE) based on ECLIPSE
  - Code, Makefiles, ELF, and Doc Generation based on a template structure
  - Full MISRA 2012 compliant Register Level Access (RLA) low level drivers
  - Easy to use MCU's Pins & Run modes & Clock tree configuration
  - Software Examples for Discovery kits and premium evaluation boards
  - Free GCC / GHS / HighTec compiler support

- SPC5-STUDIO LLD is targeting evaluation purpose only.
- Further integration work should be needed for mass production.

How to Get SPC5-STUDIO

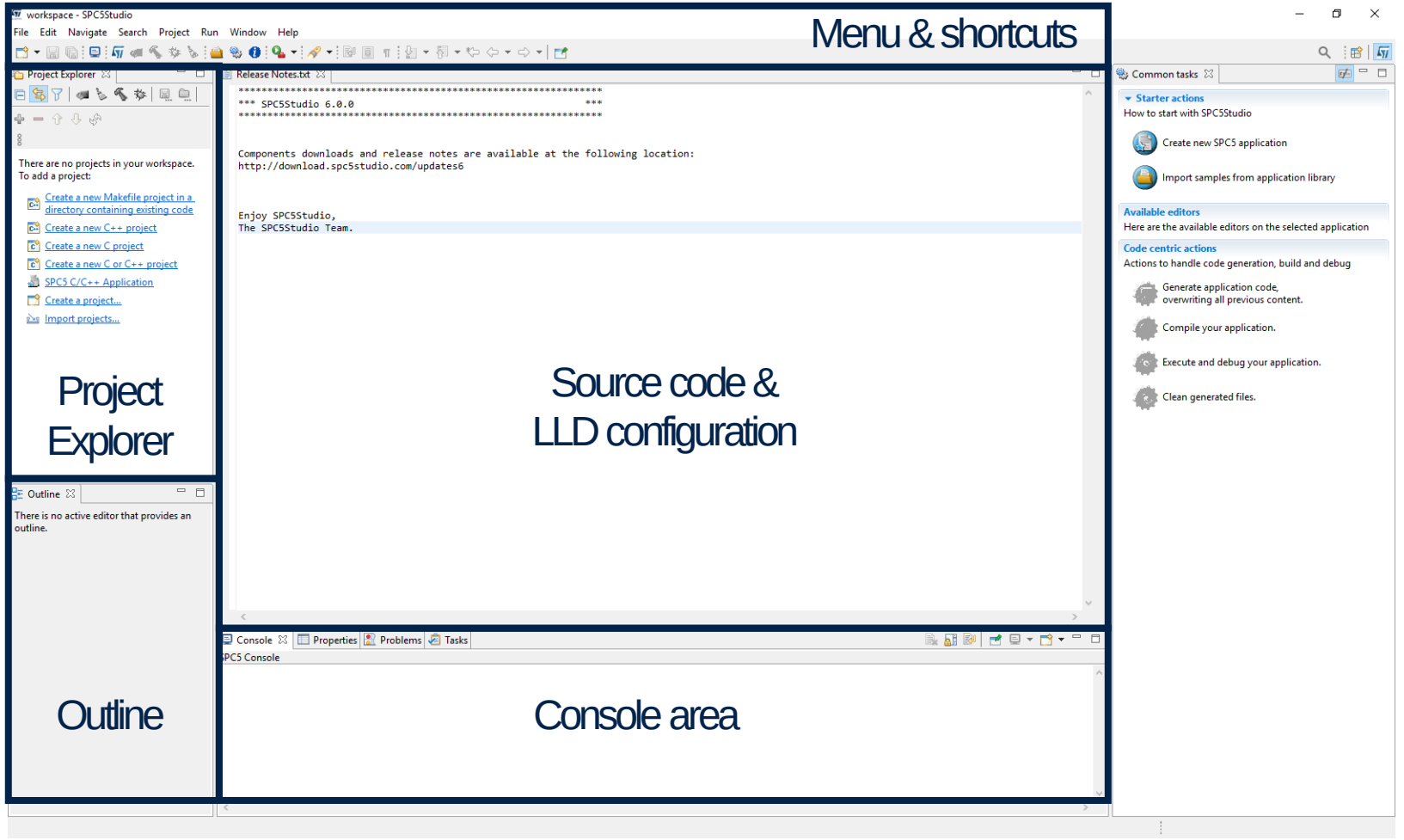
- https://st.com





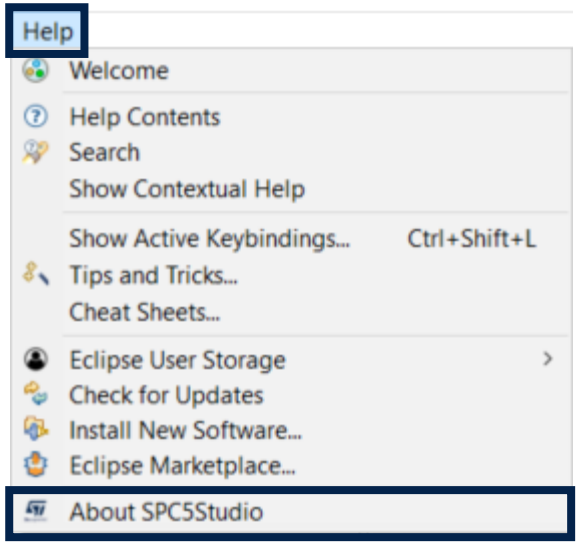
ST website account is needed

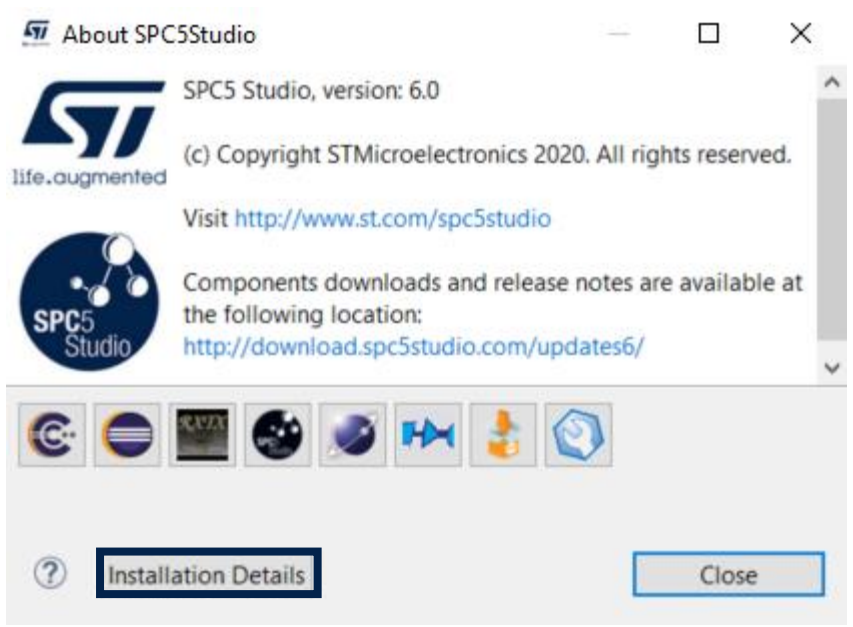
SPC5-STUDIO

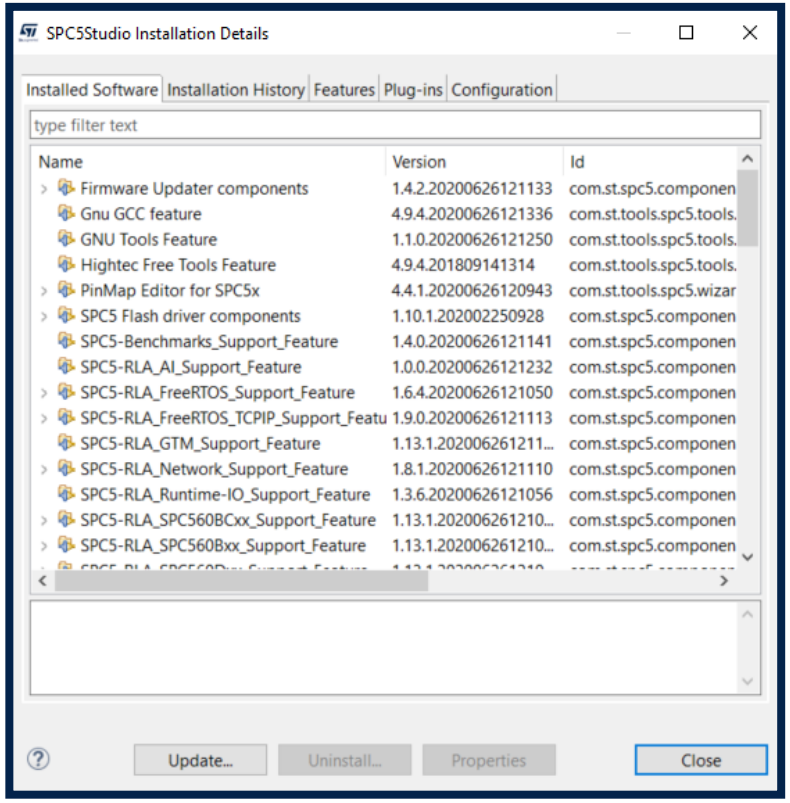

workspace - SPC5Studio
File Edit Navigate Search Project Run Window Help
Menu & shortcuts
Project Explorer
There are no projects in your workspace.
To add a project:
Create a new Makefile project in a directory containing existing code
Create a new C++ project
Create a new C project
Create a new C or C++ project
SPC5 C/C++ Application
Create a project...
Import projects...
Project Explorer
Release Notes.txt
*** SPC5Studio 6.0.0 ***
Components downloads and release notes are available at the following location:
http://download.spc5studio.com/updates6
Enjoy SPC5Studio,
The SPC5Studio Team.
Source code & LLD configuration
Common tasks
Starter actions
How to start with SPC5Studio
Create new SPC5 application
Import samples from application library
Available editors
Here are the available editors on the selected application
Code centric actions
Actions to handle code generation, build and debug
Generate application code, overwriting all previous content.
Compile your application.
Execute and debug your application.
Clean generated files.
Outline
There is no active editor that provides an outline.
Outline
Console
Properties
Problems
Tasks
SPC5 Console
Console area

SPC5-STUDIO

- Studio & plugin version

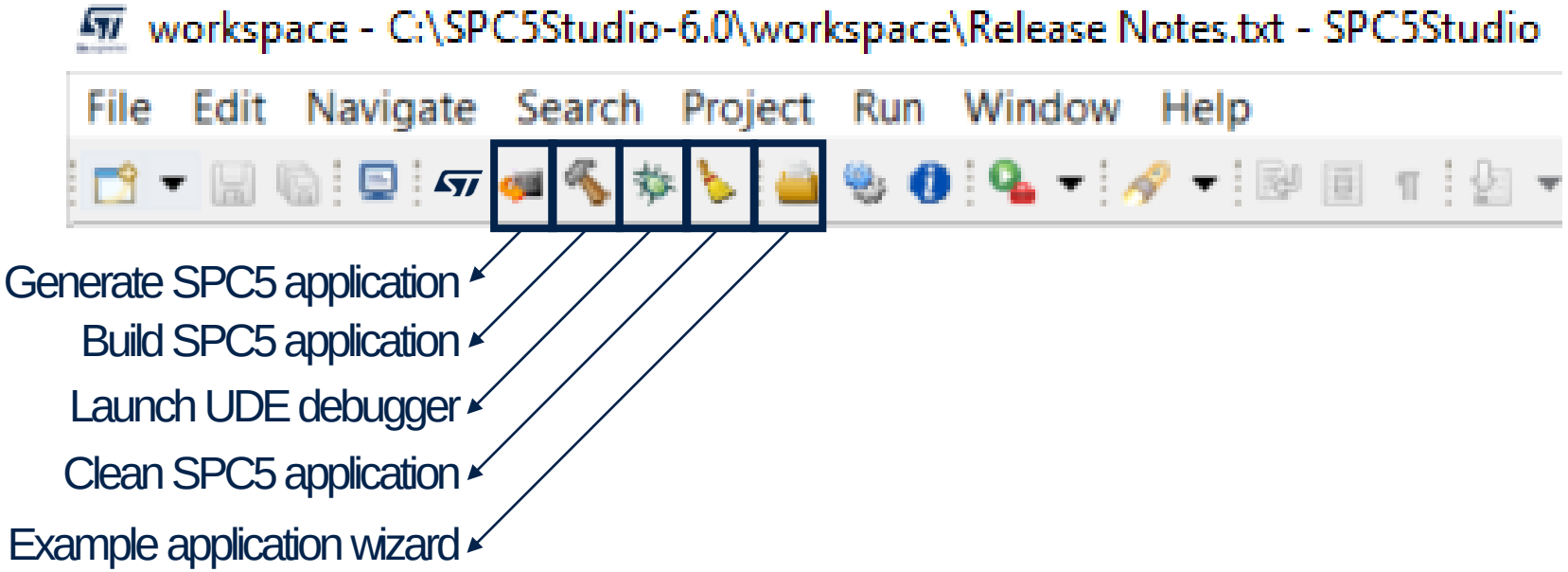






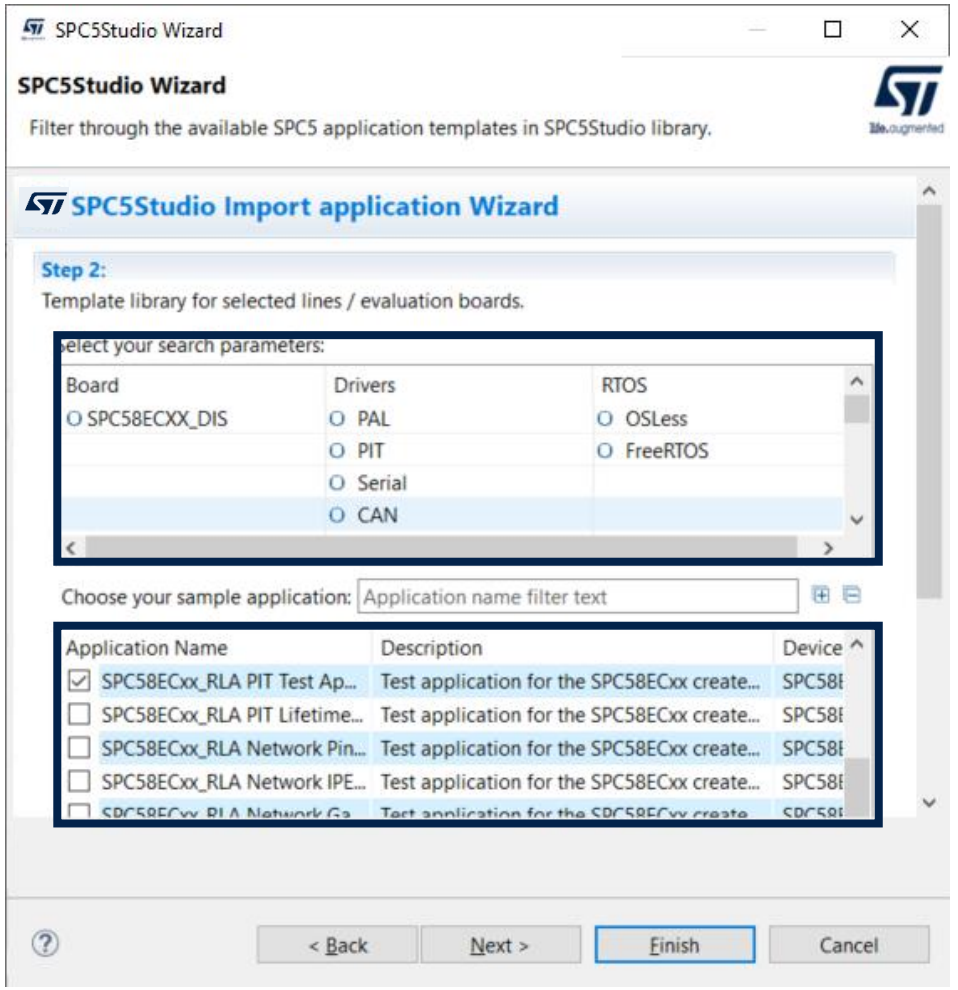
SPC5-STUDIO

- Short cut icons



Example code wizard

- User-friendly wizard



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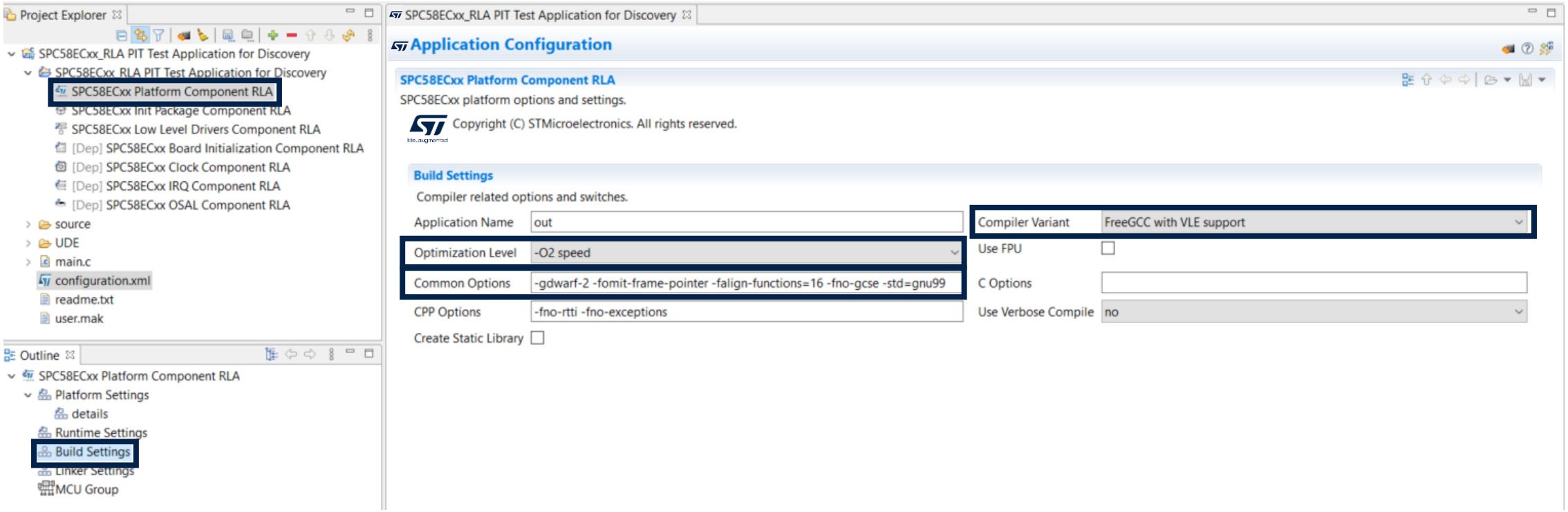
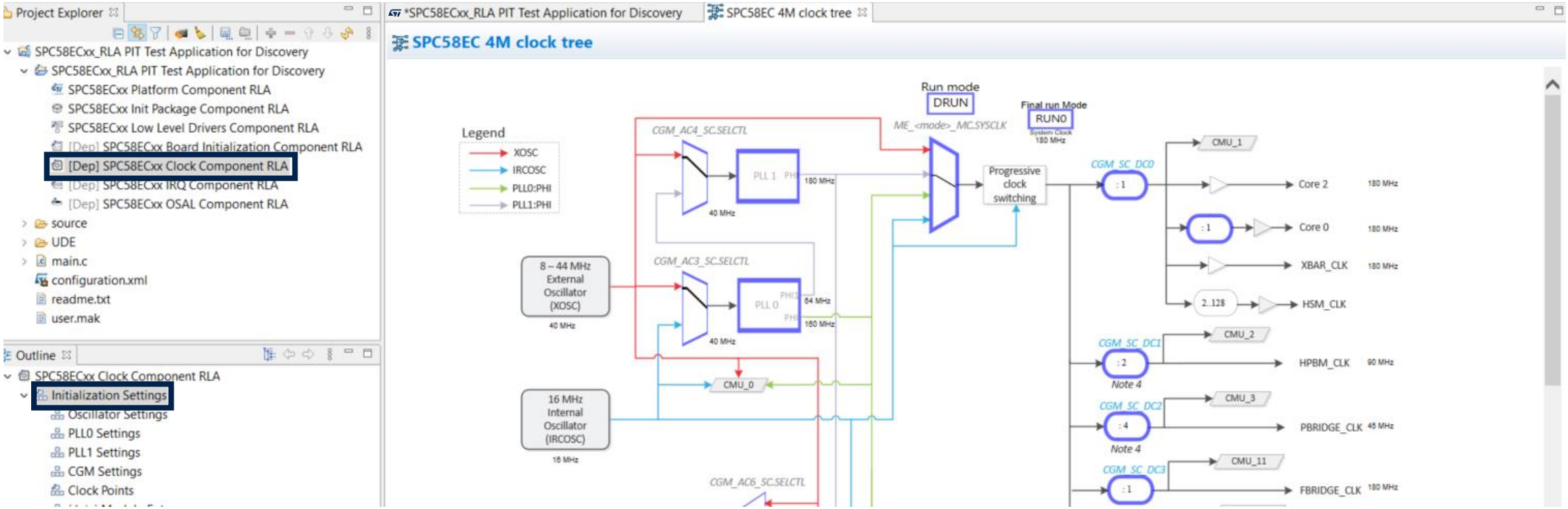
Platform component

- Build Settings



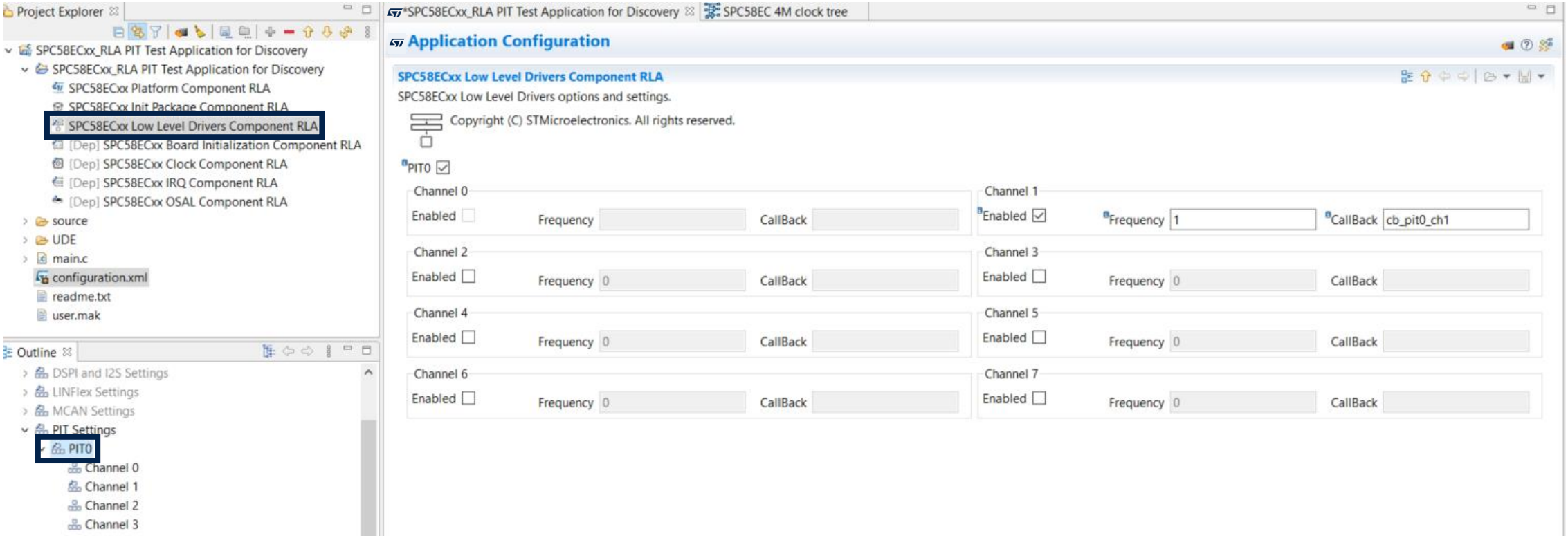
Clock component

- Clock Settings



LLD component

- LLD Settings



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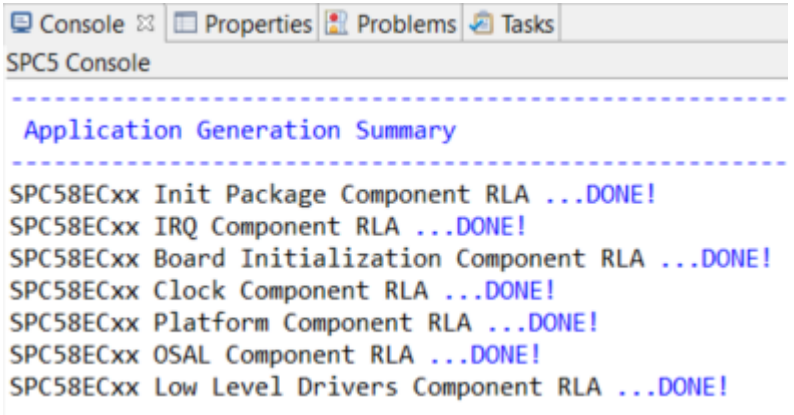
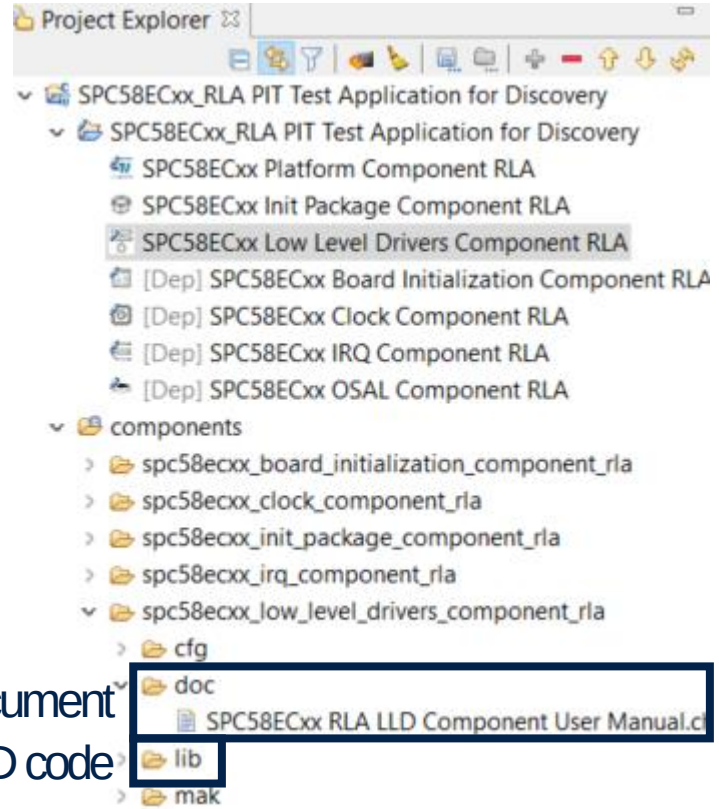
Generate

- Generate
  - After generate, LLD driver code will be present





Help document

LLD code

Build

- Build
  - After build, bin / hex / elf / map will be present

```
Console  Properties  Problems  Tasks
CDT Build Console [SPC58ECxx_RLA PIT Test Application for Discovery]
Compiling eirq.c
Compiling pit_lld_cfg.c
Compiling osal.c
Compiling systimer.c
Compiling board.c
Compiling irq_cfg.c
Compiling eirq_cfg.c
Compiling main.c
Compiling components.c
Linking build/out.elf
Creating build/out.mot
Creating build/out.bin
Creating build/out.dmp
Creating build/out.hex

   text    data     bss     dec     hex filename
  17970     120    4376   22466    57c2 build/out.elf

Done

13:09:14 Build Finished. 0 errors, 0 warnings. (took 1
```

6.0 › workspace › SPC58ECxx_RLA PIT Test Application for Discovery › build

Name	Date modified	Type
lst	8/21/2020 1:08 PM	File folder
mcs	8/21/2020 1:07 PM	File folder
obj	8/21/2020 1:08 PM	File folder
out.bin	8/21/2020 1:08 PM	BIN File
out.dmp	8/21/2020 1:09 PM	DMP File
out.elf	8/21/2020 1:08 PM	ELF File
out.hex	8/21/2020 1:08 PM	HEX File
out.map	8/21/2020 1:08 PM	MAP File
out.mot	8/21/2020 1:08 PM	MOT File

Flash download / debug

- Depends on your taste

LAUTERBACH DEVELOPMENT TOOLS

pls Development Tools

Green Hills

PE micro

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Background : FOTA

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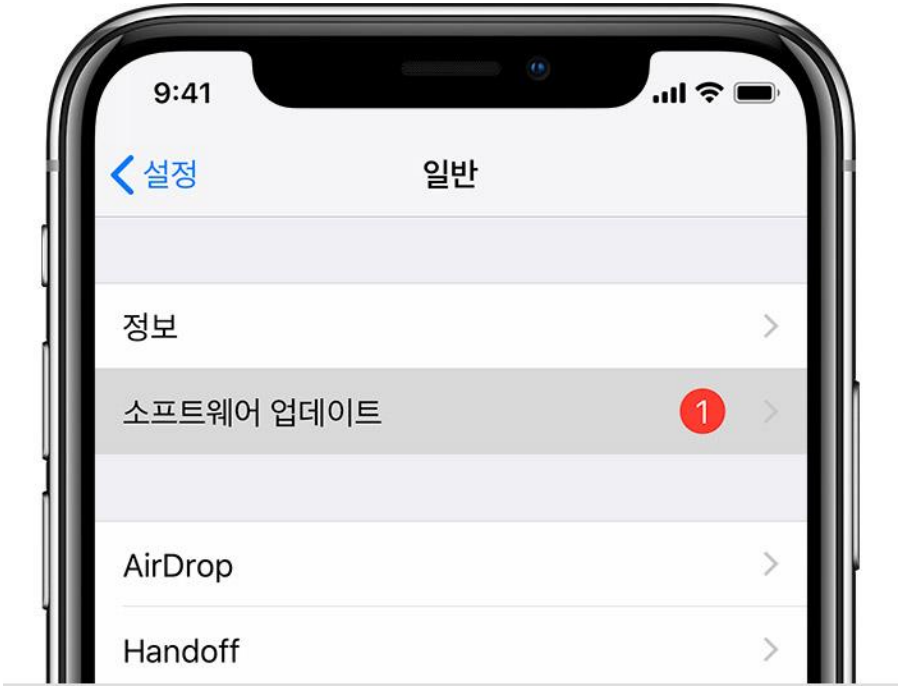
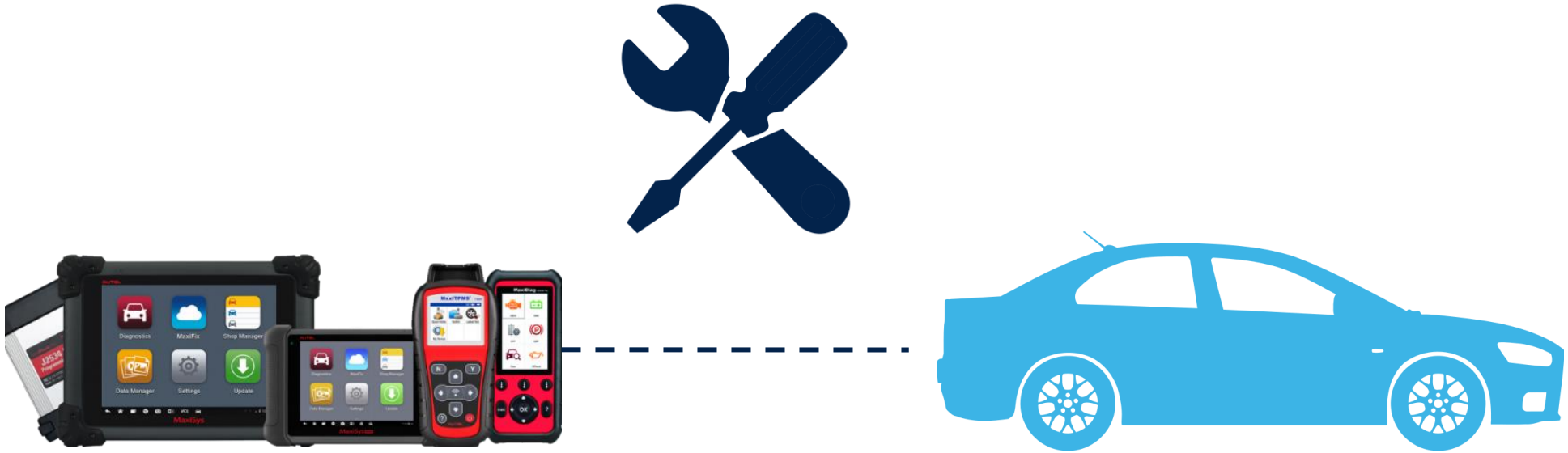
Software updates in consumer electronics

- **OS update for smartphones & set-top boxes (STB)**
  - Remote Software Updates exist for more than 10 years in consumer electronics.
  - Background downloading for new firmware via Wi-Fi / Ethernet



Software updates for cars (classic)

- **Manual Update in car repair shop**
  - Every customer needs to visit a car repair shop to update software via an on-board diagnostics (OBD) tool.

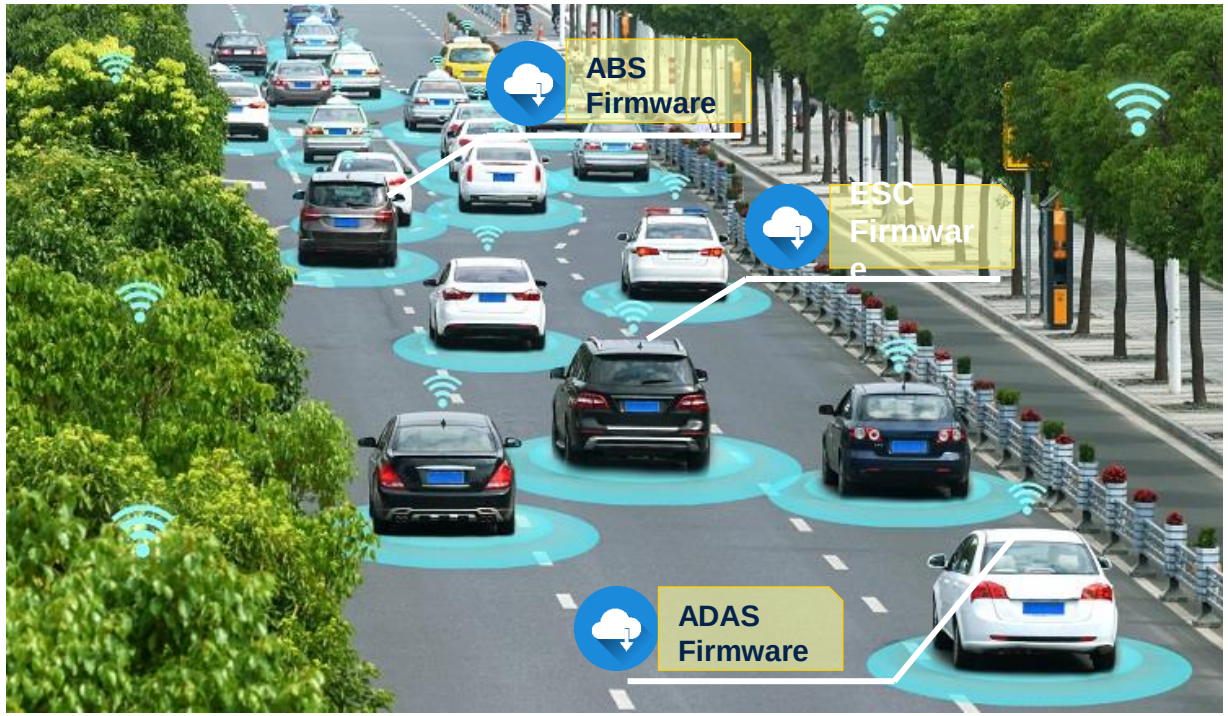


Why FOTA
concepts and basic requirements

- **Why Firmware Over The Air (FOTA) updates?**
  - On an average, an automotive vehicle today has 100 ECUs and over 100 million lines of SW code. By 2020, there are expected to be 300 ECUs in a car.
  - In such a complex automotive electronics and software set-up, the need to remotely manage and update the vehicle ECU software becomes all the more important.
  - A security attack on any Electronic Control Unit (ECU) of a vehicle may prove to be dangerous for the passengers and cause a bad reputation for the automotive OEM.
  - To avoid such a crisis, Firmware Over The Air (FOTA) updates have been identified as a robust, reliable and cost-effective method for remotely managing the software updates of connected car systems.

Benefits of FOTA
Concepts and basic requirements

- Firmware-over-the-air (FOTA) services enable firmware downloads and updates for any of the specific electronic control units (ECUs) inside a car.
- Cost-efficient and better managed firmware updates
- Upgrade the firmware safely, anytime & anywhere
- Lowers the time to market



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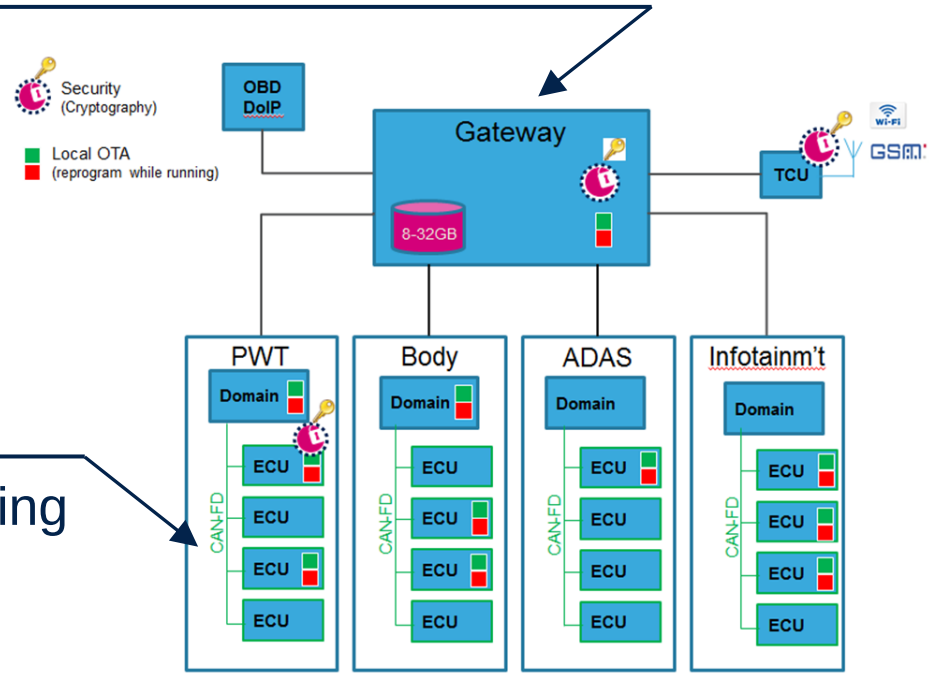
FOTA Requirements Application Scheme

- **Central OTA management application, like gateway and/or storage**
  - Flash context management by HW
  - Interface for external memory
  - Ultra-fast communication interface
  - Advanced security features

- **Local OTA available application**
  - Flash erasing/program while application is running
  - Security features (authentication, cryptography)
  - Fast communication interface



SPC5 Chorus family fully supports both kinds of applications

AFLS + FOTA Demo

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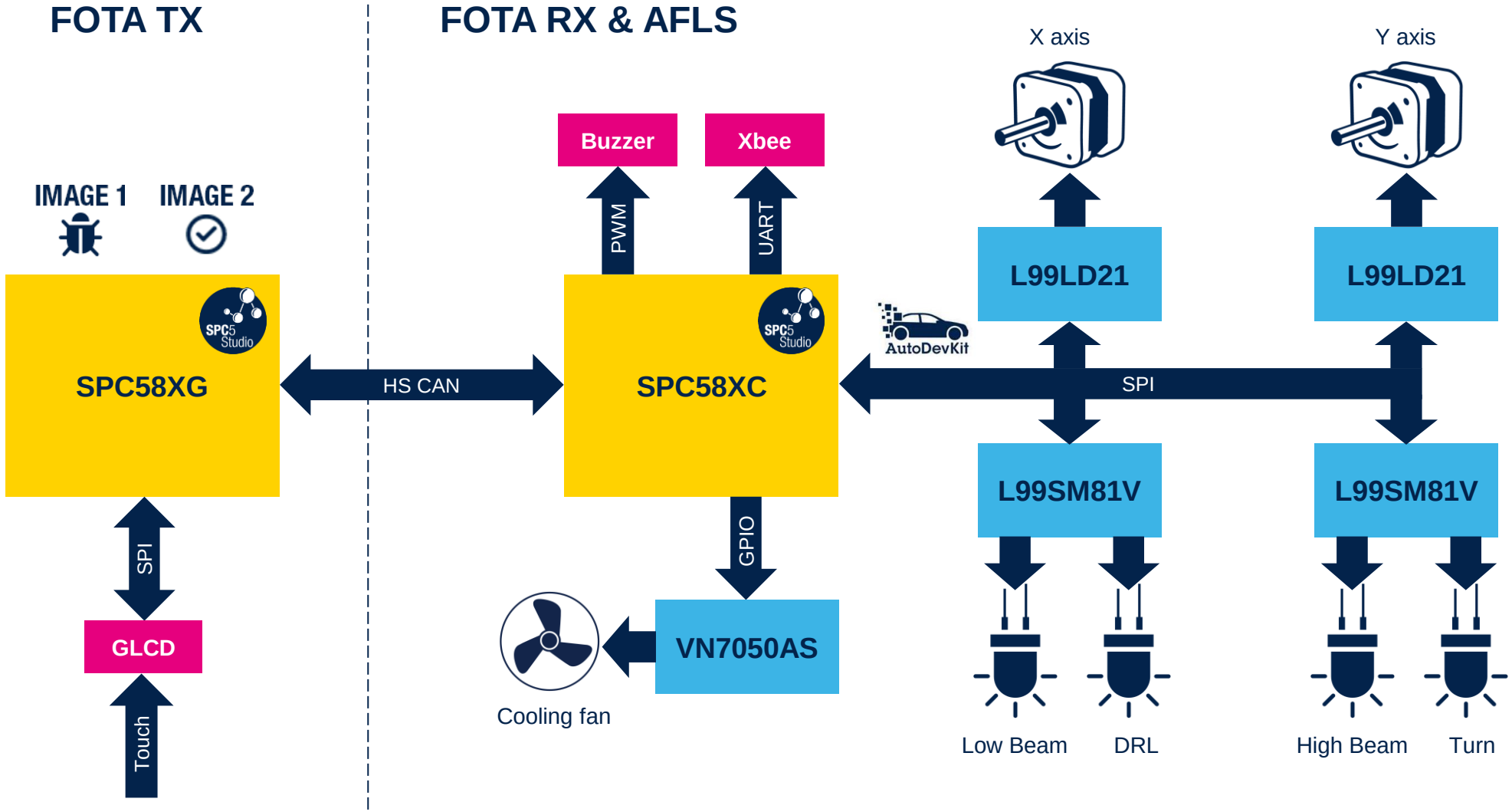
Introduction

- This demo shows FOTA[1)] functionality during AFLS[2)] application running.
- User can see the demo progress through LED front lamp, stepper motor, cooling fan, GLCD, serial log and buzzer.
- Key ST product
  - L99LD21 : LED driver
  - VN7050AS : IPS
  - L99SM81 : Motor driver
  - SPC58XC : Chorus 4M MCU
  - SPC58XG : Chorus 6M MCU

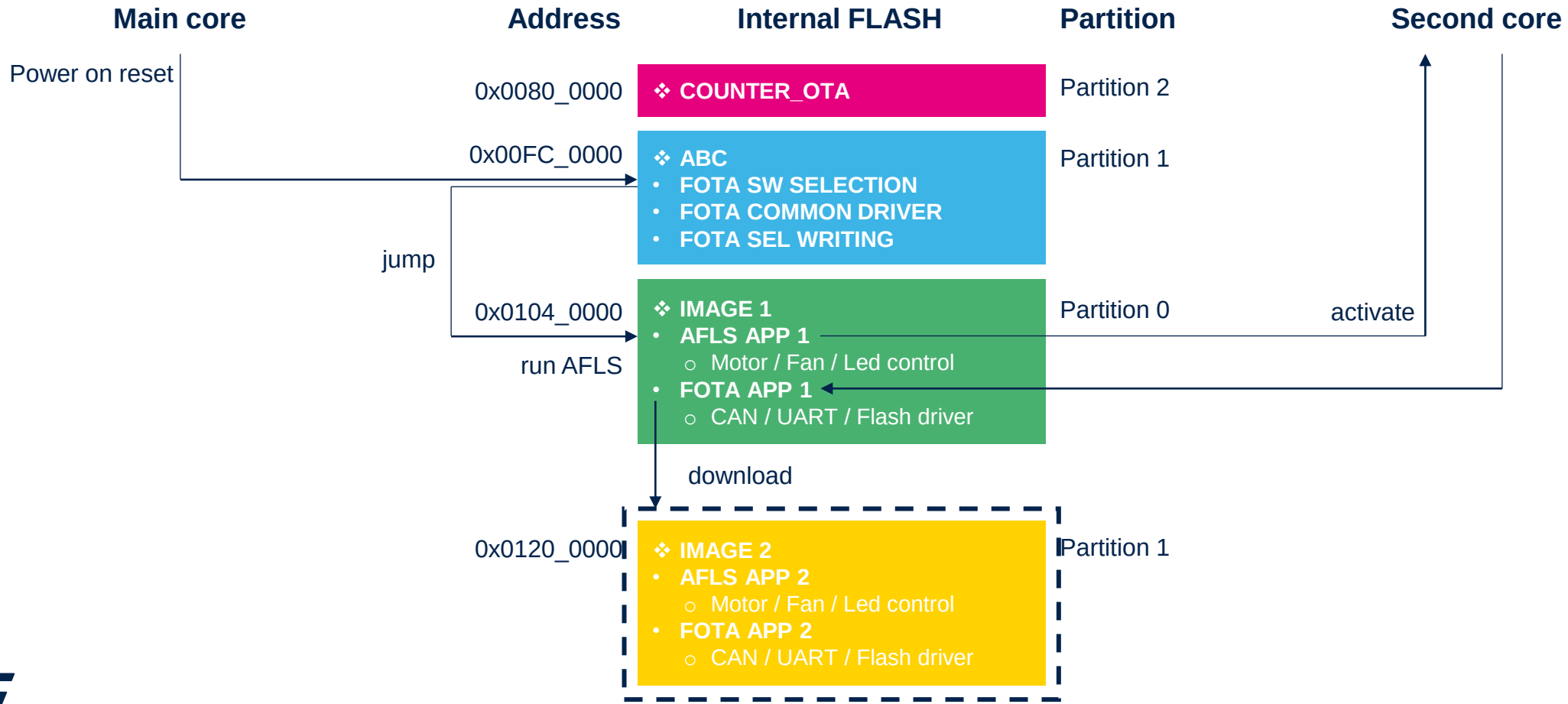
1) Firmware Over The Air
2) Adaptive Front Lamp System

Block diagram (HW)



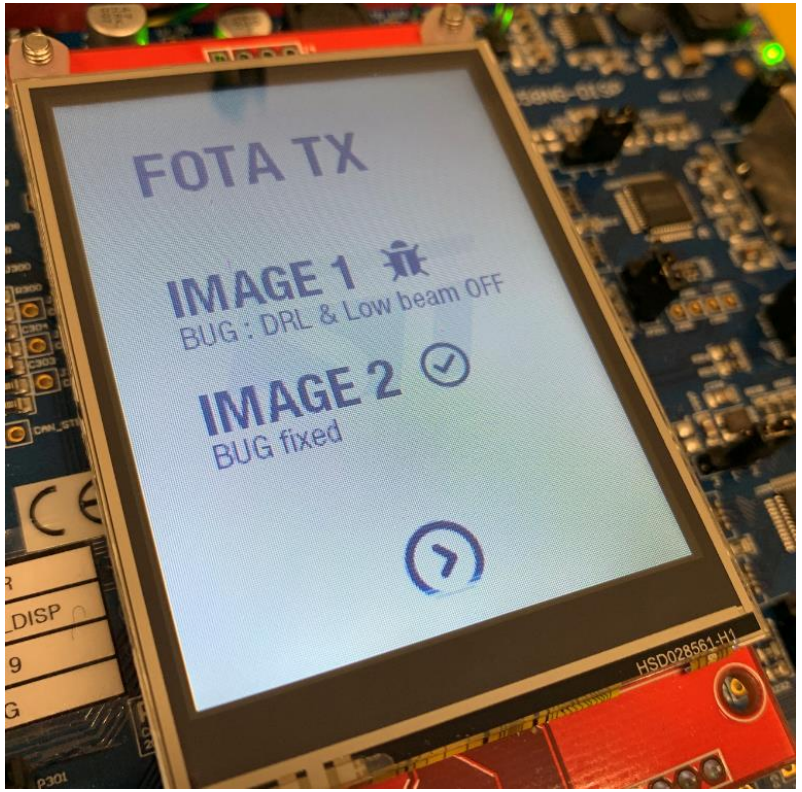
Block diagram (SW)

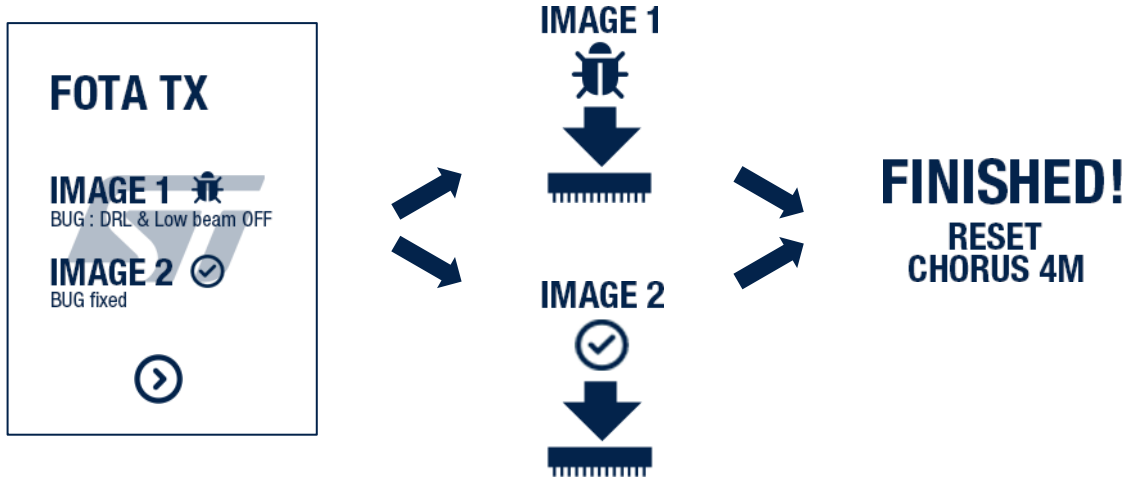
- How it works?



Appearance

- **GLCD**





Appearance

- **Serial Log**

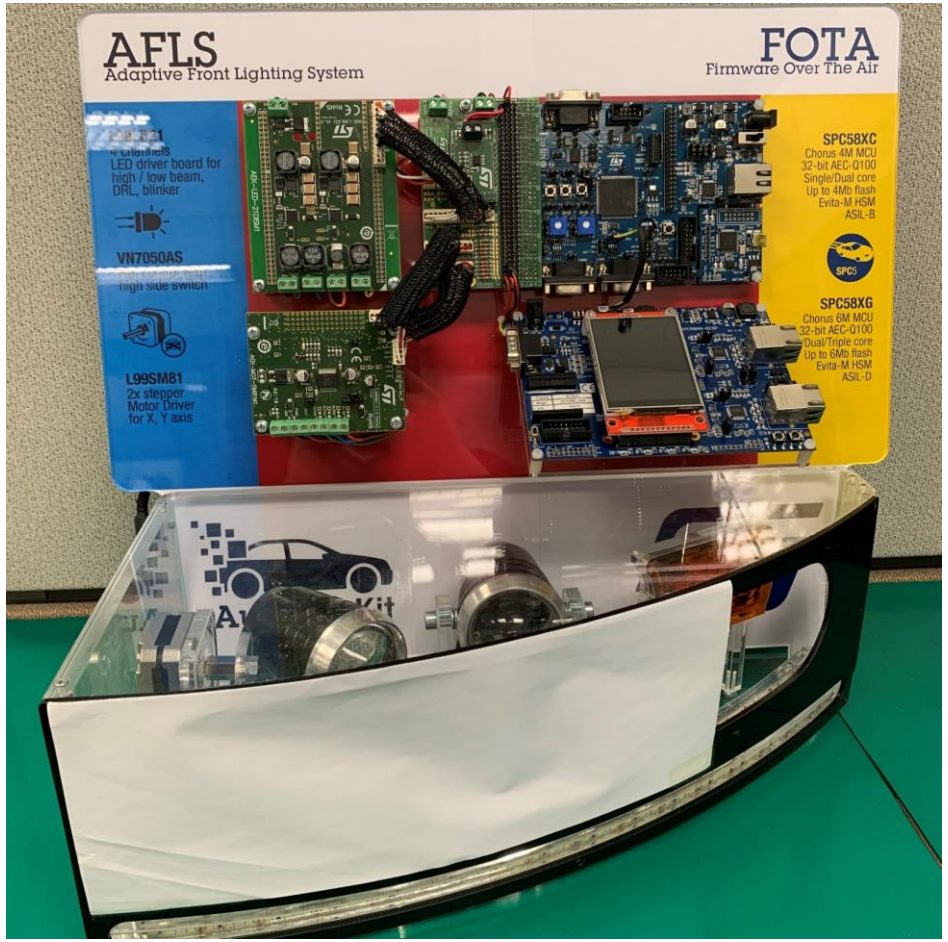
Console log

```
================================================
                STMicroelectronics
                    ADG KOREA
================================================
                    AFLS + FOTA
           Adaptive Front Lighting System
                Firmware Over The Air
================================================
# DEMO information
  FOTA TX : Chorus6M (SPC58XG)
  FOTA RX : Chorus4M (SPC58XC)
  COMM. : HS CAN (250Kbps)
================================================
# Log from FOTA RX
  AFLS : AFLS core ACTIVATED...
  AFLS : Boot loader executing...
  AFLS : OTA counter reading...
  AFLS : Code jump area -> [IMAGE 1]
  AFLS : IMAGE 1 executing...
  AFLS : AFLS Initializing...
  AFLS : FOTA core ACTIVATED...
  AFLS : IMAGE 1 running !
  FOTA RX : Ready to receive IMAGE 2...
```

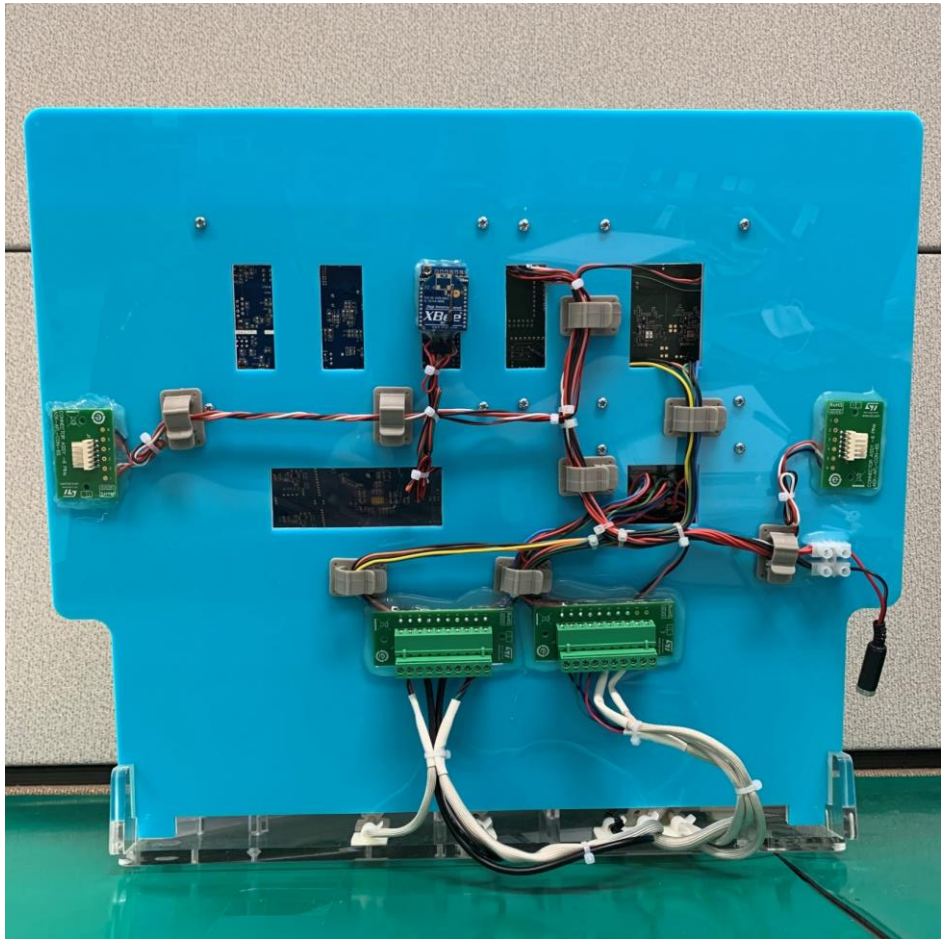
Console log

```
# Log from FOTA RX
  AFLS : AFLS core ACTIVATED...
  AFLS : Boot loader executing...
  AFLS : OTA counter reading...
  AFLS : Code jump area -> [IMAGE 2]
  AFLS : IMAGE 2 executing...
  AFLS : AFLS Initializing...
  AFLS : FOTA core ACTIVATED...
  AFLS : IMAGE 2 running !
  FOTA RX : Ready to receive IMAGE 1...
  FOTA RX : IMAGE 1 downloading...
  FOTA RX : IMAGE 1 download complete!
  FOTA RX : Next Code jump area -> [IMAGE 1]
================================================
                    DEMO END
                RESET Chorus 4M
================================================
```

Appearance

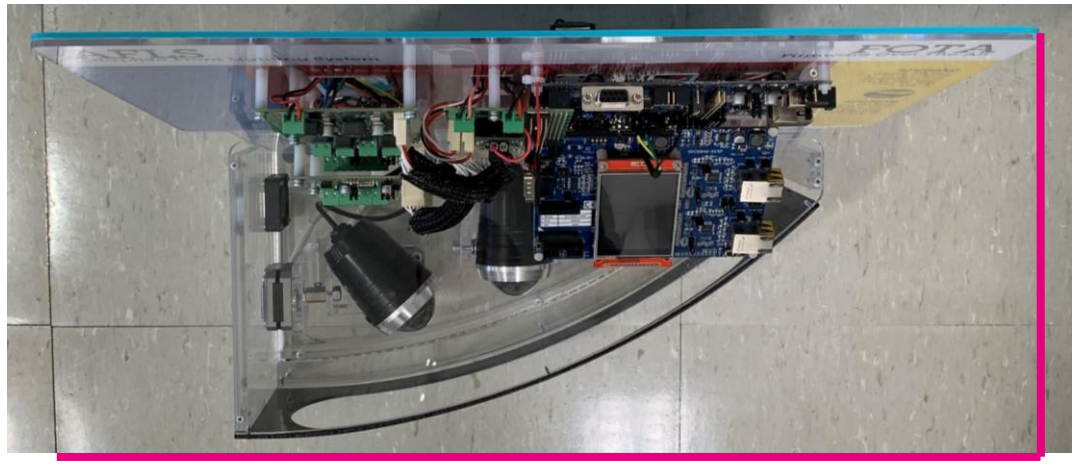


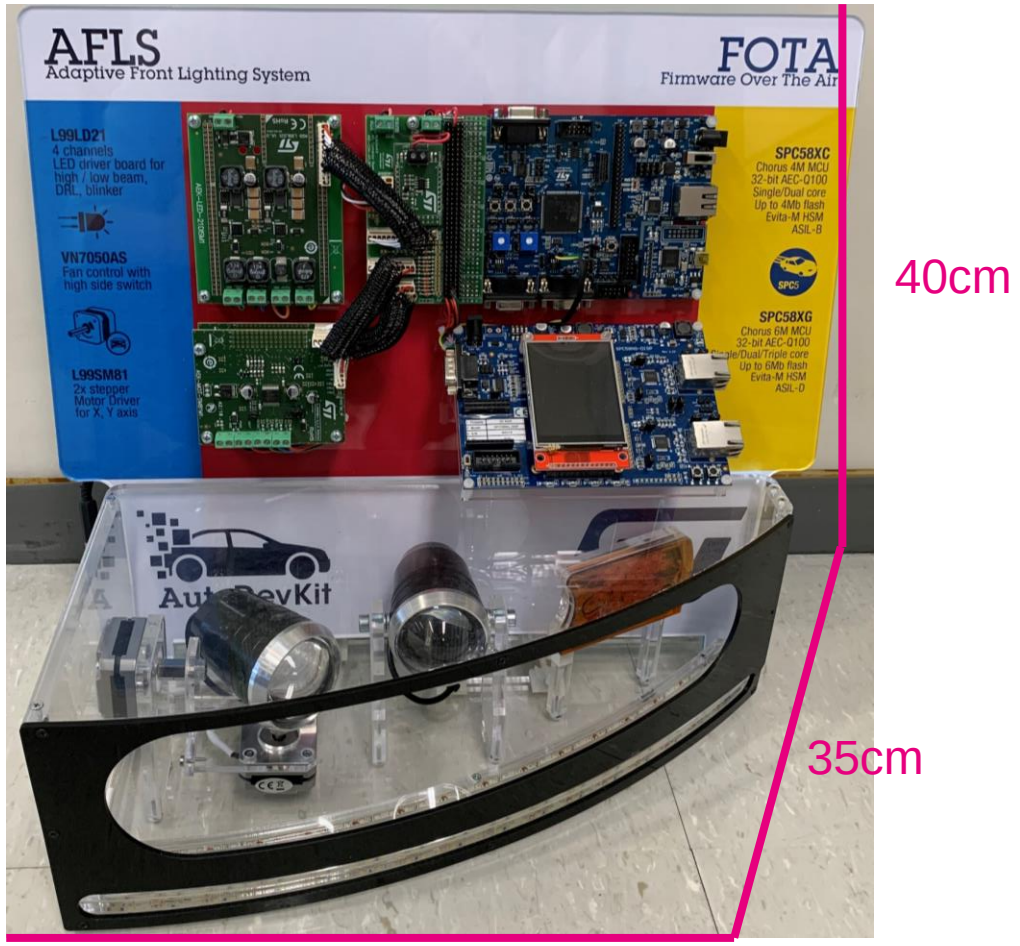
Front



Back

Appearance


35cm
50cm

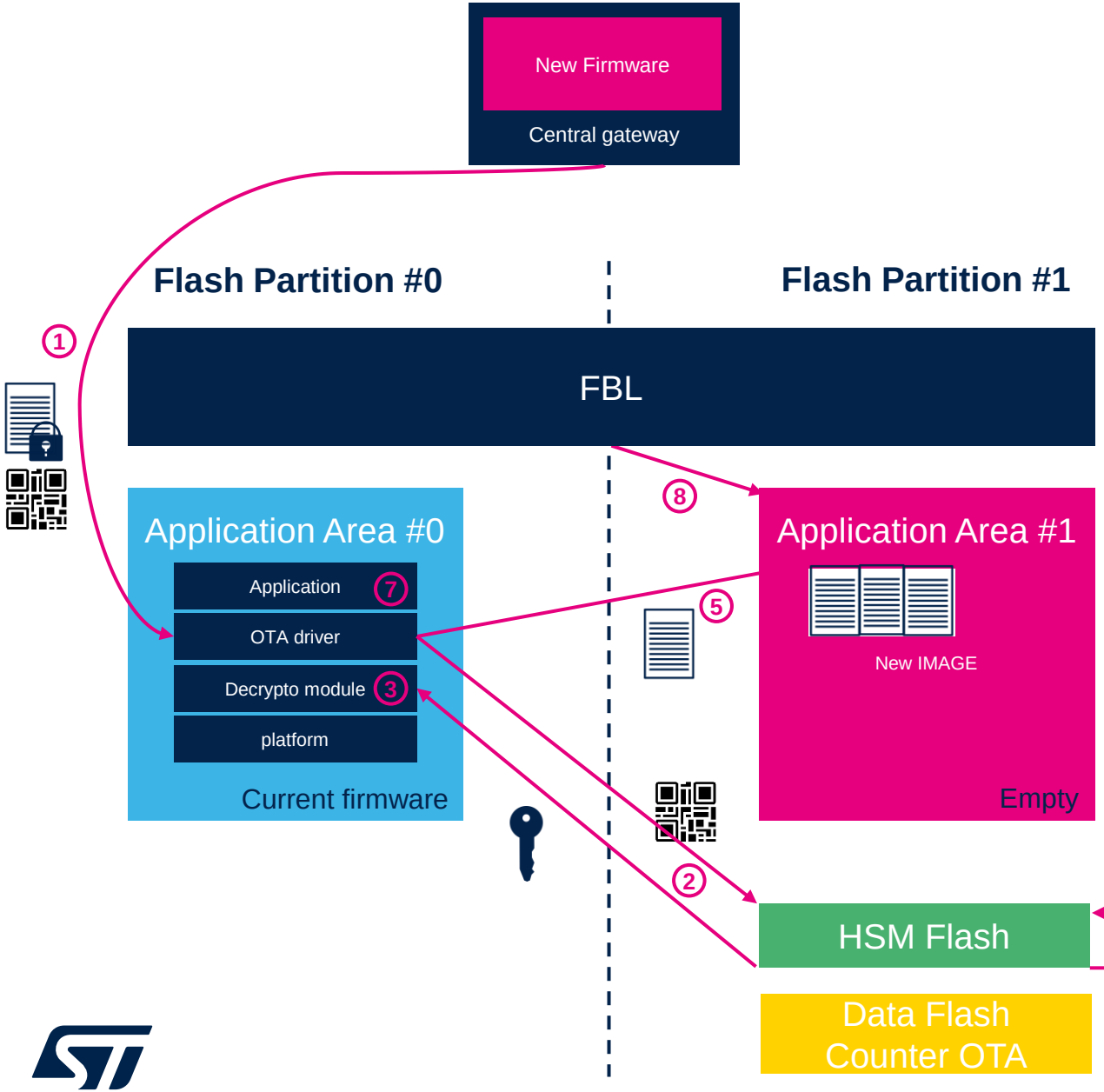

AFLS
Adaptive Front Lighting System
FOTA
Firmware Over The Air
L99LD21
4 channels
LED driver board for
high / low beam,
DRL, blinker
VN7050AS
Fan control with
high side switch
L99SM81
2x stepper
Motor Driver
for X, Y axis
SPC58XC
Chorus 4M MCU
32-bit AEC-Q100
Single/Dual core
Up to 4Mb flash
Evita-M HSM
ASIL-B
SPC58XG
Chorus 6M MCU
32-bit AEC-Q100
Up to 6Mb flash
Evita-M HSM
ASIL-D
40cm
35cm
50cm

DEMO

- Demo video

TO BE UPDATED

Chorus 4M OTA scenario
Single core



1. Receiving encrypted data via Lowest priority task (High speed CAN / Ethernet) during Application running
2. HSM extracts crypto key from received data and pass to decrypto module.
3. Data decryption will be done by decrypto module(Host core) with crypto key.
4. HSM jumps to RAM to suspend. (Suspend API)
5. Background task does flash write to empty area with update segment size.
6. HSM jumps back to flash to resume. (Resume API)
7. Back to application after update segment download. Repeat 1 ~ 6 until finishing update about New IMAGE.
8. FBL determine Application Area #X where to jump at next MCU reset.

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Thank you

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