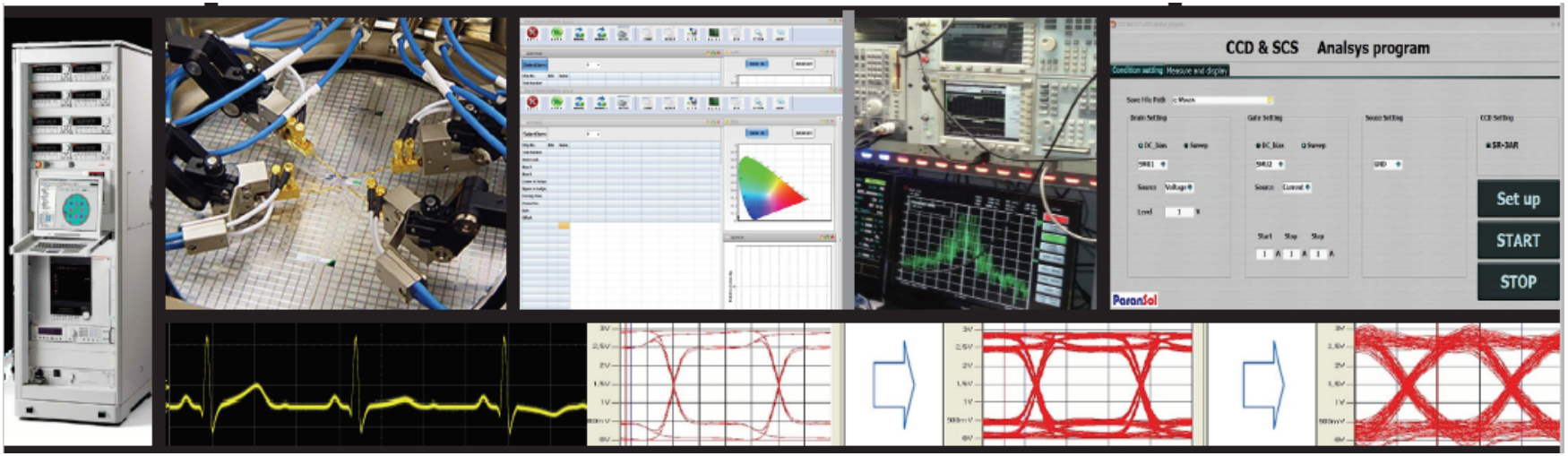
100BASE-T1 Automotive Ethernet
I3C 프로토콜 어날라이저/엑서사이저

(주)탐시스텍



Agenda

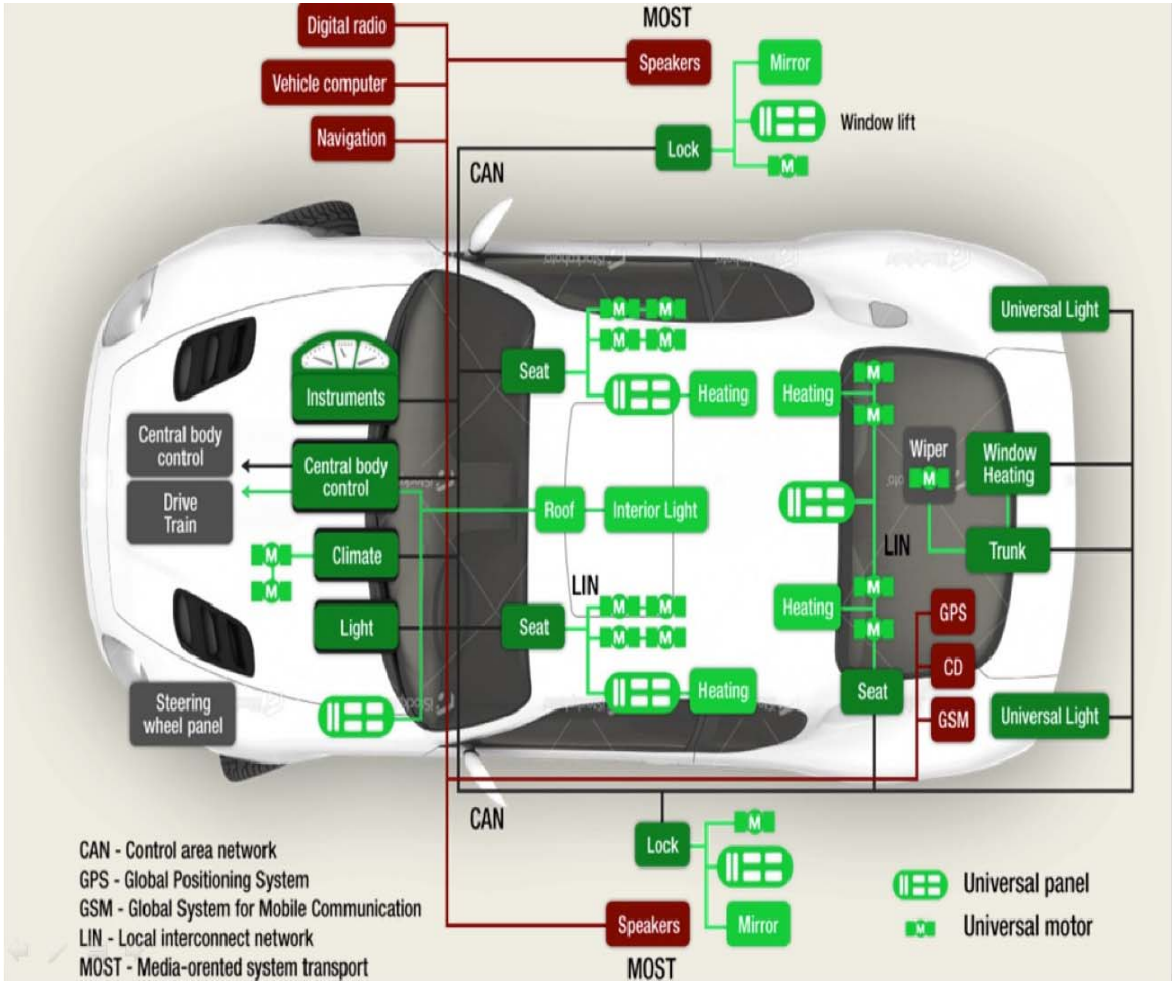
- About Prodigy Technovations
- Trends & Overview of Automotive In-vehicle Bus Network
- Automotive Ethernet Industry Needs
- Introduction to **PGY-100BASET1-PA**
- Demo of PGY-100BASET1-PA
- Overview of I3C interface
- Introduction to **PGY-I3C-EX-PD**
- Demo of PGY-I3C-EX-PD

Prodigy Technovations

- Founded in 2009 with software application for Tektronix Oscilloscope
- Hardware based Protocol Analyzer launched in 2015
- Protocol Analyzer
  - eMMC, SD, SDIO
  - UFS3.1
  - 100BaseT1 Automotive Ethernet
  - I3C, RFFE, SPMI Exerciser and Protocol Analyser
  - 10 Channel Logic Analyser with 1GS/Sec, I2C, SPI and UART Trigger and decode
  - I2C, SM Bus, SPI Exerciser and Protocol Analyzer
- Tektronix Oscilloscope based Electrical Validation and Protocol decode Software
  - I2C, SPI, UART, eMMC, SD, SDIO, QSPI, I3C, SPMI, RFFE, UFS, UniPRO, HDMI, MHL, USB2.0/3.0, 3.1Gen2, I2S, SVID, JTAG,

Mainstream Automotive In-Vehicle Networking

- Electronic Control Units (ECUs) are Embedded System devices which control and monitor cars
- ECUs are interconnected using LIN, CAN, CAN FD, FlexRay and MOST Interface
- Modern Car has 75+ ECU.

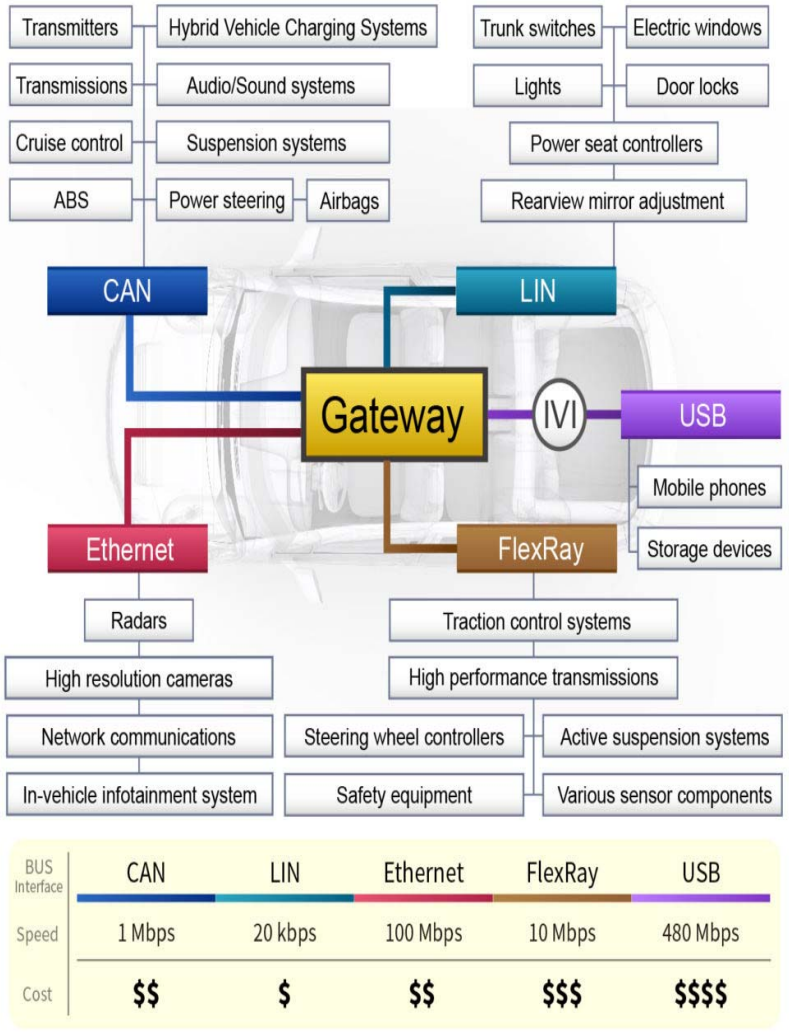


Current In-Vehicle Network Bus

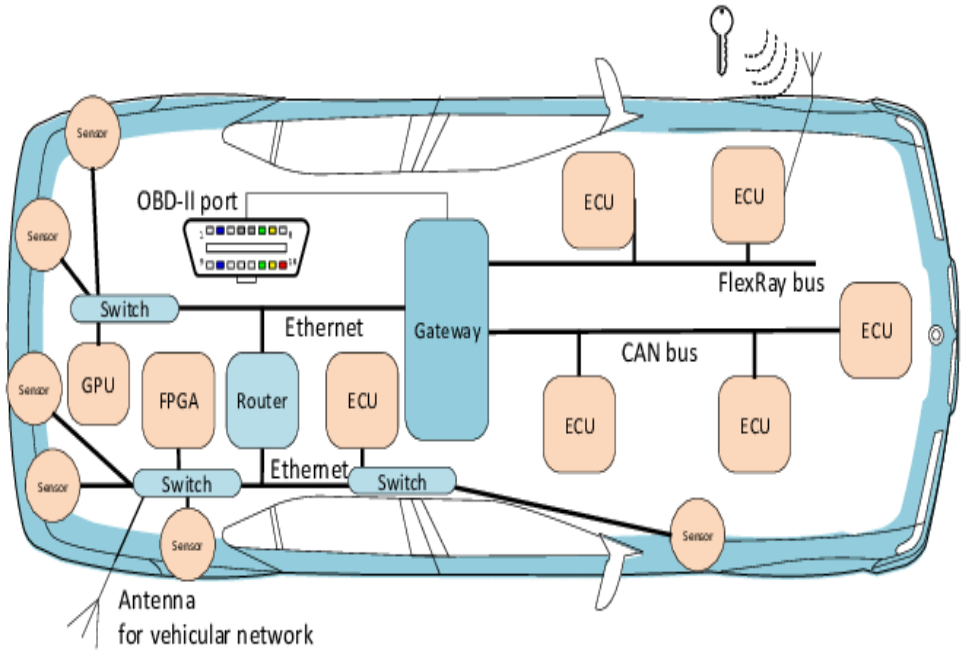
- Local Interconnect Network (LIN) Bus
  - Low cost , Low speed 19.2 Kbps ,Single Copper Cable , Easy to implement
- Controller Area Network (CAN) Bus
  - The most dominant ,most common and popular vehicle network
  - Many variants for different speed, Max Speed 15 Mbps
  - Single Twisted Pair cable , Its plug and play.
- FlexRay Bus
  - Safety and time critical Network. 10Mbps with Redundancy built in.
- Media Oriented Systems Transport (MOST) Bus
  - Originally designed for Infotainment System with data speed of 25, 50, 150 Mbps
  - Ring Topology

Emerging In-Vehicle Network Bus

- Adoption of Industrial and consumer Ethernet interfaces in Automotive in-vehicle bus
  - Ethernet & USB
  - Gateways
- New Applications are adapted using Ethernet protocol and USB
  - Radars, High Res Cameras
- MOST Bus application for Infotainment is replaced by Ethernet



Future In-Vehicle Network Bus



- Consolidation of In-vehicle bus by Ethernet, CAN and FlexRay Bus
- High Performance computing in-vehicle
- Connected Car

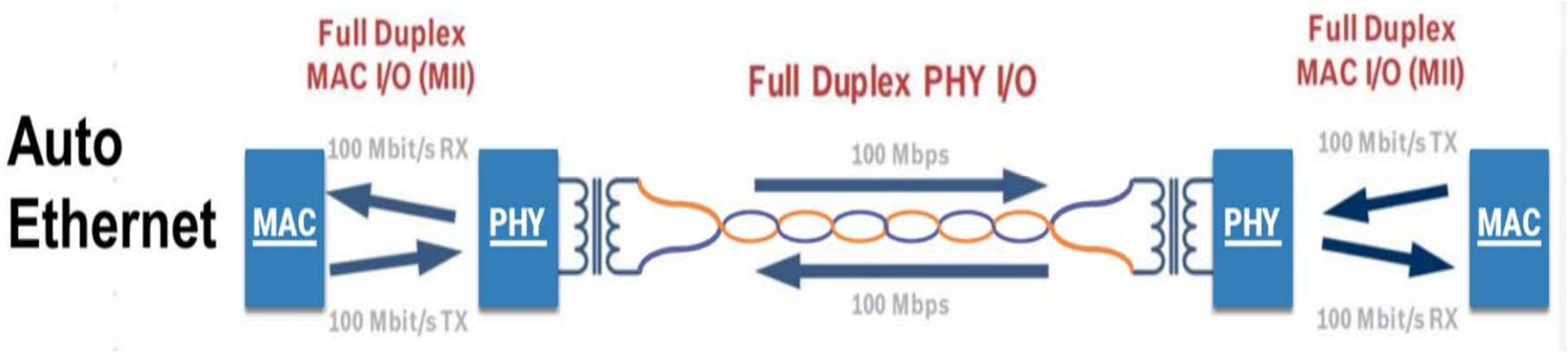
Automotive Industry Needs and challenges

- Increased use of in-vehicle electronics
  - More and more applications like autonomous car becoming bandwidth hungry
- Growing in volume and complex
  - Substantial increase of Cameras, Diagnostic features, ADAS and Infotainment
  - Display consoles evolving computerized centres
- Bandwidth Challenges
  - More data requires higher transmission rates

Automotive Industry Needs and challenges

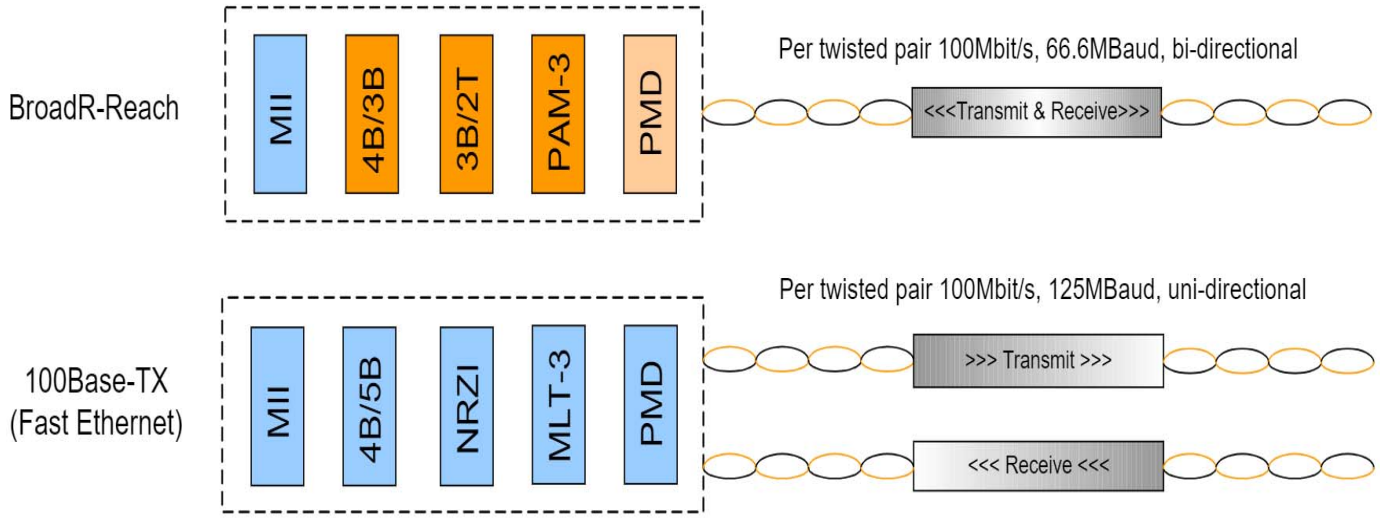
- Cable limitations
  - Automakers seeking less costly forms of wiring
- Reliability, extreme operating temperature and least power consumption
- Compatibility and need for open architecture
  - In-vehicles network must be scalable, support multiple systems and devices
  - Time to market
- Automotive Industry standards
  - Stringent regulations requirements

100BASE-T1 PHY layer



- MAC layer and above protocol layer is as per 802.3 standards document
- MAC to PHY layer interface is RGMII/SGMII

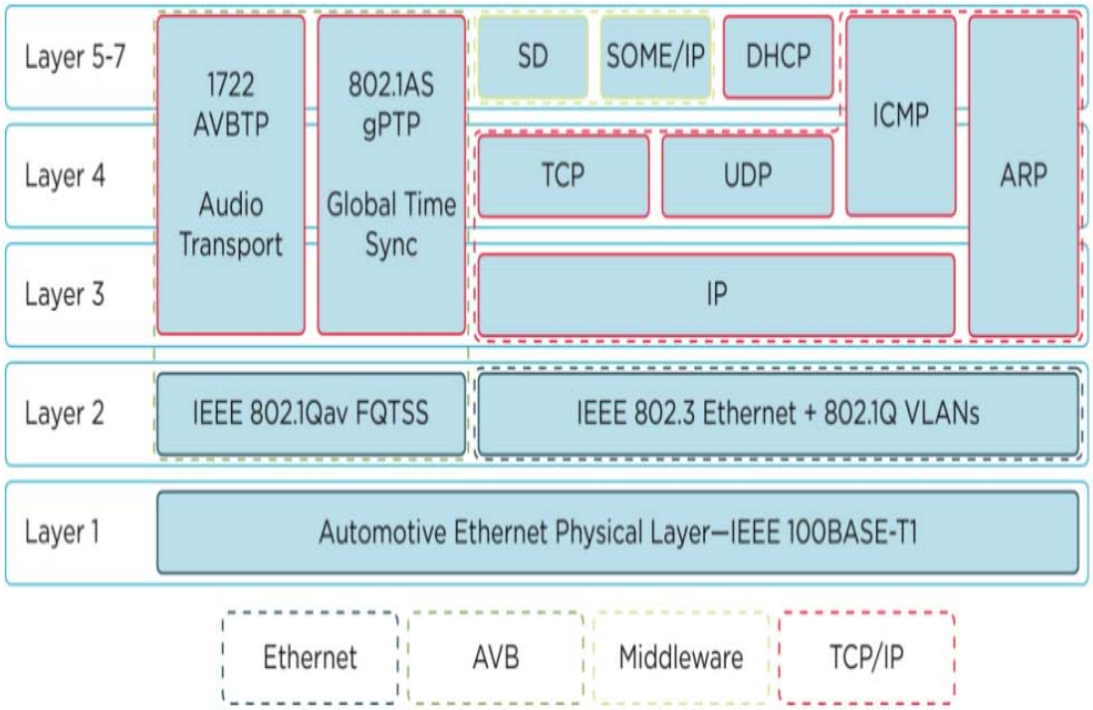
Automotive vs. Standard Ethernet



- Standard Ethernet has two wire transmit and Receive
  - Unidirectional, 100 mtr length cable, Unspecified EMC, Plug and play

- 100BASE-T1 has one pair twisted pair cable with full duplex
  - Bi-directional, 15 mtr cable length, Stringent EMC requirements

OSI layers of 100BASE-T1



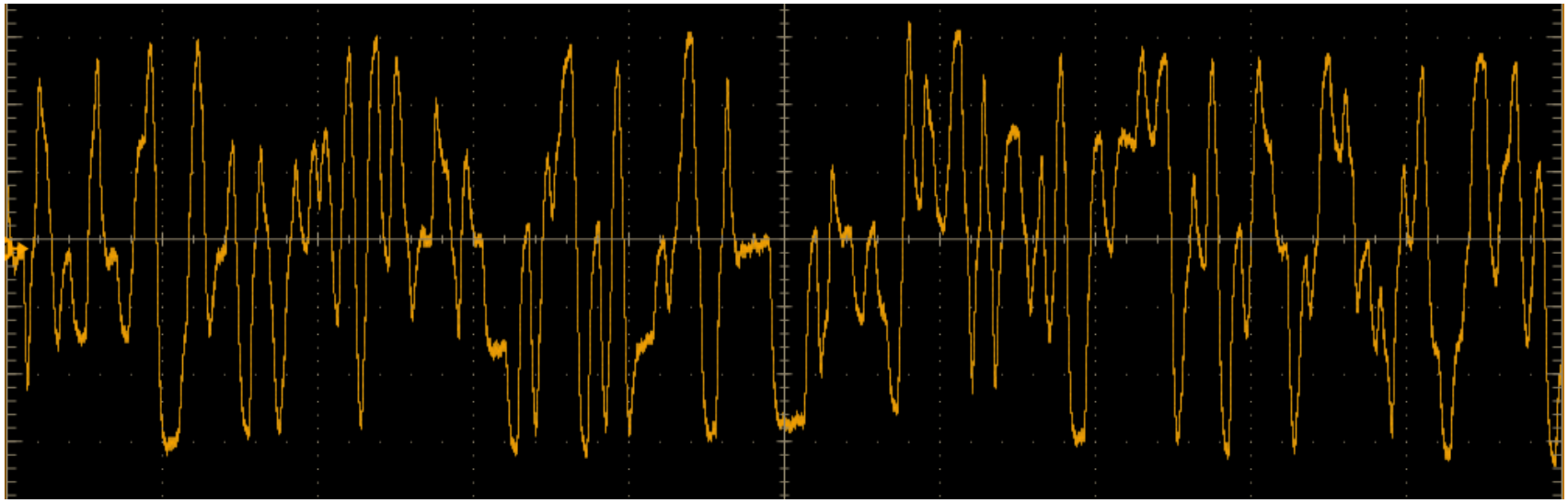
- 100BASE-T1 is supports all these protocols.
- Based on customer application, customers are expected to implement different protocol stack

Automotive Ethernet Protocol Analysis challenges

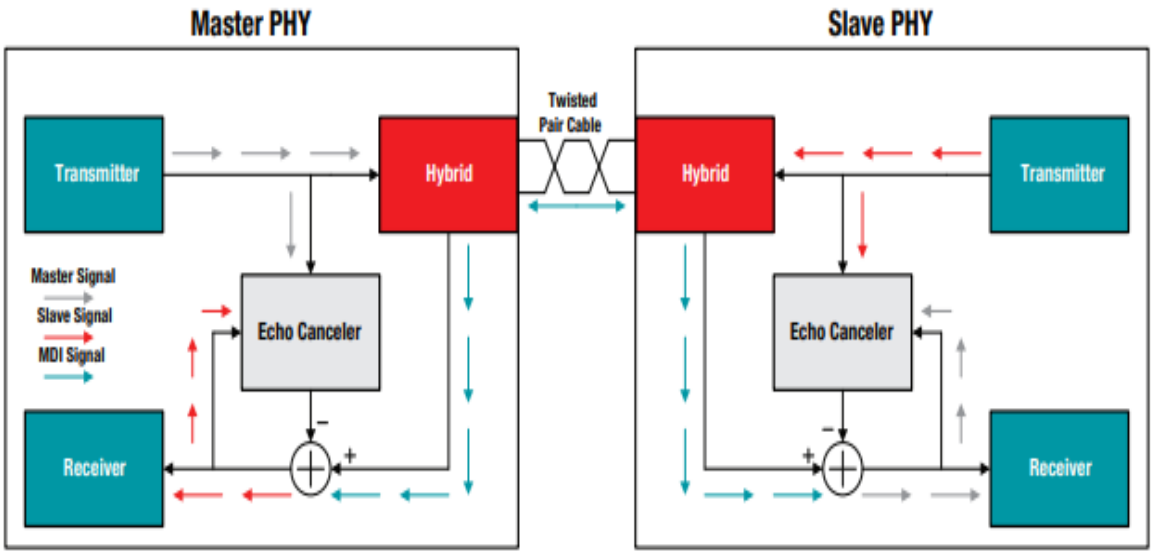
- Need to analyse the timing of protocol activity with real-world data
- Correlate Automotive Ethernet Protocol and Control Signals such as MDC and MDIO activity
- In low latency network, capture specific Protocol events without going through all protocol data
- Analyse the Protocol Activity over long period of time
- It is extremely difficult to extract Master and Slave signals from superimposed full duplex PAM3 signals
- Initialization of protocol activity between master and Slave demands frequency and phase synchronization for eco cancellation
  - Active tapping the signal can impair the line training between Master and Slave

100BASE-T1 Physical Layer Signalling

- Full duplex Signals
  - Full duplex signalling is achieved on the principles of superimposition of Master and Slave signals
  - Signals from Master and Slave are crossing each other and difficult to analyse without separating them using intelligent device

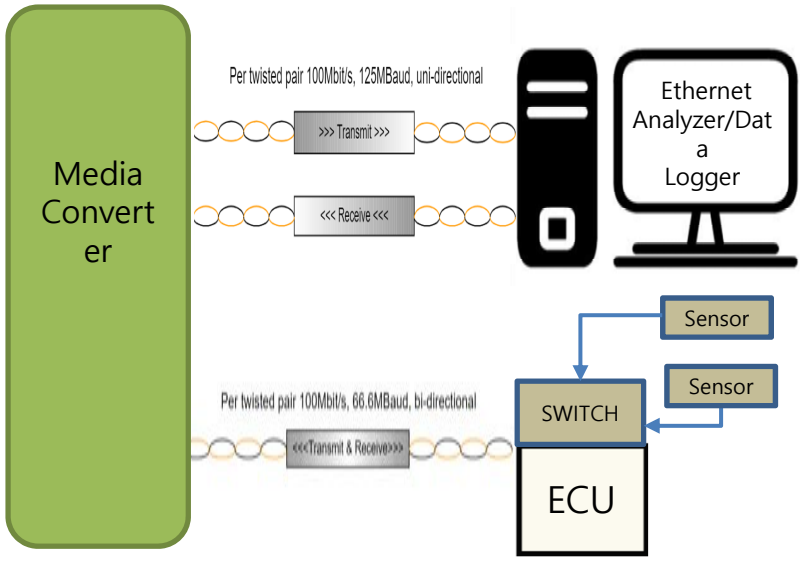


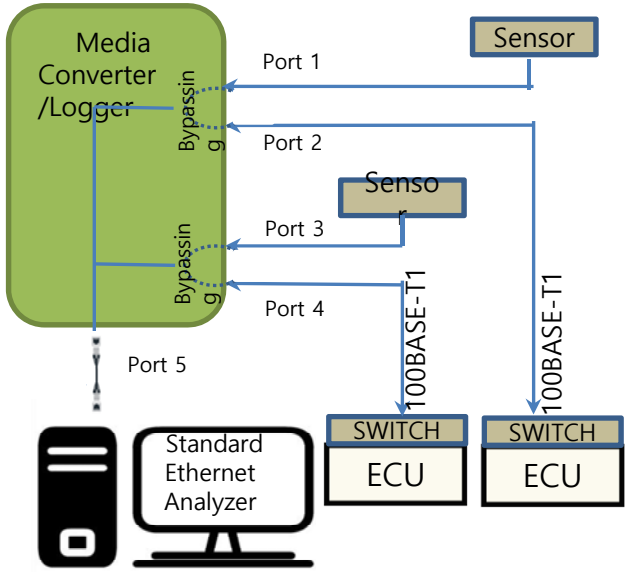
Signal Separation 100BaseT1 PHY



- Dedicated PHY chip for master and Slave
- Use echo cancellation to remove their own signals and extract received signal
- Two PHY link training to transmit at same frequency and phase
- Active circuit separates the signal separation

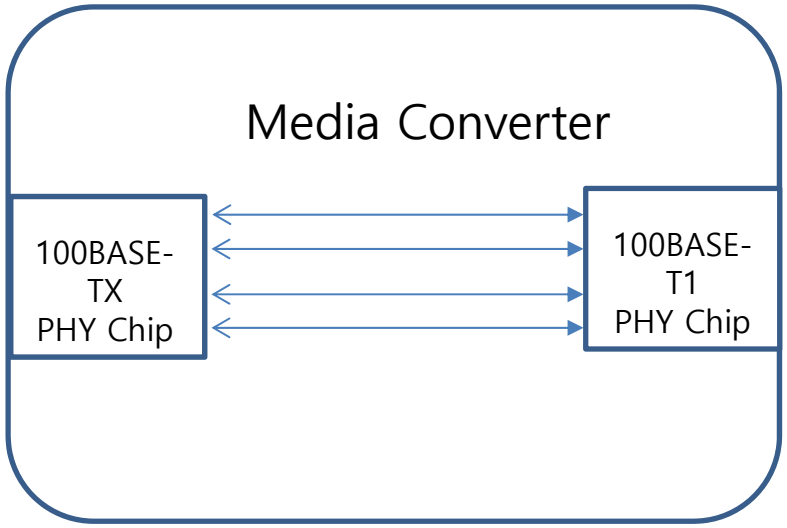
Active Taping for signal Separation





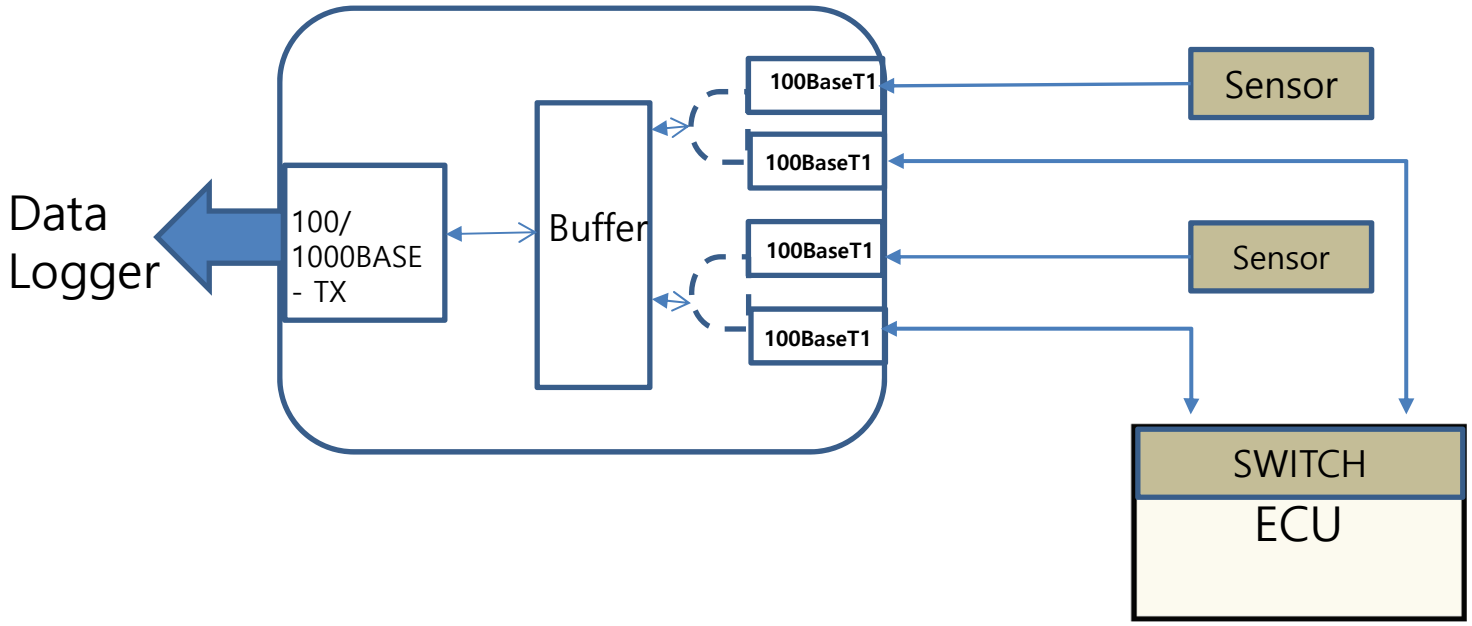
- Type 1
  - Adapts different Physical Layer
  - Buffers different Data rate and forwards
  - Bad frames not forwarded
  - Timing provided by Windows, not accurate.
- Type 2
  - Receive –tap- retransmit
  - Port copy or Port forwarding
  - Time/Frame Encapsulation
  - Causes delay, buffering , Bottle Neck
  - Lacks real-world timing for protocol Analysis

Media Converter



- Converts the 100BASE-T1 signal suitable for Fast/Standard Ethernet interface
  - Latency in translation of 100BASE-T1 to 100BASE-Tx
  - 100BASE-T1 full duplex data rate may cause buffer overflow in 100BASE-Tx half duplex data rate

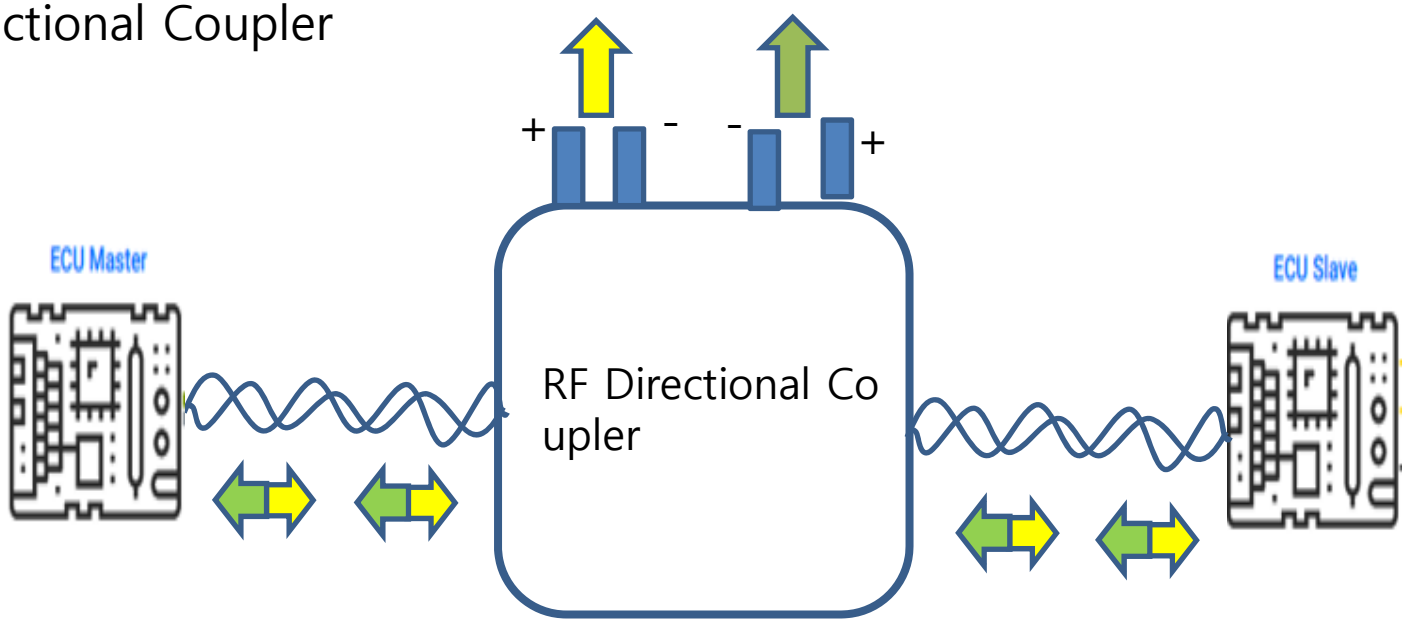
Through Port data logging



- Provides data for each sensor
- Multi port line training while debugging the design
- Buffer the data can cause timing errors
- Signal translation would cause additional delay
- Each port can be monitored

Passive Tapping of Signals

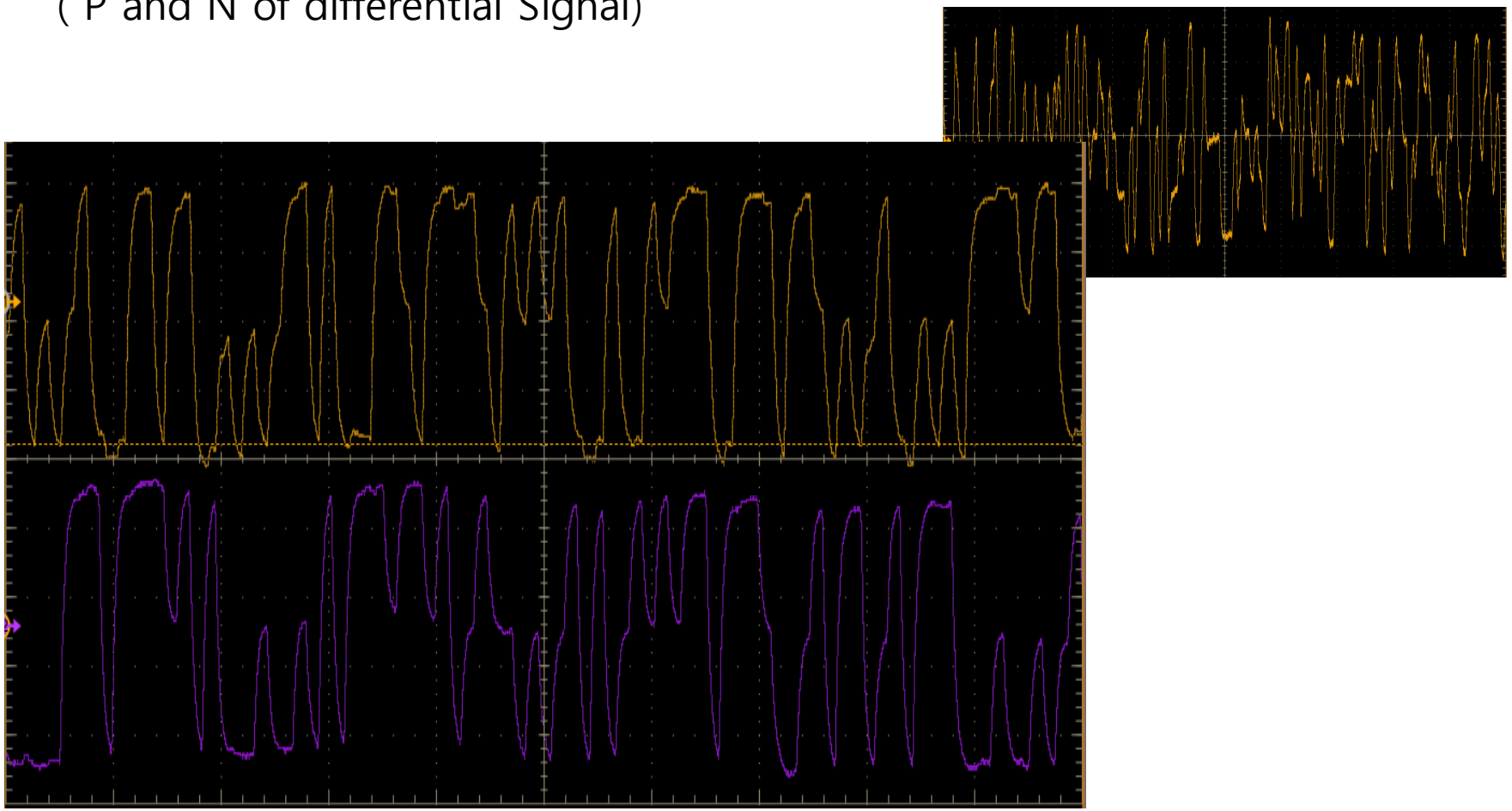
- Directional Coupler



- Passive Tap methodology
  - Small amount signal is tapped and viewed in test equipment

Output Signal from Directional Coupler

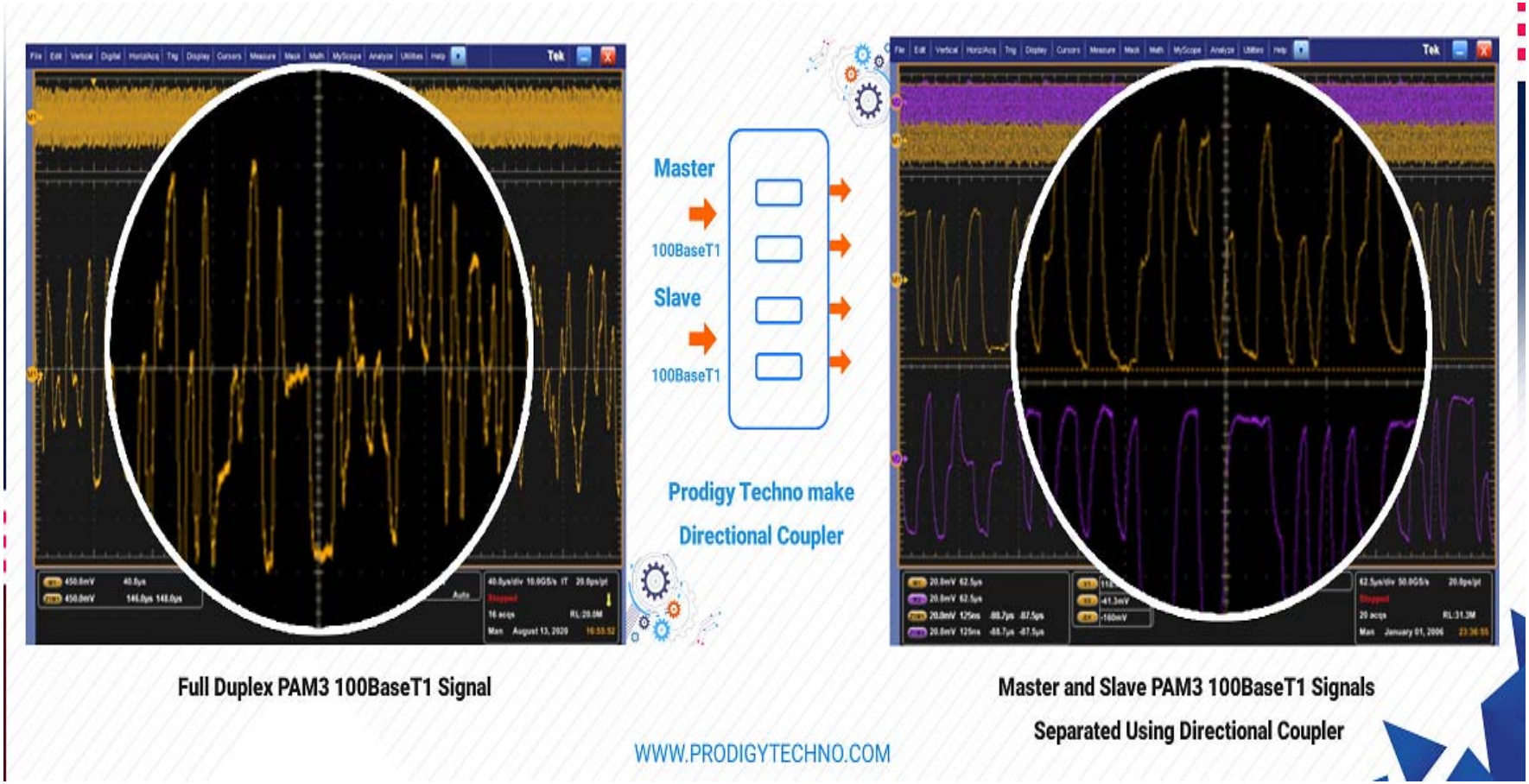
- Directional coupler separates Master and Slave signals
  (P and N of differential Signal)



Input /output waveforms of Directional Coupler

Input

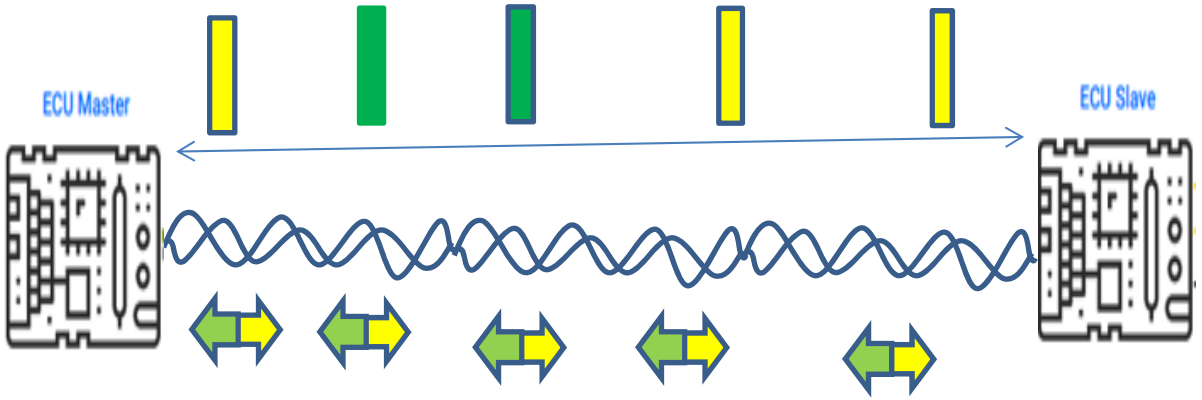
Output



Full Duplex PAM3 100BaseT1 Signal

Master and Slave PAM3 100BaseT1 Signals
Separated Using Directional Coupler

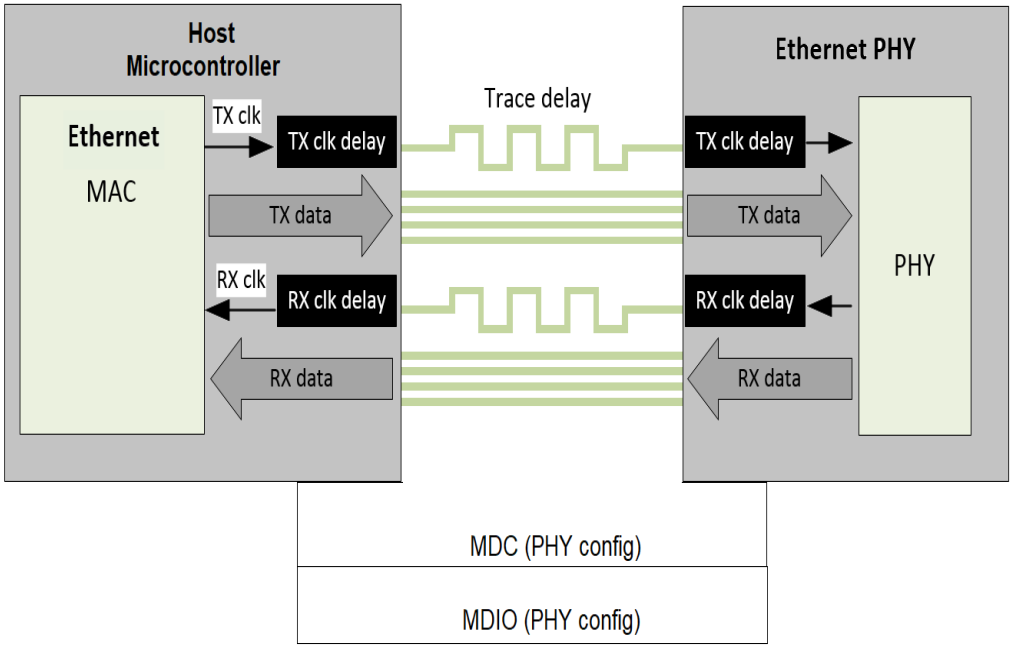
Low bus Utilization challenges in data acquisition



- Automotive bus is utilized less than 30%. Most the of the information in-between packet is idle pattern
  - Idle patterns fills the acquisition memory, very few packet capture
  - Demands the test equipment to have large expensive high speed memory
  - Demands intelligence packet capture with hardware filter for idle patterns

Correlating MDIO/MDC signals

- Many of the 100BASE-T1 Protocol Activity are dependent on MDIO/MDC Protocol activity
- Important to correlate the 100BASE-T1 Protocol Activity with MDIO/MDC signals
  - MDIO/MDC interface is used to set the PHY registers as per operational need



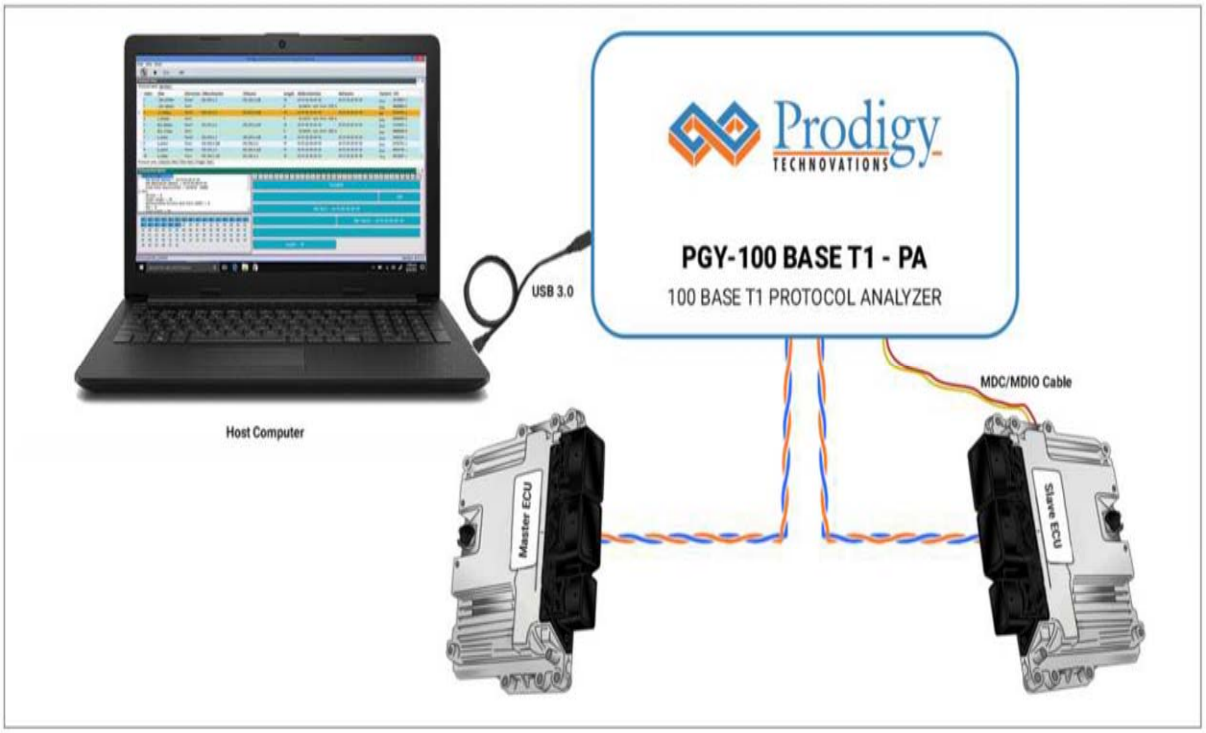
Protocol events over long period of time

- Automotive vehicles are expected operate in continuously operate long period of time
  - Operating conditions can be extreme (very cold or hot conditions)
  - Needs to operate in the presence of EMI
  - Reliability of in-vehicle network determine the customer satisfaction and profitability
- Demands extensive testing with long duration capture with flexibility analyse events which are time apart

PGY-100BASE-T1 Protocol Analysis Solutions

- Protocol decode and Analysis of 100Base-T1 Bus
- **Passive Tapping** allows non-intrusive method of monitoring 100BASE-T1 Bus
- Powerful **multi-layer protocol layer trigger** capabilities enable capturing data at specific events
- Decoding of TC10 Sleep and Wakeup events of Master and Slave ECU.
- **Continuous streaming** of protocol activity SSD/HDD enables long duration protocol data capture.
- Simultaneously monitoring of 100BASE-T1 and MDIO/MDC protocol activity

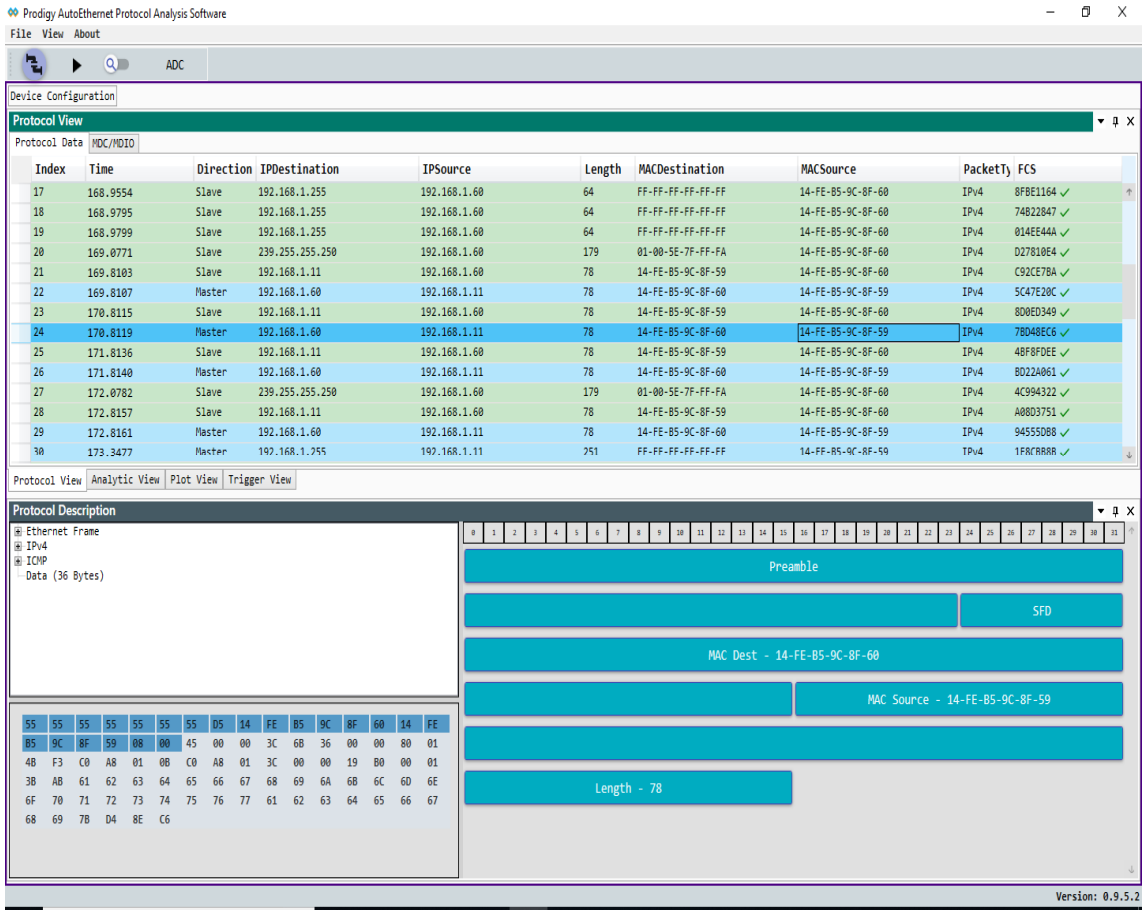
Typical 100BASE-T1 Protocol Analysis Setup



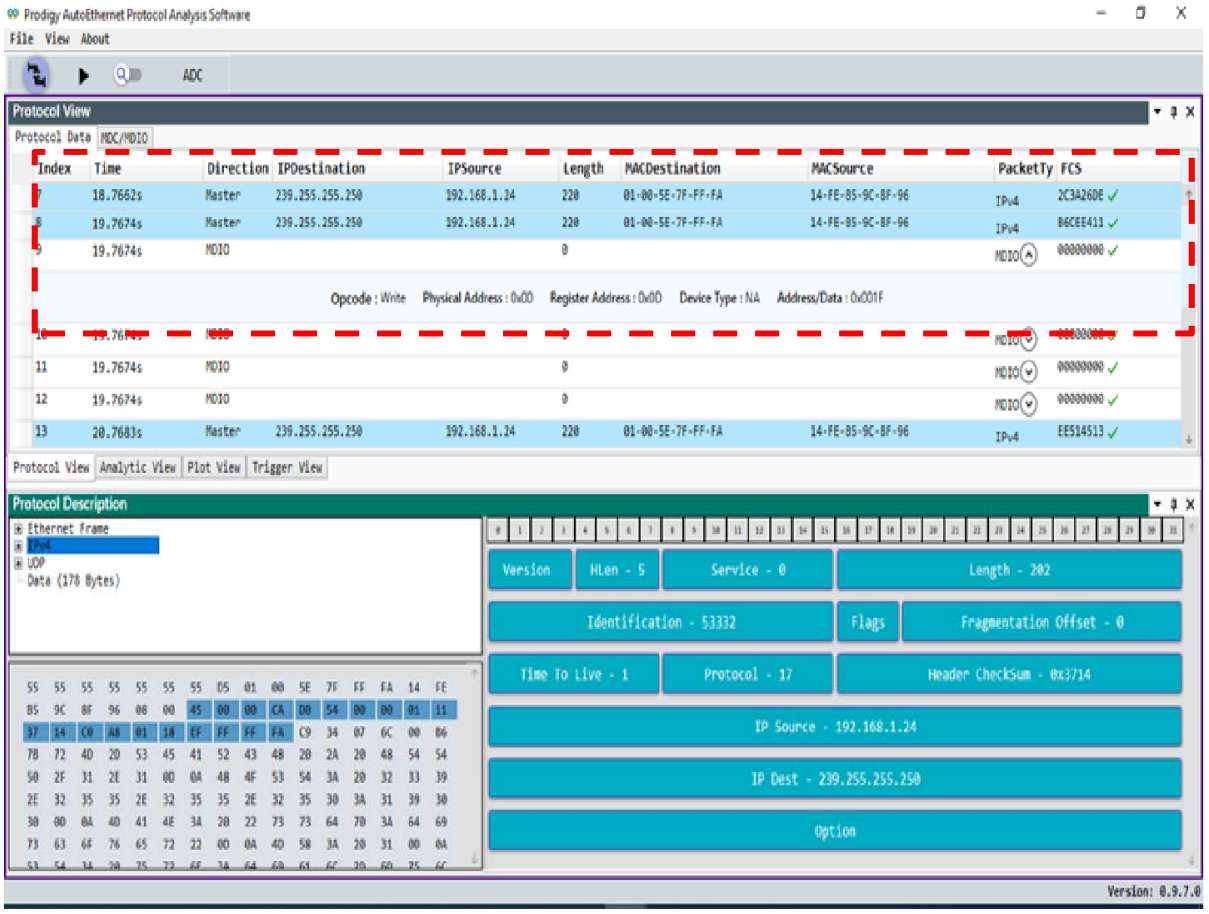
- Output of Master and Slave is input to PGY-100BASE-T1 Protocol Analyser's Directional Coupler (DC)
- Output of DC is input to signal conditioned circuit to extract +1, 0, -1 bits from PAM3 signal

Protocol Analysis view

- Ethernet Protocol Decode
- Live FCS error checks
- Decoding of IPv4, ARP, IPv6 packet
- Time Stamp of each packet

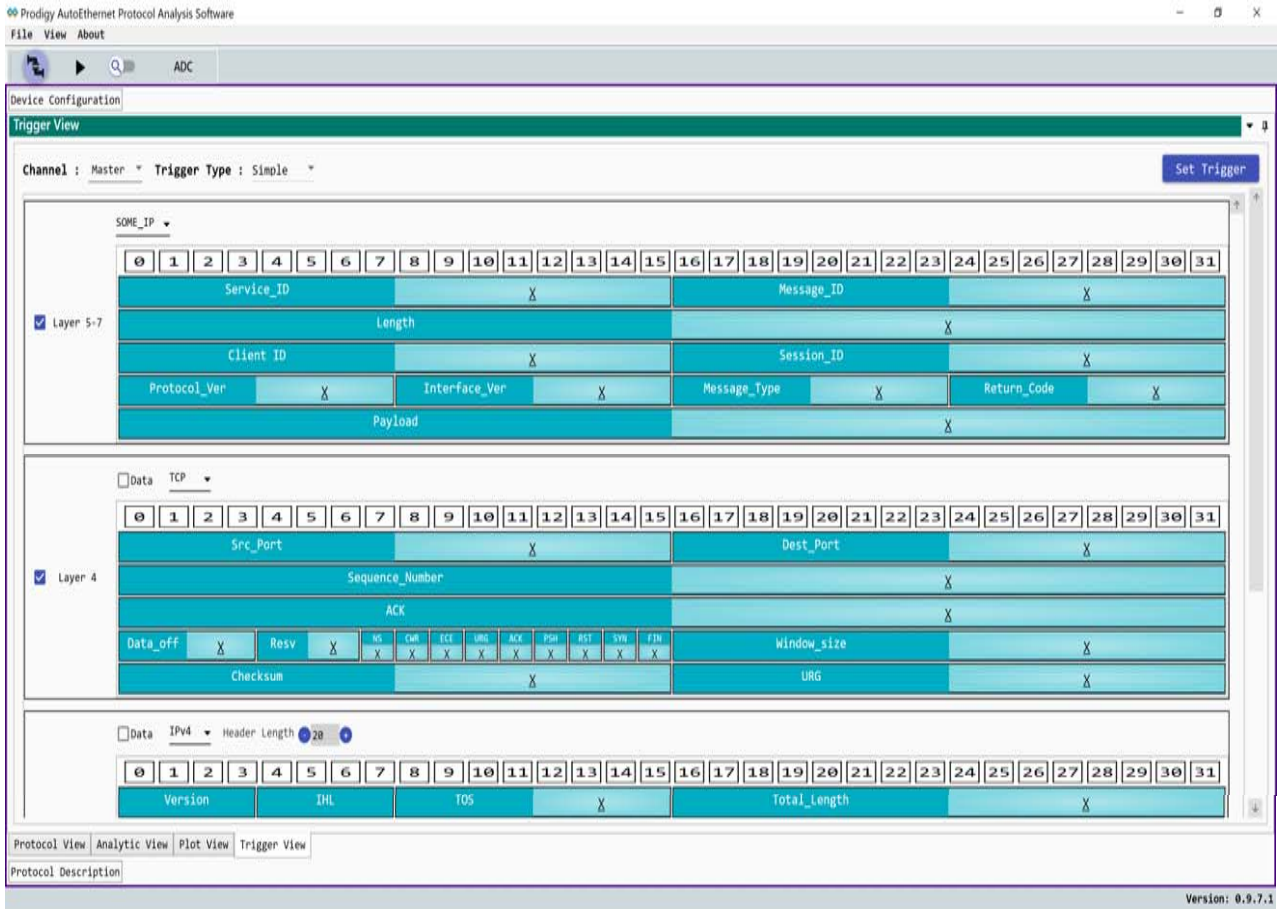


Simultaneously viewing 100BASE-T1 and MDIO decode



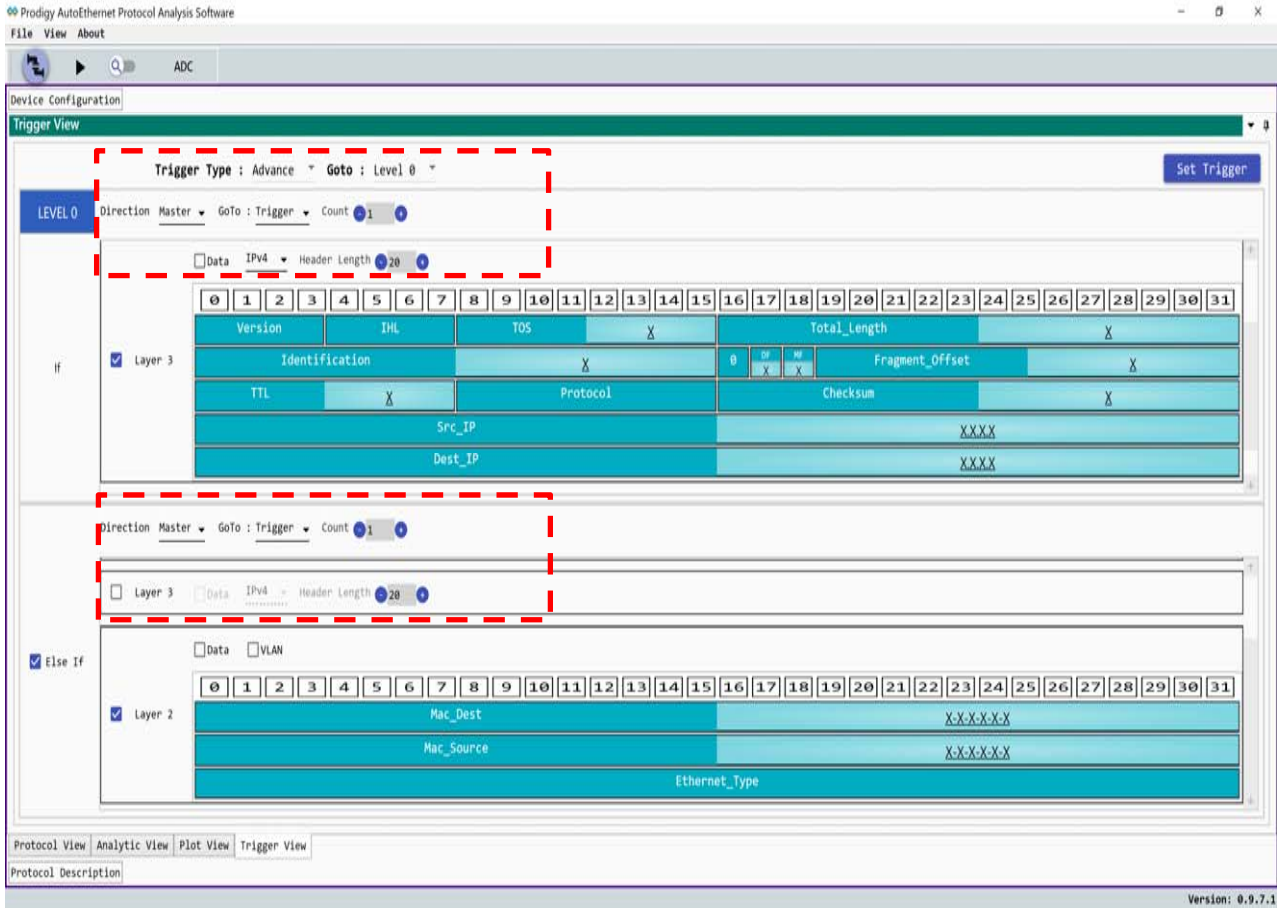
- Enables correlation of MDIO activities with 100BASE-T1 Protocol activity
- Decoding of MDIO packets

Real-time hardware trigger capabilities



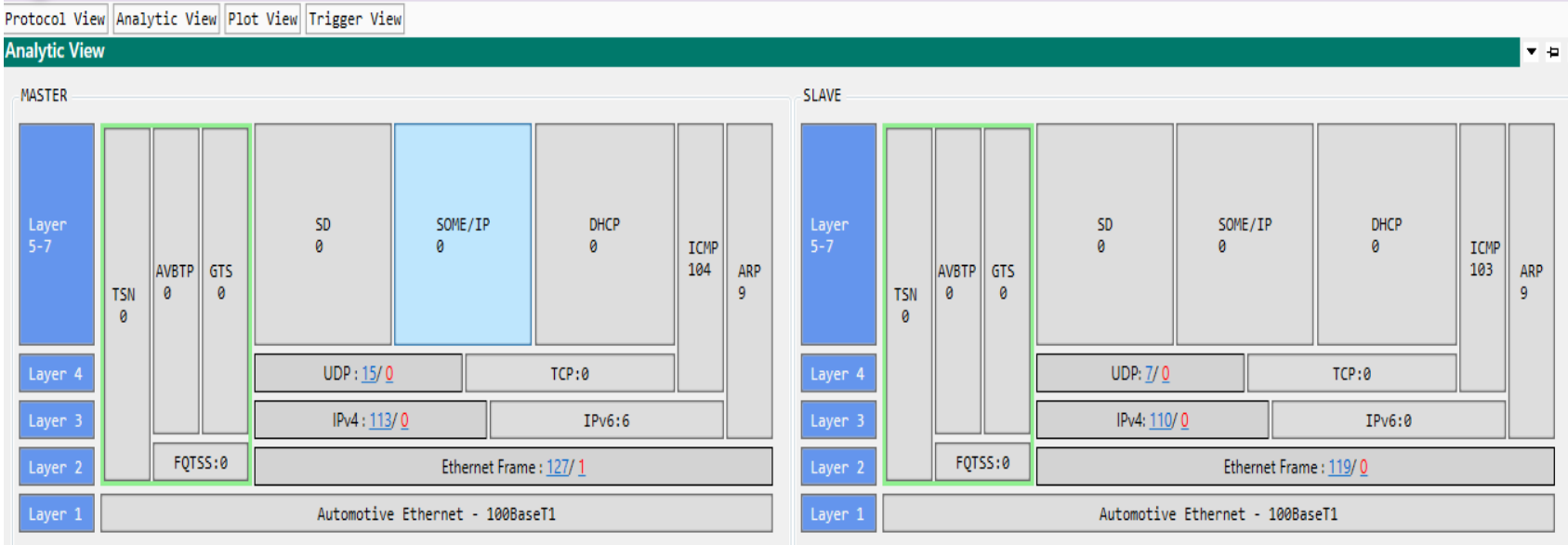
- Simple Trigger Capabilities
  - Allows protocol layer packet trigger condition setup (layer 2-7)

Real-time hardware trigger capabilities



- Advanced Trigger Capabilities (If-then-Else If)
  - Allows protocol layer packet trigger condition setup (layer2-7)

Analytical View

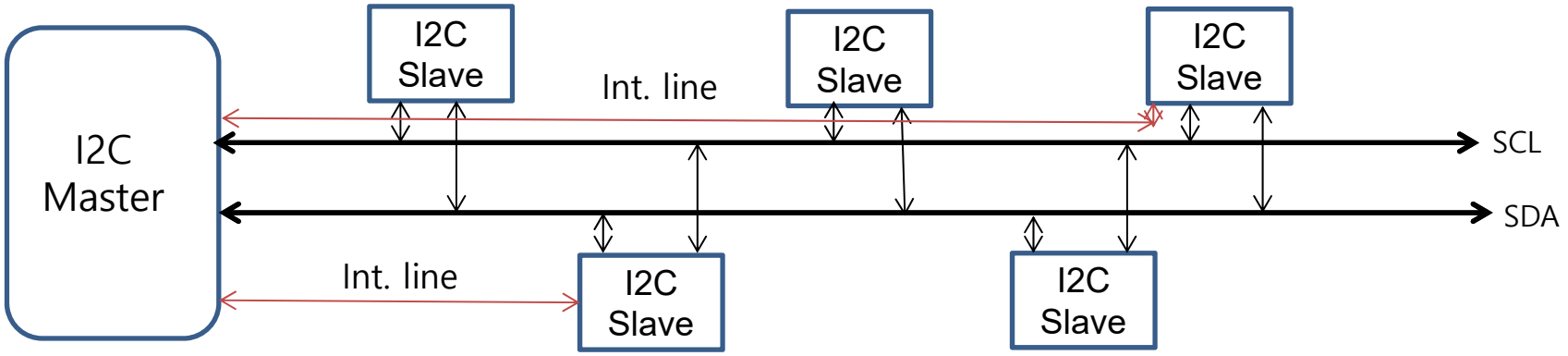


- Provides overview of different Protocol Packets
  - Counts different Protocol packets in each layer
  - Errors in Each layer

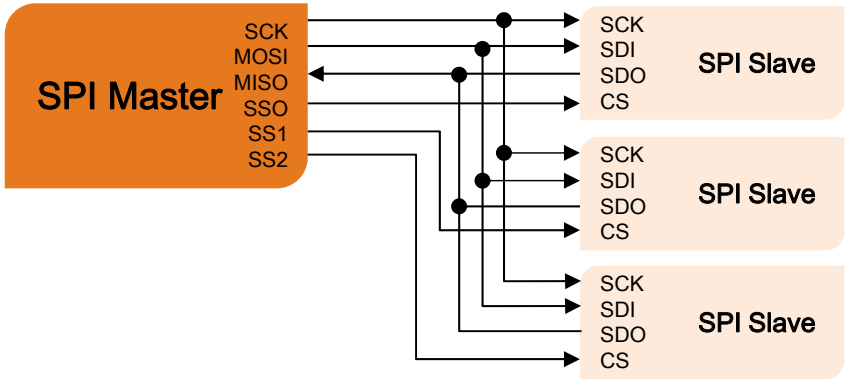
PGY-100BASET1-PA Value Proposition

- Industry first solution for non-intrusively passive tap the 100BASE-T1 bus at physical layer
  - Ensure negligible latency and accurate capturing of protocol data
- Powerful basic and multi-level layer 2 - 7 protocol trigger
  - Enables design engineer to capture protocol activity at specific event
- Continuous streaming of captured protocol data to host computer SSD/HDD
  - Enabling long duration capture

Current Low Speed Bus Interface



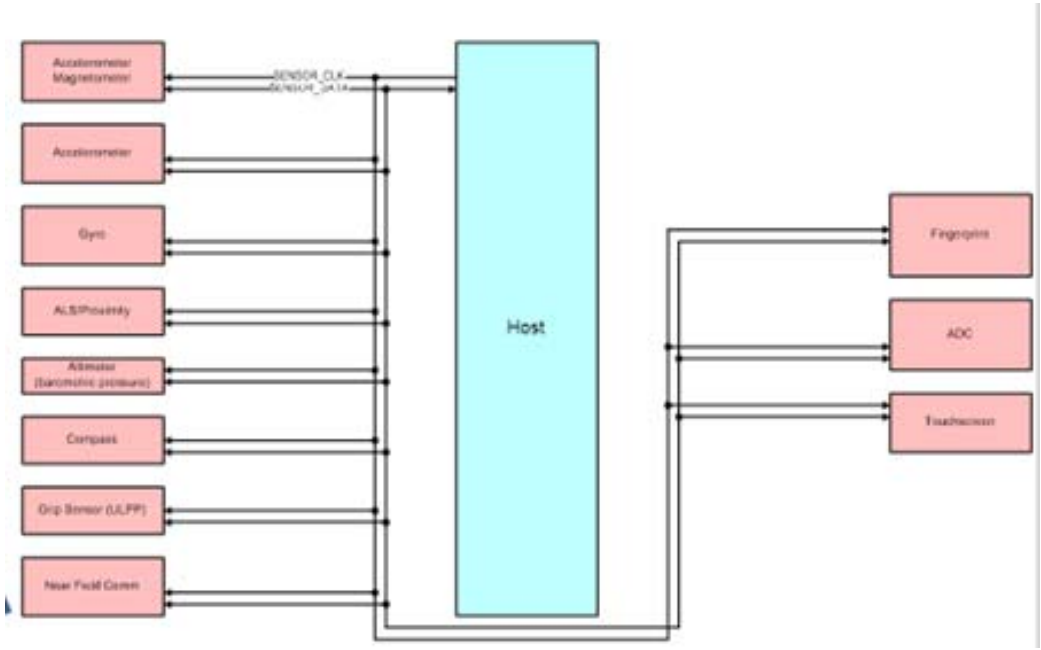
Max Speed 3.4Mbps



Max Speed 40 to 60Mbps

I3C Bus

- Higher data rate up to 33Mbps
- In-band interrupts
- Less number of IOs
- Flexible data rate varying from 1Kbps to 33Mbps
- Early adopters for sensor interfacing and DDR5 (PMIC and SPD)



I3C Interface

- Intended to improve on existing I2C/SPI Interface
- Standard multidrop interface between host processor and peripheral sensor
- Key features
  - Use of little energy possible in transporting data and control info
  - Reduce the number of physical pins
  - Two wire serial interface up to 12.5MHz
  - Legacy I2C Device can co-exist on the I3C bus
  - Dynamic addressing while supporting legacy addressing
  - I2C like serial data rate messaging
  - Optional High Data Rate messaging modes
  - Multi drop, Multi-master, In-band interrupt support, hot join support

I3C Specification Status

- I3C Specification Versions is approved by MIPI
  - I3C specification version is ver. 1.0 is the first release of I3C Spec
  - I3C Basic Specification
  - I3C ver. 1.1 is released in 2019

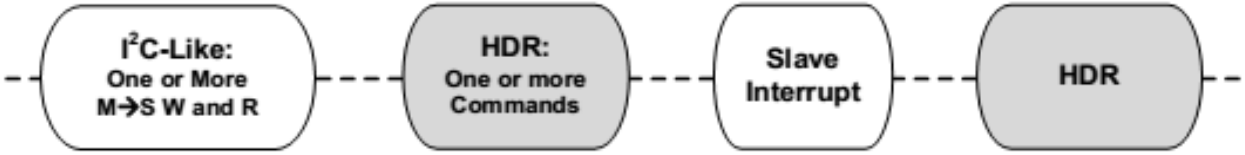
- Major features in I3C ver.1.1 compare I3C ver. 1.0
  - Multi lane support
  - Additional new commands

I3C Basic Specification

- I3C Basic Specification is in public domain
- I3C Basic Specification don't include following key features of I3C ver. 1.0 Specs
  - Timing Control
  - HDR Double Data Rate Mode (HDR-DDR)
  - HDR Ternary Symbols
    - Extends data rate
- I3C ver. 1.1 features supported in I3C Basic Spec
  - Direct read/Write CCC
  - Get Max. Data Speed Refinement
  - SETAASA CCC
  - Low Voltage/High Capacitive load IO
- To know more about I3Cver.1.0 and I3Cver.1.1, contact MIPI Alliance

I3C Fundamental principles

- Two wires are designed as SCL and SDA
  - SDA is bi-directional data line
  - SCL is a clock line driven by Master in I3C basic specification
- I3C supports mixing of various message types
  - I2C like SDR messages
  - Broadcast and Direct Common Command code messages
  - HDR mode messages
  - I2C messages
  - Slave initiated requests, In-band interrupts and request for Master Role



I3C data Speed and Data modes

- Supports most legacy I2C devices
- Single Data Rate –I3C enhanced version of I2C with data rate up to 12.5 MHz
  - I3C coding SDR
  - I3C coding SDR with CCC Direct addressing
  - I3C coding SDR with CCC broadcasted addressing

- High Data rate – Additional I3C Modes that adds significant capability in I3C ver1.0 – don't follow I2C protocol
  - HDR – Dual Data Rate Modes (HDR- DDR)
  - HDR- Ternary Symbol Legacy Mode (HDR-TSL)
  - HDR-Ternary Symbol Pure Bus-Mode (HDR-TSP)

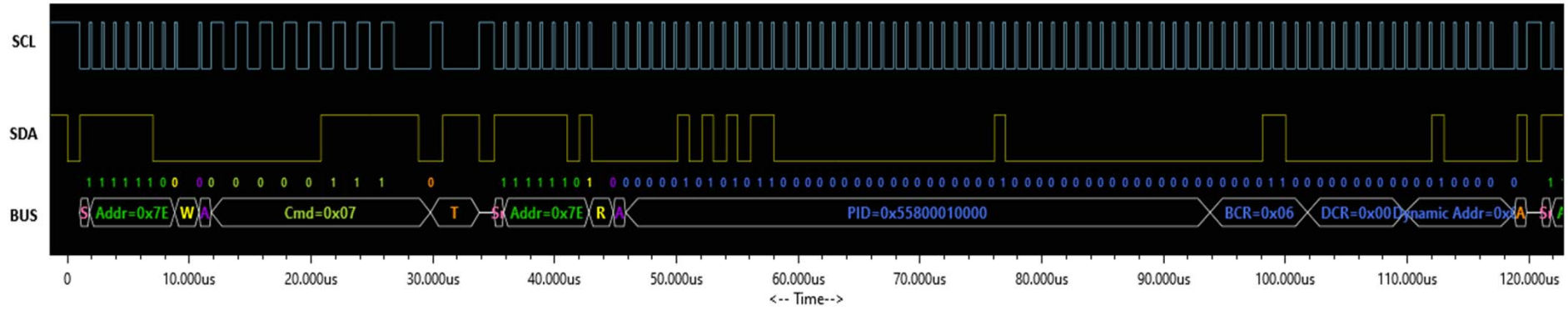
I3C Commands

- Broadcast Commands
  - Master issues these common command codes (CCC) and received by all Slaves
- Direct Command
  - Master issues this command to a specific I3C Slave device
- Private Commands
  - Master issues private write/read to a specific I3C slave device

Bus Initialization Process

- There are three methods to assign dynamic address to the slave device
  - ENTDAA Command(Enter Dynamic Address Assignment)
  - SETDASA Command(Set Dynamic Address from Static Address)
  - SETAASA Command(Set All Address from Static Address)

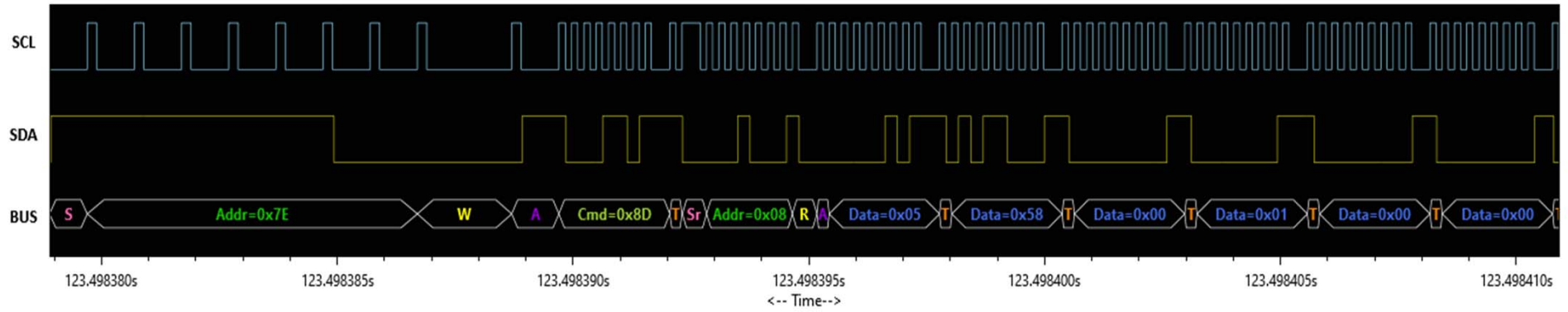
- To Change the Priority of the slave device
  - SETNEWDA Command(Set New Dynamic Address)



ENTDAA Sequence

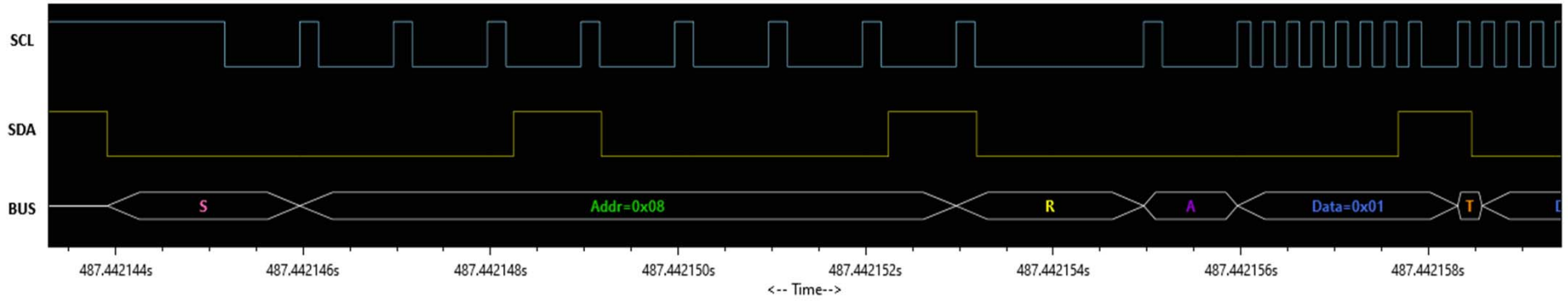
Directed Commands use case

- Directed Commands are used to write/read registers from the slave devices
- List of registers in the slave
  - Max read length
  - Max write length
  - Bus characteristics register
  - Device characteristics register
  - Provisional ID
  - Device status



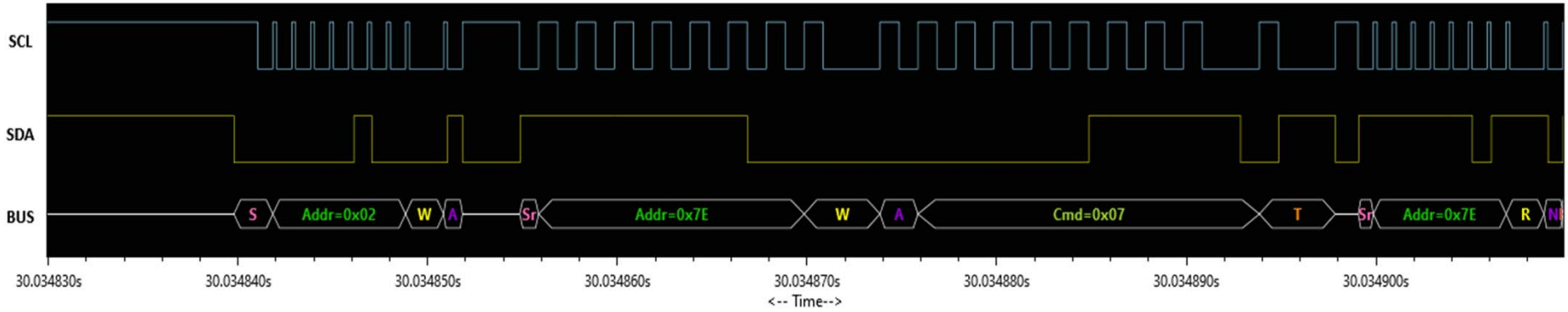
In-band Interrupt process

- In-band interrupt is initiated by the slave
- To initiate in-band interrupt, slave will pull SDA line low
- Master should send open drain frequency clock on the bus.
- Slave should send its own dynamic address with read bit set on the SDA line.
- As per mutual understanding between master and slave, Master can initiate Read operation.



Hot Join Process

- Hot join is initiated by the slave
- To initiate Hot join, slave will pull SDA line low
- Master should send open drain frequency clock on the bus
- Slave should send 8'h02 on the SDA line
- After that master can initiate address assignment procedure



Testing I3C Devices

- I3C devices need to electrical specification of I3C basic
  - Need to meet DC I/O Characteristics
  - Timing Characteristics at I2C Speed
  - Timing Characteristics at open drain operation
  - Timing Characteristics at Push-pull operation

- Need to test I3C devices for different Protocol support
  - I3C Slave
  - I3C Master
  - Legacy I2C devices
  - Error Injections
  - Margin tests
  - JEDEC Spec JESD301-1 (PMIC) and JESD300-1 (SPD)

DC IO Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	1.10 1.65 2.97	1.20 1.80 3.30	1.30 1.95 3.63	V
Low-Level Input Voltage	V_{IL}	-0.3	-	0.3 * V_{DD}	V
High-Level Input Voltage	V_{IH}	0.7 * V_{DD}	-	V_{DD} + 0.3	V
Schmitt Trigger Inputs Hysteresis	V_{hys}	0.1 * V_{DD}	-	-	V
Output Low Level	V_{OL}	- -	- -	0.18 0.27	V V
Input Current (per Input-Only I/O Pin)	I_I	-10 -5	- -	10 5	µA µA
Capacitance (per Only I/O Pin)	C_I	- -	- -	5 10	pF pF
Capacitance Mismatch Between Pins	ΔC	- -	- -	1.5 3	pF pF
Push-Pull Only					
Output High Level	V_{OH} 	V_{DD} – 0.18 V_{DD} – 0.27	- -	- -	V V
Legacy Mode with Pull-up					
Pull-Up for Open Drain	R_P	$V_{DD} - V_{OL}$ 3mA For $V_{DD} \geq$ 1.4V $V_{DD} - V_{OL}$ 2mA For $V_{DD} \geq$ 1.4V	t_r 0.8473 * Cb 2833		Ω

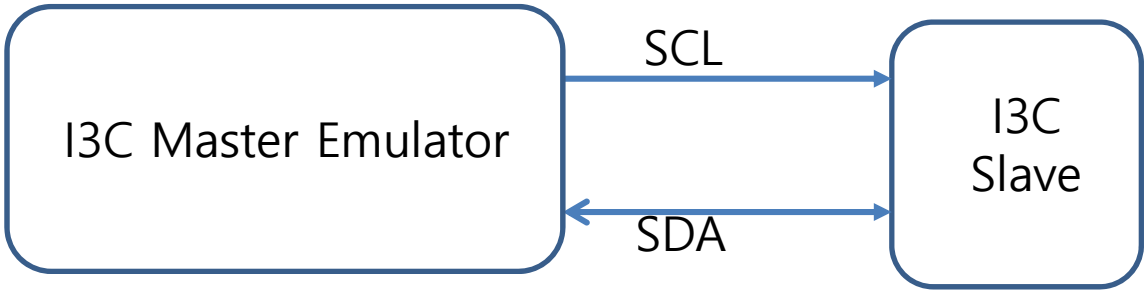
Timing Requirement at I2C legacy Devices

Parameter	Symbol	Legacy Mode 400kHz / Fm		Legacy Mode 1MHz / Fm+		Units
		Min	Max	Min	Max	
SCL Clock Frequency	f_{SCL}	0	0.4	0	1.0	MHz
Setup Time for a Repeated START	t_{SU_STA}	600	-	260	-	ns
Hold Time for a (Repeated) START	t_{HD_STA}	600	-	260	-	ns
SCL Clock Low Period	t_{LOW}	1300	-	500	-	ns
	t_{DIG_L}	$t_{LOW} + t_{rCL}$	-	$t_{LOW} + t_{rCL}$	-	ns
SCL Clock High Period	t_{HIGH}	600	-	260	-	ns
	t_{DIG_H}	$t_{HIGH} + t_{rCL}$	-	$t_{HIGH} + t_{rCL}$	-	ns
Data Setup Time	t_{SU_DAT}	100	-	50	-	ns
Data Hold Time	t_{HD_DAT}	-	-	-	-	ns
SCL Signal Rise Time	t_{rCL}	20	300	-	120	ns
SCL Signal Fall Time	t_{fCL}	20 * (V_{DD} / 5.5 V)	300	20 * (V_{DD} / 5.5 V)	120	ns
SDA Signal Rise Time	t_{rDA}	20	300	-	120	ns
SDA Signal Fall Time	t_{fDA}	20 * (V_{DD} / 5.5 V)	300	20 * (V_{DD} / 5.5 V)	120	ns
Setup Time for STOP	t_{SU_STO}	600	-	260	-	ns
Bus Free Time Between a STOP Condition and a START Condition	t_{BUF}	1.3	-	0.5	-	µs
Pulse Width of Spikes that the Spike Filter Must Suppress	t_{SPIKE}	0	50	0	50	ns

I3C timing Measurements Push-Pull Mode

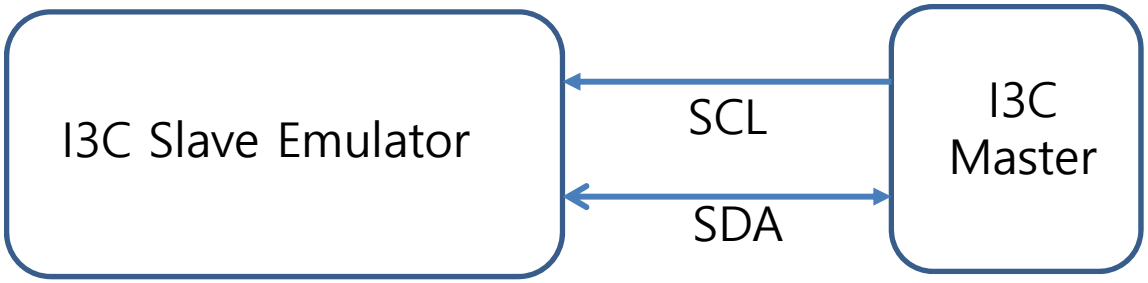
Parameter		Symbol	Min	Typ	Max	Units
SCL Clock Frequency		f_{SCL}	0.01	12.5	12.9	MHz
SCL Clock Low Period		t_{LOW}	24	-	-	ns
		t_{DIG_L}	32	-	-	ns
SCL Clock High Period for Mixed Bus		t_{HIGH_MIXED}	24	-	-	ns
		$t_{DIG\_H\_MIXED}$	32	-	45	ns
SCL Clock High Period		t_{HIGH}	24	-	-	ns
		t_{DIG_H}	32	-	-	ns
Clock in to Data Out for Slave		t_{SCO}	-	-	12	ns
SCL Clock Rise Time		t_{CR}	-	-	150e06 * 1 / f_{SCL} (capped at 60)	ns
SCL Clock Fall Time		t_{CF}	-	-	150e06 * 1 / f_{SCL} (capped at 60)	ns
SDA Signal Data Hold in Push-Pull Mode	Master	t_{HD_PP}	t_{CR} + 3 and t_{CP} + 3	-	-	-
	Slave	t_{HD_PP}	0	-	-	-
SDA Signal Data Setup in Push-Pull Mode		t_{SU_PP}	3	-	N/A	ns
Clock After Repeated START (Sr)		t_{CASr}	t_{CASmin}	-	N/A	ns
Clock Before Repeated START (Sr)		t_{CBSr}	t_{CASmin} / 2	-	N/A	ns
Capacitive Load per Bus Line (SDA/SCL)		C_b	-	-	50	pF

Testing I3C Slave Device



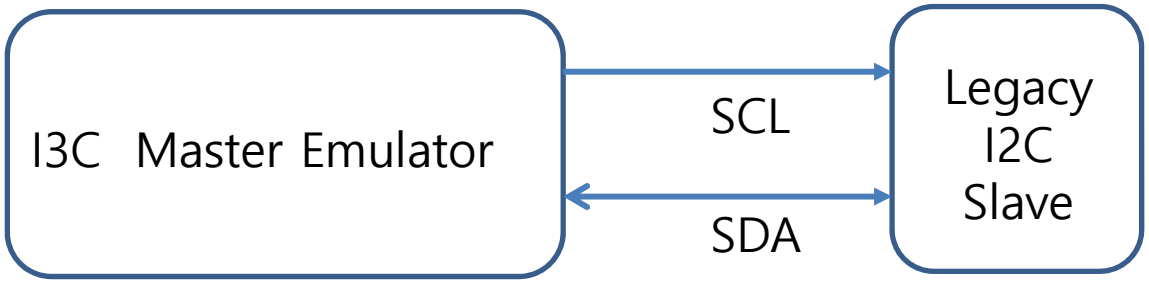
- I3C Master Emulator Requirements
  - Should be able to operate at all Vdd voltage range
  - Should vary the timing parameters
  - Capable of sending CCC commands
  - Protocol layer Error Injection
  - Voltage and Timing Margin Test Capability to stress the DC and timing parameters of slave
  - Should handle Slave Interrupt
  - Should support hot join

Testing I3C Master Testing Needs



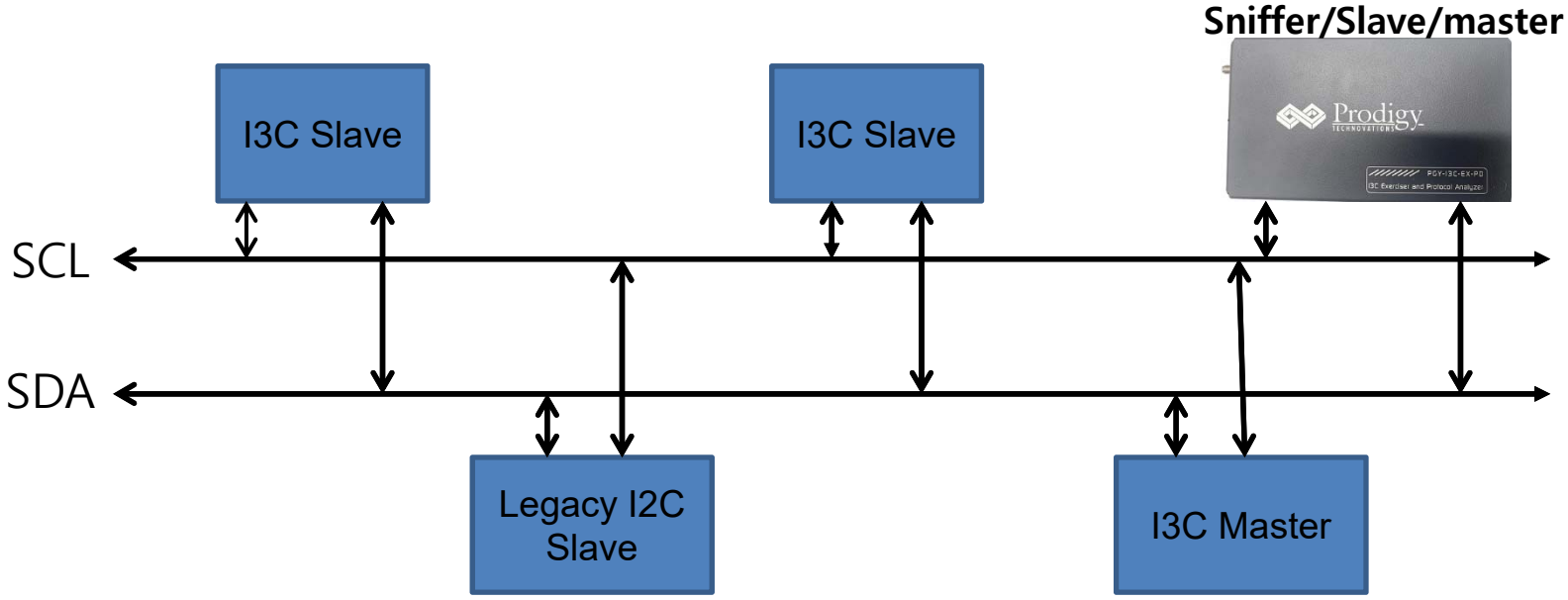
- I3C Slave Emulator Requirements
  - Should be able to operate at all Vdd voltage range
  - Should respond to master within I3C timing spec
  - Capable of responding CCC commands
  - Respond appropriately to Protocol layer errors
  - Interrupt capable
  - Hot Join support

Testing Legacy I2C Slave in I3C Bus



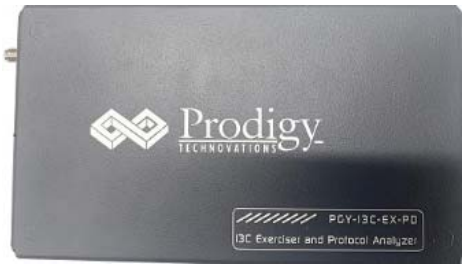
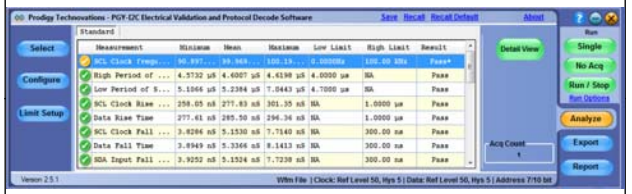
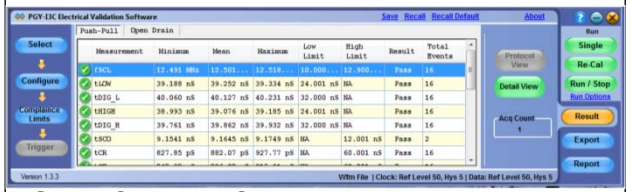
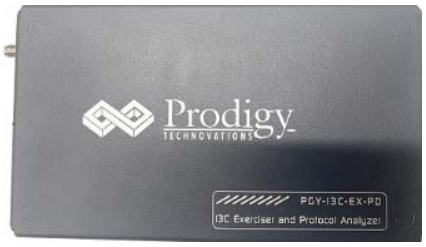
- I3C Master Emulator Requirements
  - Should be able to operate at all Vdd voltage range
  - Should vary the timing parameters
  - Should be able to generate I2C write/read commands
  - Voltage and Timing Margin Test Capability to stress the DC and tim ing parameters of slave

Emulating I3C Bus



- Emulate I3C with Master and Slave
  - Real world traffic generation of Master and Slave
  - Continuously capture I3C traffic
  - Real time analysis of errors in I3C Traffic
  - Hardware based trigger on I3C Protocol packets
  - Search and Filter features
  - Report Generation

Test Solution from Prodigy

I3C Bus Electrical and Protocol Test Needs	Prodigy Technovation Solution	
	Generation or Exerciser	Measurement and Anlysis
DC I/O Chracterization		
Timing Charcatertics at I2C Speed		PGY-I2C-EV I2C Electrical Validation
Timing Characteristics at Open Drain operation for I3C		
Timing Characteristics at Open Drain operation for I3C		PGY-I3C-EV I3C Electrical validation
I3C Master Emulation		
I3C Slave Emulation		
Legacy I2C Slave Emulation		
I3C Secondary master Emulation		
I3C Bus Emulation	**PGY-I3C-EX-PD I3c Exerciser and Protocol Analyzer**	**PGY-I3C-EX-PD I3C Exerciser and Protocol Analyzer**

TAMsystech

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