



# Configuring the Intel<sup>®</sup> FPGA E-Tile Hard IP for Ethernet

# Configuring the Intel® FPGA E-Tile Hard IP for Ethernet - Objective and Agenda

Describe the method for configuring the features and functionality of the Hard IP for Ethernet found in Intel® FPGA E-Tiles

- Overview and hard IP features
- Parameterizing the IP

# Prerequisites

- Understanding of the Ethernet protocols
- Understanding of the FPGA design flow
- Familiarity with the Intel® FPGA E-tile and Hard IP for Ethernet architecture
  - Documentation: E-Tile Transceiver PHY User Guide
    - <https://www.intel.com/content/www/us/en/programmable/documentation/kqh1479167866037.html>
  - Online training: Intel® FPGA E-Tile Transceiver Basics
    - <https://www.intel.com/content/www/us/en/programmable/support/training/course/os101116.html>

# E-Tile Hard IP for Ethernet Intel® FPGA IP Core

The E-Tile Hard IP for Ethernet IP Core supports full and partial configurations of the following variants

- Single channel **10GE/25GE**
- 1 – 4 channels **10GE/25GE** with optional Reed-Solomon Forward Error Correction (RS-FEC)
- **100GE** with optional RS-FEC
- **100GE** or 1 – 4 channels **10GE/25GE** with optional RS-FEC and optional 1588 Precision Time Protocol (PTP)
- Custom PCS with optional RS-FEC

# Ethernet Hard IP Use model

Intel® Stratix 10® E-tile Floor Plan					Channel Settings				
XCVR PMA	RSFEC	EHIP_TOP		Core Interface	Protocol	Level	Rate	FEC mode	RS FEC
Channel_23	RESFEC_5	EHIP_CORE_3	EHIPLANE_23	Interface_23	None	None	None	Off	Off
Channel_22			EHIPLANE_22	Interface_22	None	None	None		Off
Channel_21			EHIPLANE_21	Interface_21	None	None	None		Off
Channel_20			EHIPLANE_20	Interface_20	Ethernet	NRZ	10G		Off
Channel_19	RESFEC_4	EHIP_CORE_3	EHIPLANE_19	Interface_19	None	None	Off	Off	
Channel_18			EHIPLANE_18	Interface_18	None	None		None	Off
Channel_17			EHIPLANE_17	Interface_17	None	None		None	Off
Channel_16			EHIPLANE_16	Interface_16	None	None		None	Off
Channel_15	RESFEC_3	EHIP_CORE_2	EHIPLANE_15	Interface_15	Ethernet	NRZ	25.78G	Fractured	528, 514
Channel_14			EHIPLANE_14	Interface_14	Ethernet	NRZ	25.78G		528, 514
Channel_13			EHIPLANE_13	Interface_13	None	None	None		Off
Channel_12			EHIPLANE_12	Interface_12	None	None	None		Off
Channel_11	RESFEC_2	EHIP_CORE_1	EHIPLANE_11	Interface_11	Ethernet	NRZ	25.78G	Aggregate	528, 514
Channel_10			EHIPLANE_10	Interface_10	Ethernet	NRZ	25.78G		528, 514
Channel_9			EHIPLANE_9	Interface_9	Ethernet	NRZ	25.78G		528, 514
Channel_8			EHIPLANE_8	Interface_8	Ethernet	NRZ	25.78G		528, 514
Channel_7	RESFEC_1	EHIP_CORE_1	EHIPLANE_7	Interface_7	None	None	Off	Off	
Channel_6			EHIPLANE_6	Interface_6	None	None		None	Off
Channel_5			EHIPLANE_5	Interface_5	PTP	None		None	Off
Channel_4			EHIPLANE_4	Interface_4	PTP	None		None	Off
Channel_3	RESFEC_0	EHIP_CORE_0	EHIPLANE_3	Interface_3	Ethernet	NRZ	25.78G	Aggregate	528, 514
Channel_2			EHIPLANE_2	Interface_2	Ethernet	NRZ	25.78G		528, 514
Channel_1			EHIPLANE_1	Interface_1	Ethernet	NRZ	25.78G		528, 514
Channel_0			EHIPLANE_0	Interface_0	Ethernet	NRZ	25.78G		528, 514

Variant A: Single 10GE/25GE

Variant B: 1 to 4 10GE/25GE with optional RS-FEC

Variant C: 100GE with optional RS-FEC

Variant D: 100GE or 1 to 4 10GE/25GE with optional RS-FEC and optional PTP (6 channels total)

# E-Tile Ethernet Protocol Support

IP Version	Protocol	Details
100GE	100GBASE-KR4	4 x 25.78125 Gbps non-return-to-zero (NRZ) for copper backplane
	100GBASE-CR4	4 x 25.78125 Gbps NRZ for Direct Attach Copper Cable
	CAUI-4	4 x 25.78125 Gbps NRZ lanes for Low Loss Links: Chip-to-Chip or Chip-to-Module
	CAUI-2	2 x 53.125 Gbps PAM4 lanes for Low Loss Links: Chip-to-Chip, Chip-to-Module, and DAC
25GE	25GBASE-KR	1 x 25.78125 Gbps lane for Backplane
	25GBASE-CR	1 x 25.78125 Gbps lane for Direct Attach Copper Cable
	25GBASE-R AUI	1 x 25.78125 Gbps lane for Low Loss Connections to External PHY Modules
	25GBASE-R Consortium Link	1 x 25.78125 Gbps lane based on the 25G/50G Consortium Specification
10GE	10GBASE-KR	1 x 10.3125 Gbps lane for Backplane
	10GBASE-CR	1 x 10.3125 Gbps lane for Direct Attach Copper Cable

# Example E-Tile Hard IP for Ethernet IP Core

## Features

- Optional auto negotiation and/or link training logic
- Optional 1588v2 PTP
- RS-FEC(528,514) and RS-FEC(544,514) support for 25G and 100G Ethernet
- Frame structure control such as jumbo packet and interpacket gap (IPG) length
- Frame monitoring and statistics control such as link fault detection and reporting and CRC checking and error reporting
- Serial PMA and parallel loop-back support for self-diagnostic testing
- Interface for reading and controlling internal management registers

# Core Implementation Variations

Available on all IP core variants except Custom PCS with optional RS-FEC

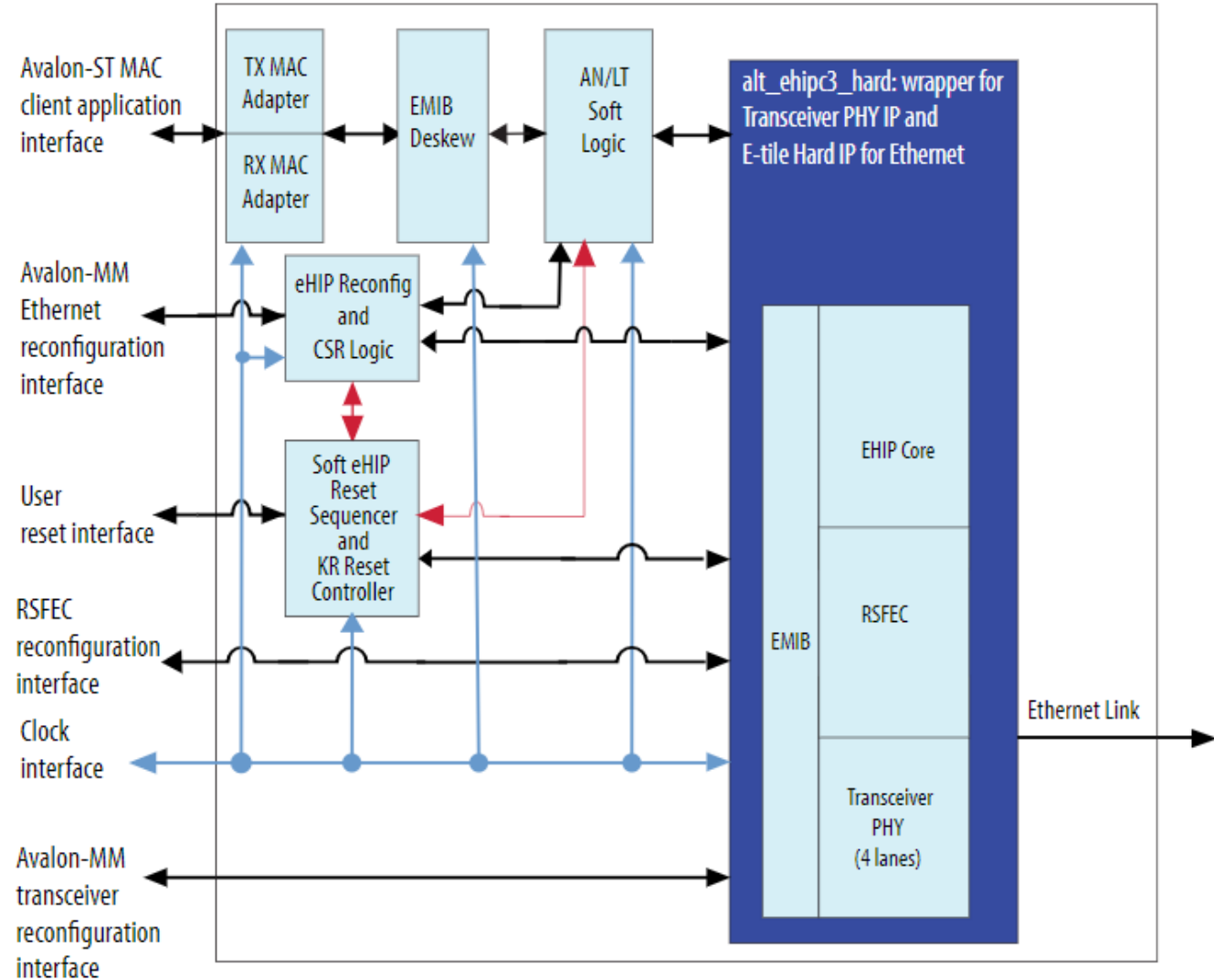
- MAC and PCS
- PCS only
- Flexible Ethernet (FlexE)
- Optical Transport Network (OTN)
  
- E-tile transceivers used for PMA/PMD in all implementations

# E-tile Hard IP for Ethernet Block Diagram

Example 100GE with RS-FEC Block Diagram

The E-tile Ethernet IP consist of both hard (on-tile) and soft (in FPGA) logic

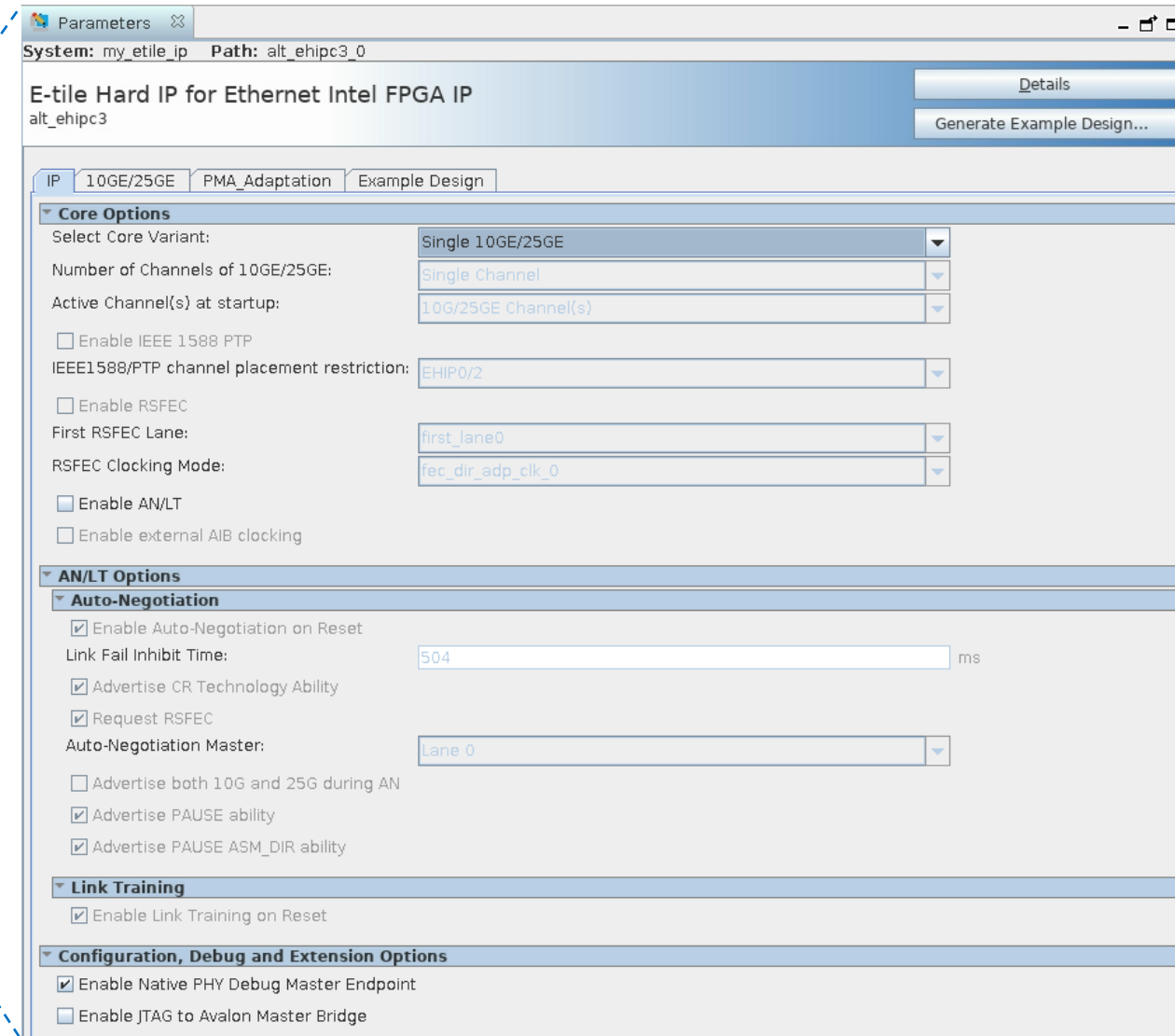
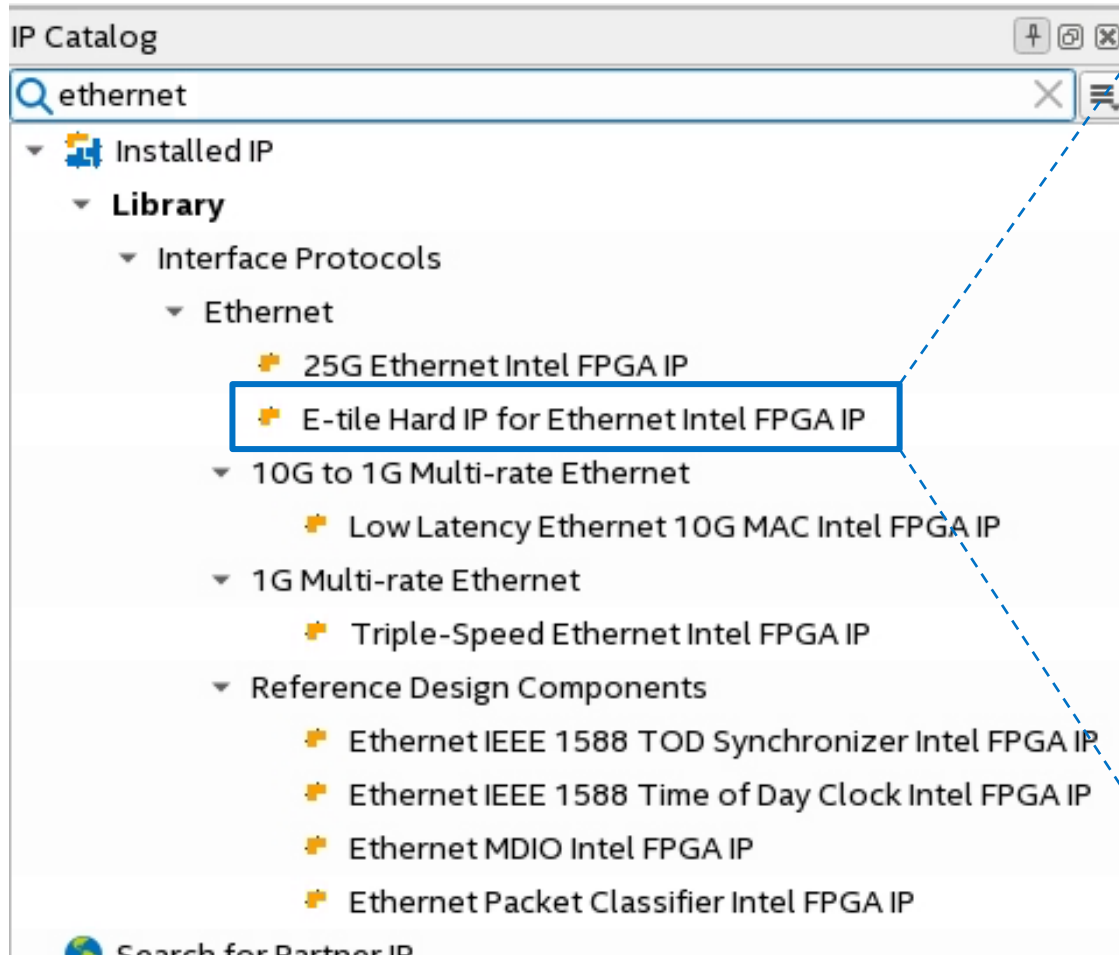
- Hard logic
  - MAC/PCS/PMA
  - RS-FEC
  - PTP
- Soft logic
  - Auto-negotiation and link training logic
  - Reset controller and sequencer
  - Reconfiguration and CSR logic
  - RX and TX adapters



# Configuring the Intel® Stratix® 10 FPGA E-Tile Hard IP for Ethernet

Parameterizing the E-Tile Hard IP for Ethernet

# E-tile Hard IP for Ethernet Intel FPGA Parameter Editor



# Parameter Editor – IP Tab

**E-tile Hard IP for Ethernet Intel FPGA IP**  
alt\_ehipc3

Details  
Generate Example Design...

IP 10GE/25GE PMA\_Adaptation Example Design

**Core Options**

Select Core Variant:  
Single 10GE/25GE  
Single 10GE/25GE  
1 to 4 10GE/25GE with optional RSFEC  
Single 100GE with optional RSFEC  
100GE or 1 to 4 10GE/25GE with optional RSFEC and 1588 PTP  
Custom PCS with optional RSFEC

Number of Channels of 10GE/25GE:

Active Channel(s) at startup:

Enable IEEE 1588 PTP

IEEE1588/PTP channel placement restriction:

Enable RSFEC

First RSFEC Lane: first\_lane0

RSFEC Clocking Mode: fec\_dir\_adp\_clk\_0

Enable AN/LT

Enable external AIB clocking

# Parameter Editor – IP Tab (cont.)

IP 100GE 10GE/25GE PMA\_Adaptation Example Design

**Core Options**

Select Core Variant: 100GE or 1 to 4 10GE/25GE with optional RSFEC and 1588 PTP

Number of Channels of 10GE/25GE: Single Channel

Active Channel(s) at startup: 10G/25GE Channel(s)

Enable IEEE 1588 PTP  
IEEE1588/PTP channel placement restriction: EHIP0/2

Enable RSFEC  
First RSFEC Lane: first\_lane0  
RSFEC Clcking Mode: fec\_dir\_adp\_clk\_0

Enable AN/LT

Enable external AIB clcking

**AN/LT Options**

**Auto-Negotiation**

Enable Auto-Negotiation on Reset  
Link Fail Inhibit Time: 504 ms

Advertise CR Technology Ability  
 Request RSFEC  
Auto-Negotiation Master: Lane 0

Advertise both 10G and 25G during AN  
 Advertise PAUSE ability  
 Advertise PAUSE ASM\_DIR ability

**Link Training**

Enable Link Training on Reset

**Configuration, Debug and Extension Options**

Enable Native PHY Debug Master Endpoint  
 Enable JTAG to Avalon Master Bridge

Choose # of 10GE/25GE channels  
Choose Active channel at start up

Enables RS-FEC and PTP

Enables AN/LT

# Parameter Editor– 100GE Tab

IP 100GE 10GE/25GE PMA\_Adaptation Example Design

**General Options 100GE**

Select Ethernet Rate: 100G

Select Ethernet IP Layers: MAC+PCS+(528,514)RSFEC

**MAC Options 100GE**

Basic 100GE Specialize

TX Maximum Frame Size: [ ]

RX Maximum Frame Size: [ ]

Enforce Maximum Frame Size

Choose Link Fault Generation: [ ]

Stop TX traffic when link down: [ ]

Bytes to remove from RX: [ ]

Forward RX Pause Reason

Use Source Address Insertion

Enable TX VLAN Detection

Enable RX VLAN Detection

Ready latency: 0

**PMA Options 100GE**

PHY Reference Frequency: 156.250000 MHz

Ethernet rate fixed at 100G

Choose core variation and RS-FEC version

Select from list of PHY reference clock frequencies

\* For the 100GE or 1 to 4 10GE/25GE with optional RSFEC and 1588 PTP variant, requires setting the Active Channel at Startup option on the IP tab to 100GE Channel

# Parameter Editor – 10GE/25GE Tab

IP 100GE 10GE/25GE PMA\_Adaptation Example Design

**General Options 10GE/25GE**

Select Ethernet Rate: 25G

Select Ethernet IP Layers: MAC+PCS

Include alternate ports

**MAC Options 10GE/25GE**

Basic 10GE/25GE Specialized 10GE/25GE

TX Maximum Frame Size: 1518

RX Maximum Frame Size: 1518

Enforce Maximum Frame Size

Choose Link Fault Generation Mode: Bidirectional

Stop TX traffic when link partner sends PAUSE?: No

Bytes to remove from RX frames: Remove CRC bytes

Forward RX Pause Requests

Use Source Address Insertion

Enable TX VLAN Detection

Enable RX VLAN Detection

Ready latency: 0

**PMA Options 10GE/25GE**

PHY Reference Frequency: 156.250000 MHz

Enable custom rate

Include refclk mux

Include deterministic latency measurement interface

Select between 10G and 25G for Ethernet rate\*

Choose core variation

\* For the 100GE or 1 to 4 10GE/25GE with optional RSFEC and 1588 PTP variant, requires setting the **Active Channel at Startup** option on the IP tab to 10GE/25GE Channel

# Parameter Editor – Basic MAC Options

IP 100GE 10GE/25GE PMA\_Adaptation Example Design

▼ **General Options 100GE**

Select Ethernet Rate: 100G

Select Ethernet IP Layers: MAC+PCS+(528,514)RSFEC

▼ **MAC Options 100GE**

Basic 100GE Specialized 100GE

TX Maximum Frame Size: 518

RX Maximum Frame Size: 518

Enforce Maximum Frame Size

Choose Link Fault Generation Mode: Bidirectional

Stop TX traffic when link partner sends PAUSE?: No

Bytes to remove from RX frames: Remove CRC bytes

Forward RX Pause Requests

Use Source Address Insertion

Enable TX VLAN Detection

Enable RX VLAN Detection

Ready latency: 0

▼ **PMA Options 100GE**

PHY Reference Frequency: 156.250000 MHz

Choose the maximum frame size

Truncates packet to max RX frame size and increments oversized packets counter

If Unidirectional, in response to local fault, transmits remote fault ordered sets. No response to incoming remote fault ordered sets

Enables removal of CRC and CRC/PAD bytes form received frames before passing to RX MAC client

# Parameter Editor – Specialized MAC Options

IP 100GE 10GE/25GE PMA\_Adaptation Example Design

▼ **General Options 100GE**

Select Ethernet Rate: 100G

Select Ethernet IP Layers: MAC+PCS+(528,514)RSFEC

▼ **MAC Options 100GE**

Basic 100GE **Specialized 100GE**

Enable Preamble Passthrough

Enable strict preamble check

Enable strict SFD check

Average Inter-packet Gap: 12

Additional IPG removed per AM period: 0

▼ **PMA Options 100GE**

PHY Reference Frequency: 156.250000 MHz

← Preamble / start of frame delimiter sent to and received from core

← Protection against spurious start frames

← Interpacket gap control

# Parameter Editor – Example Design

IP 100GE 10GE/25GE PMA\_Adaptation **Example Design**

▼ **Available Example Designs**  
Select Design: Single instance of IP core ▼

▼ **Example Design Files**  
 Simulation  
 Synthesis

▼ **Generated HDL Format**  
Generate File Format: Verilog ▼

▼ **Target Development Kit**  
Select Board: Stratix 10 TX SI Development Kit - 1ST280EY2F55E2VG ▼

# Configuring the Intel<sup>®</sup> FPGA E-Tile Hard IP for Ethernet

Summary

# Configuring the Intel® FPGA E-Tile Hard IP for Ethernet - Summary

- The E-Tile Hard IP for Ethernet Intel® FPGA IP Core enables the Intel FPGA E-tiles for 10, 25 or 100G Ethernet operation
- The E-tile Hard IP for Ethernet Intel FPGA IP Parameter Editor allows for easy selection of all configurable Ethernet MAC, PCS and PMA options

# Intel® Stratix® 10 FPGA E-Tile Hard IP for Ethernet Resources

- Documentation
  - E-Tile Transceiver PHY User Guide
    - <https://www.intel.com/content/www/us/en/programmable/documentation/kqh1479167866037.html>

# Debugging with the Ethernet Toolkit



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# Debugging with the Ethernet Toolkit Objectives

Describe the features and functionality of the Ethernet Toolkit found in the Intel® Quartus® Prime Pro software

Set up and employ the Ethernet Toolkit to perform dynamic debugging and analysis on an Ethernet system

# Ethernet Toolkit

The Ethernet Toolkit is Intel® FPGA on-chip debugging tool for analyzing real-time status of Ethernet Intel FPGA IP

# Ethernet Toolkit

The Ethernet Toolkit is Intel® FPGA on-chip debugging tool for analyzing real-time status of Ethernet Intel FPGA IP

Runs on System Console platform

Interfaces with Ethernet IP through FPGA's JTAG connection

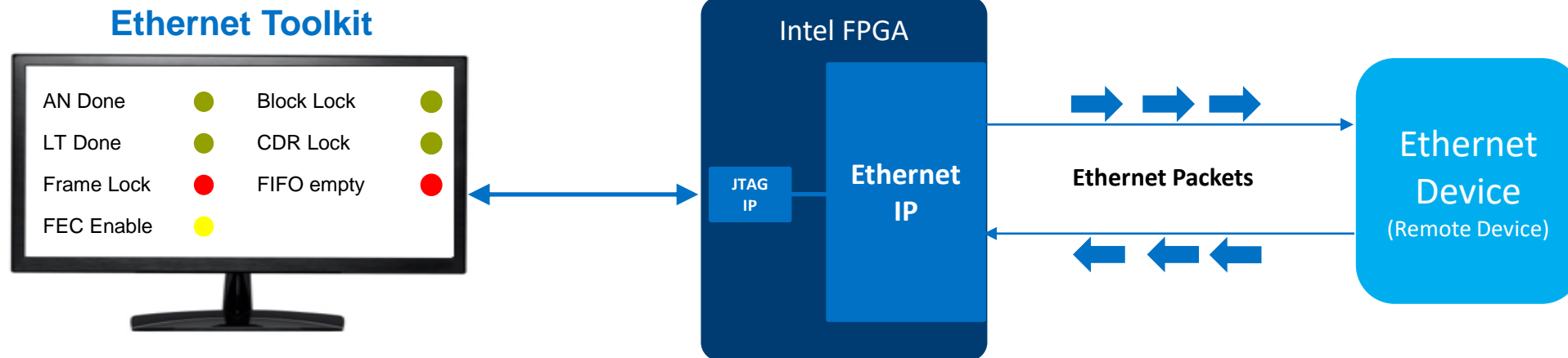
Continuously monitors IP functions through its registers

Provides graphical interface for accessing Ethernet IP and link information

\* For more details on using the System Console, see the online training entitled [System Console](#)

# Ethernet Toolkit Diagram

The Ethernet Toolkit is Intel® FPGA on-chip debugging tool for analyzing real-time status of Ethernet Intel FPGA IP



# Ethernet Toolkit Advantages

Real-time link updates

Register information decoded automatically

Lightweight

No need for additional equipment

Easy to use graphical interface

Free with Intel Quartus Prime Pro software

# Ethernet Toolkit User Functions

Verify link status

Assert MAC and channel resets

Read Ethernet IP status registers

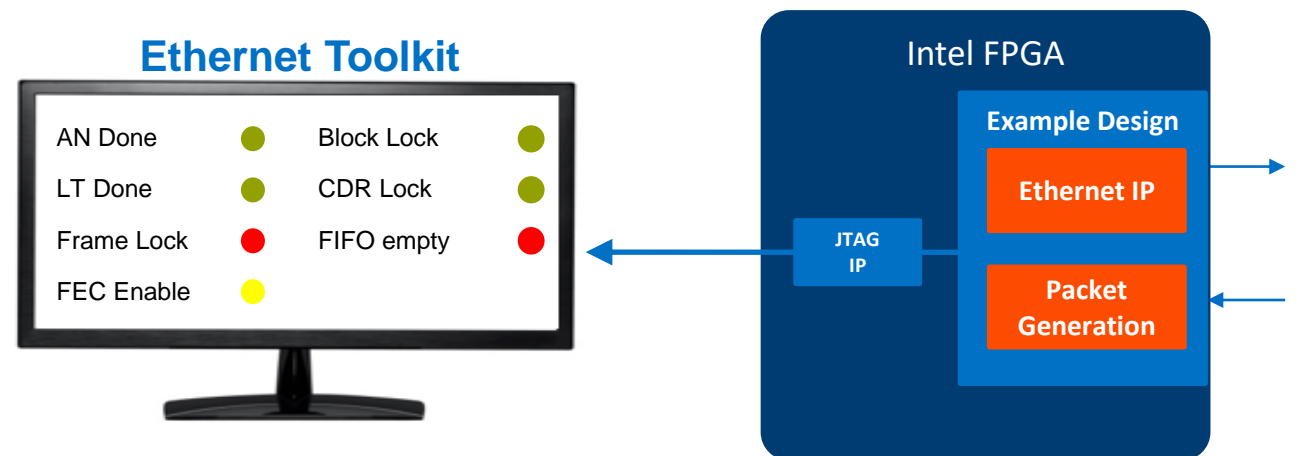
Read and Write Ethernet IP configuration registers

Read TX/RX channel statistics registers

# IP Example Design Ethernet Toolkit Support

Additional Ethernet Toolkit functionality enabled when example designs used

- Control packet generator/checker
- Run predefined test procedures
- Enable/disable MAC loopback
- Set source/destination MAC addresses



# Ethernet Toolkit, Software and IP Support – Intel® Stratix® 10 FPGAs

Supported Device Family	Transceiver Tile Type	IP Core Name	Data Rate(s) (Gbps)	Initial Software Version Support	Initial IP Version Support
Intel® Stratix® 10	L-Tile	10GBASE-KR PHY Intel® Stratix® 10 FPGA IP	10	20.1	19.1.0
		Low Latency 40G Ethernet Intel FPGA IP	40	20.1	19.1.0
		Low Latency 100G Ethernet Intel FPGA IP	100	20.1	19.1.1
	H-Tile	10GBASE-KR PHY Intel® Stratix® 10 FPGA IP	10	20.1	19.1.0
		Low Latency 40G Ethernet Intel FPGA IP	40	20.1	19.1.0
		Low Latency 100G Ethernet Intel FPGA IP	100	20.1	19.1.1
		H-Tile Hard IP for Ethernet Intel FPGA IP	100	20.1	19.2.0
	E-Tile	Low Latency E-Tile 40G Ethernet Intel FPGA IP	40	20.1	19.1.1
		E-Tile Hard IP for Ethernet Intel FPGA IP	10/25/100	20.1	19.3.0
Intel Stratix 10 GX 10M	H-Tile	Low Latency 40G for ASIC Proto Ethernet Intel FPGA IP	40	20.1	19.1.0

# Ethernet Toolkit, Software and IP Support – Intel® Agilex™ FPGAs

Supported Device Family	Transceiver Tile Type	IP Core Name	Data Rate(s) (Gbps)	Initial Software Version Support	Initial IP Version Support
Intel® Agilex™	H-Tile	Low Latency 100G Ethernet Intel FPGA IP	100	20.1	19.1.1
		H-Tile Hard IP for Ethernet Intel FPGA IP	100	20.1	19.2.0
	E-Tile	Low Latency E-Tile 40G Ethernet Intel FPGA IP	40	20.1	19.1.1
		E-Tile Hard IP for Ethernet Intel FPGA IP	10/25/100	20.1	19.3.0

\* Always check the latest [Ethernet Toolkit documentation](#) for current or additional IP and tile support.

# Debugging with the Ethernet Toolkit

Ethernet Toolkit Flow

# Ethernet Toolkit Flow

Set up the Ethernet Toolkit

Launch the Ethernet Toolkit

# Ethernet Toolkit Flow

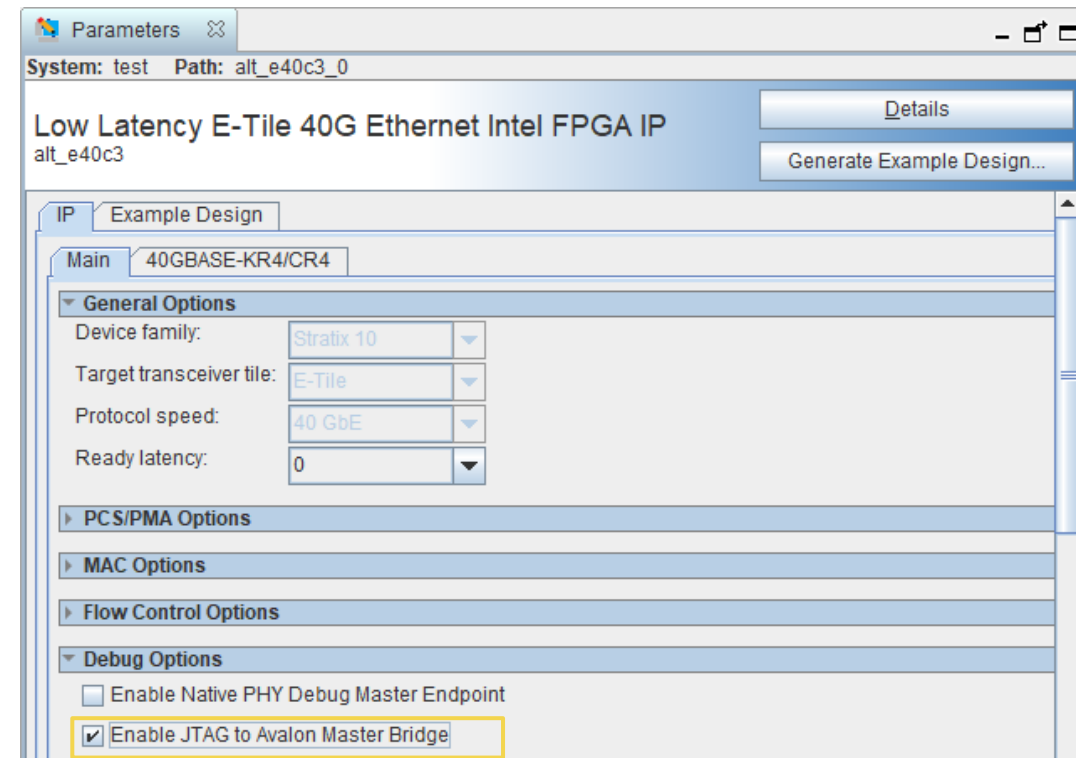
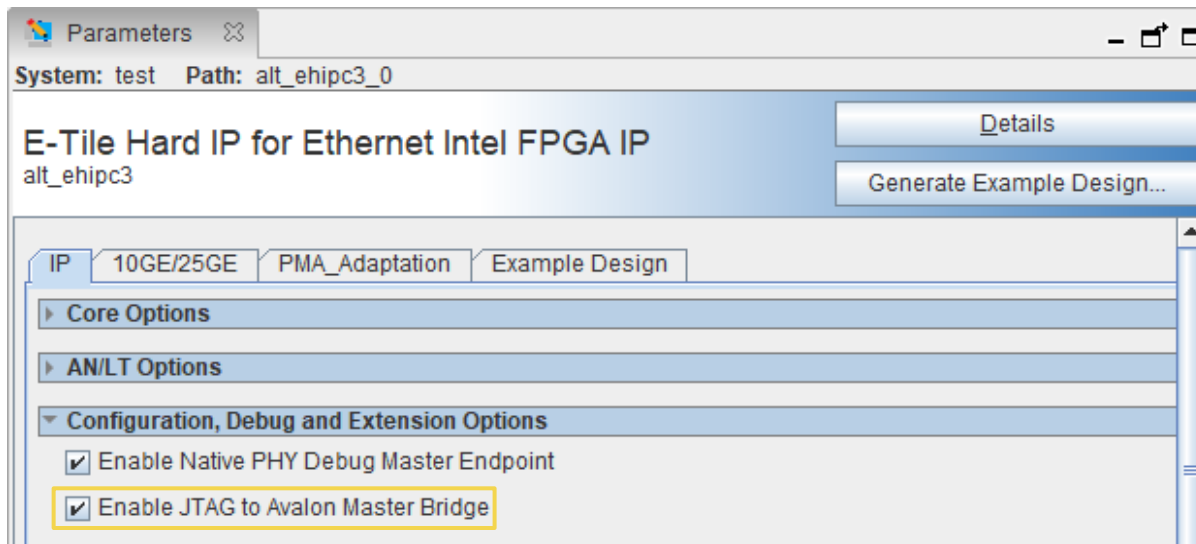
## Set up the Ethernet Toolkit

- Enable JTAG to Avalon Bridge
- Generate Ethernet IP example design (optional)
- Compile design and configure FPGA

## Launch the Ethernet Toolkit

# Enable JTAG to Avalon Bridge

Creates the logic necessary for the Ethernet Toolkit to perform memory accesses into the IP register space over JTAG



# Generate Ethernet IP Example Design (Optional)

Each Ethernet IP generates hardware ready example designs

The screenshot displays the 'E-Tile Ethernet IP for Intel Agilex FPGA' configuration window. The window title is 'System: test\_20\_3 Path: alt\_ehipc3\_fm\_0'. The main title is 'E-Tile Ethernet IP for Intel Agilex FPGA' with the instance name 'alt\_ehipc3\_fm'. A 'Details' button is located in the top right corner. Below the title bar, there are four tabs: 'IP', '10GE/25GE', 'PMA\_Adaptation', and 'Example Design'. A yellow callout box labeled 'Enable IP features' points to the 'Example Design' tab. The 'Example Design' section contains several expandable sections: 'Available Example Designs' with a 'Select Design:' dropdown set to 'Single instance of IP core'; 'Example Design Files' with checked checkboxes for 'Simulation' and 'Synthesis'; 'Generated HDL Format' with a 'Generate File Format:' dropdown set to 'Verilog'; and 'Target Development Kit' with a 'Select Board:' dropdown set to 'Agilex F-Series Transceiver-SoC Development Kit - AGFB014R24A2E2VR0'. A yellow callout box labeled 'Enable target board' points to this dropdown. In the top right corner, there is a 'Generate Example Design...' button, which is highlighted by a yellow callout box labeled 'Generate example design'.

# Ethernet Toolkit Flow

Set up the Ethernet Toolkit

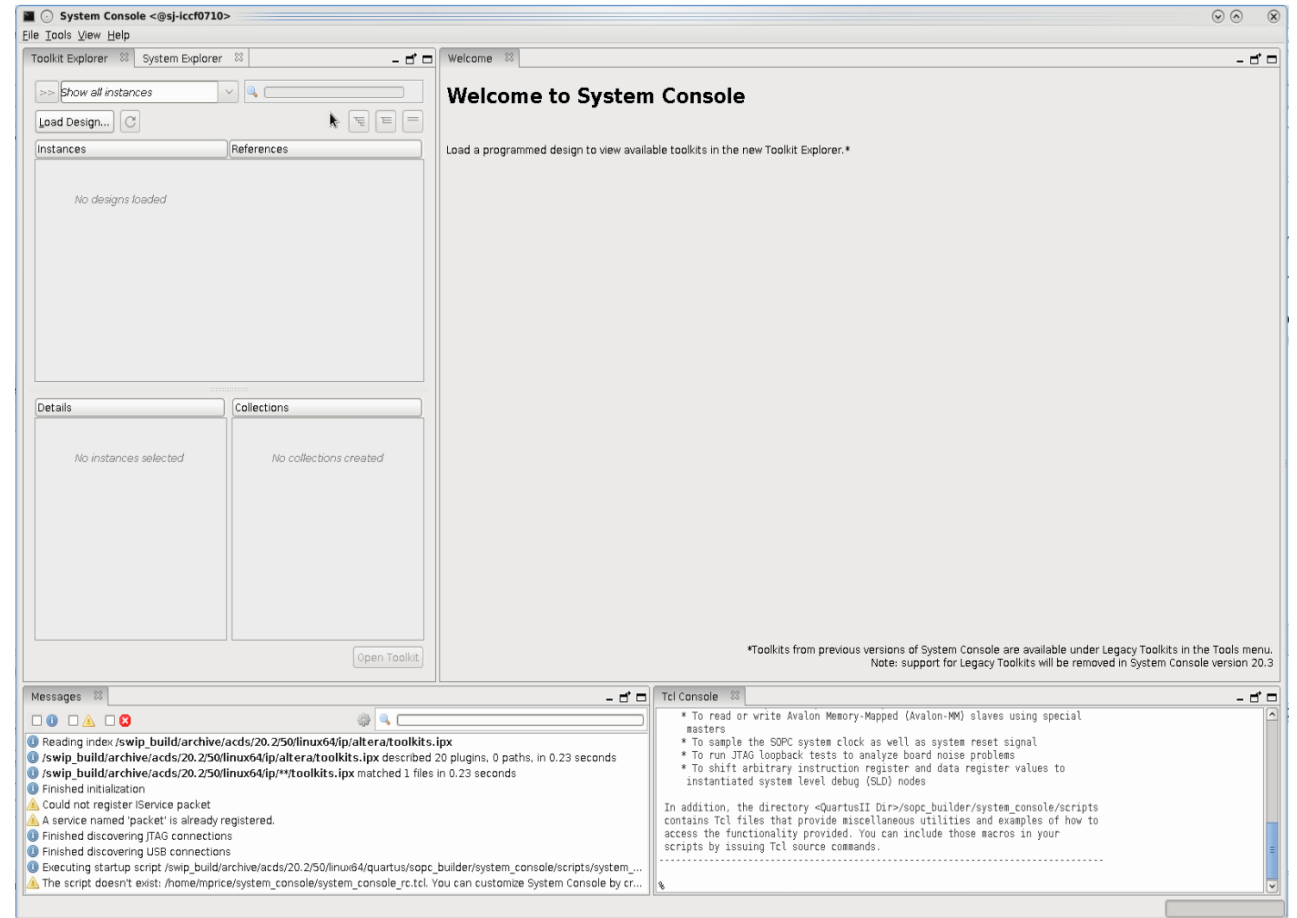
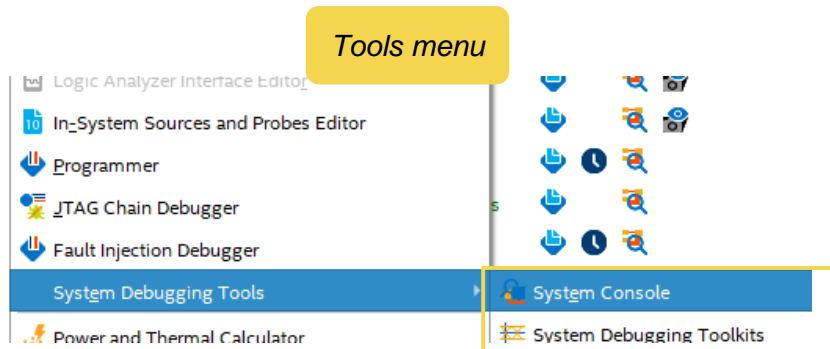
## Launch the Ethernet Toolkit

1. Launch System Console
2. Load Design
3. Select Ethernet IP instance for control and open Ethernet Toolkit
4. Run checks and tests

# 1. Launch System Console

## Open the System Console or System Debugging Toolkits

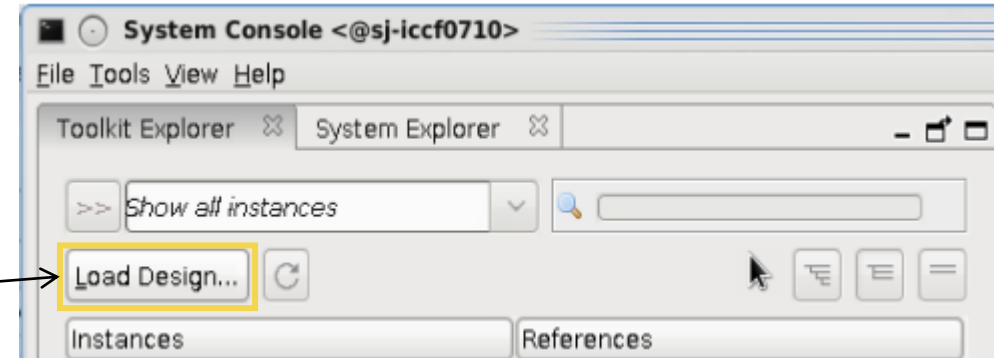
- Intel® Quartus® Prime Pro software  
Tools menu → System Debugging  
Tools submenu



## 2. Load Design

### Load your Ethernet IP design project(s) into System Console

- Click Load Design button
- Project will auto-load if Ethernet Toolkit is launched from Intel® Quartus® Prime Pro software with project open
- Load multiple projects if testing multiple interfaces/devices/boards

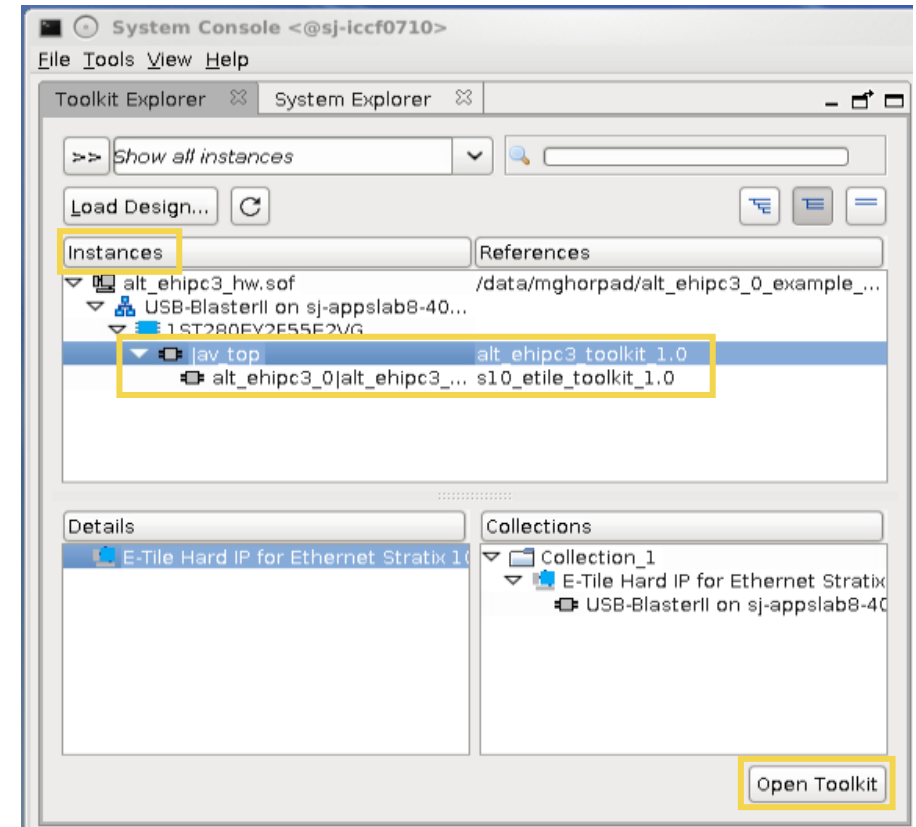


# 3. Select Ethernet IP instance for control and Open Toolkit

Supported Ethernet IP instances in design automatically recognized by System Console and listed in the Instances section

Select target Ethernet IP from list of IP instances

Click Open Toolkit



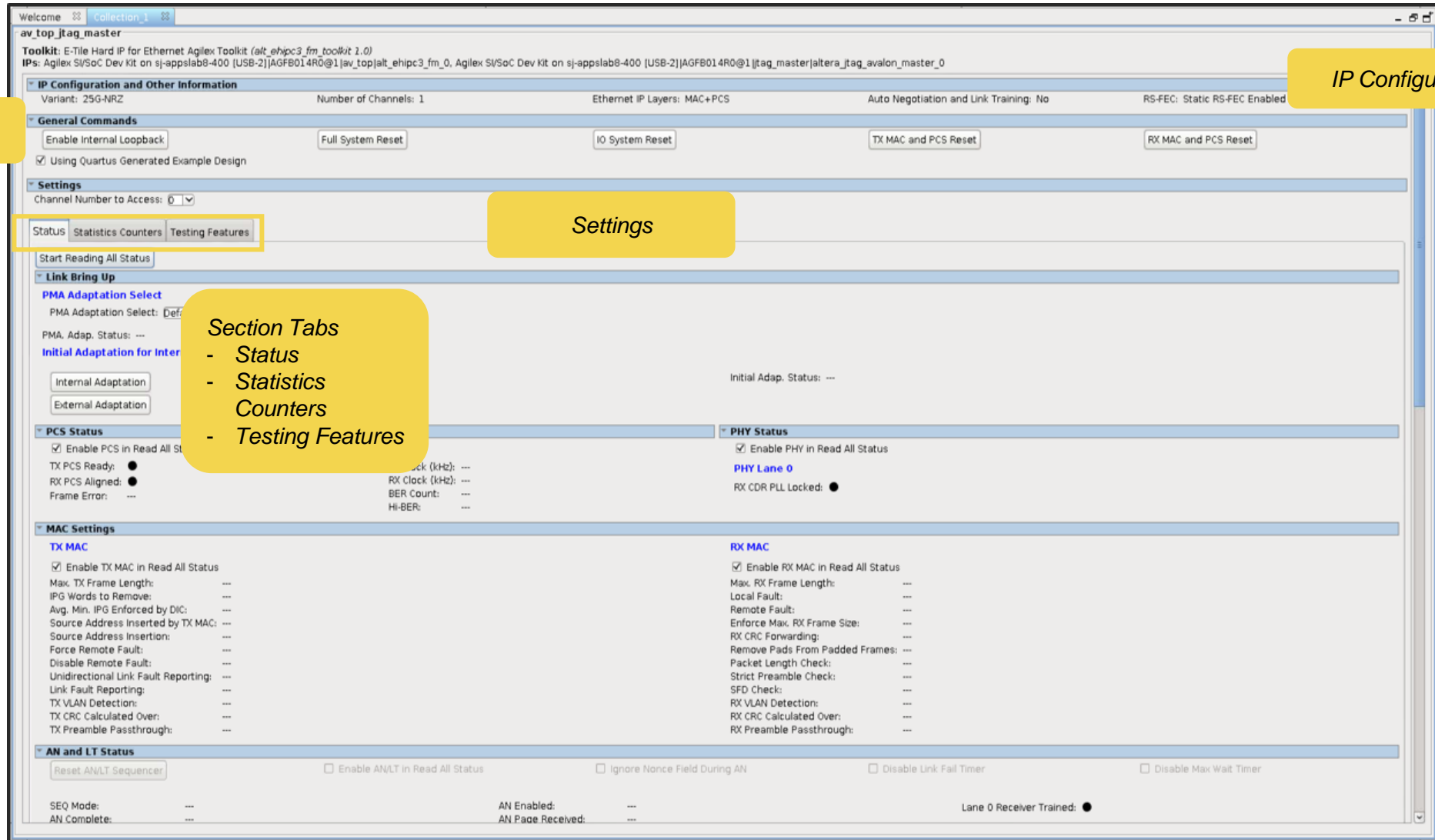
# 4. Run Checks and Tests

Use IP registers to interact with Ethernet IP components

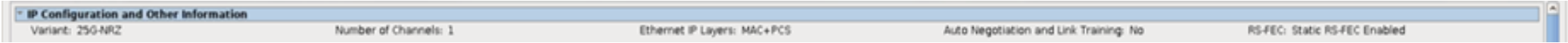
- Resets
- MAC
- PCS/PMA
- RS-FEC
- Auto Negotiation (AN) /Link Training (LT) logic

\* Available information changes based on IP core variation and IP options enabled.

# Ethernet Toolkit User Interface



# IP Configuration



## Verify IP settings

- IP core variant
- IP Ethernet components and features enabled

# General Commands

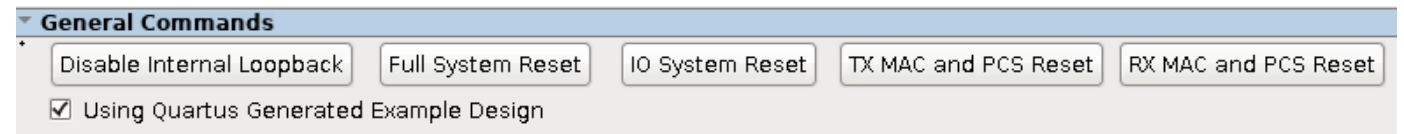
Enable/disable loopback

System reset

Reset

- PMA
- TX MAC and PCS
- RX MAC and PCS

Enable example design control



# Settings

▼ **Settings**  
Channel Number to Access:  ▼

Select the channel number within Ethernet IP for register access

# Status Tab

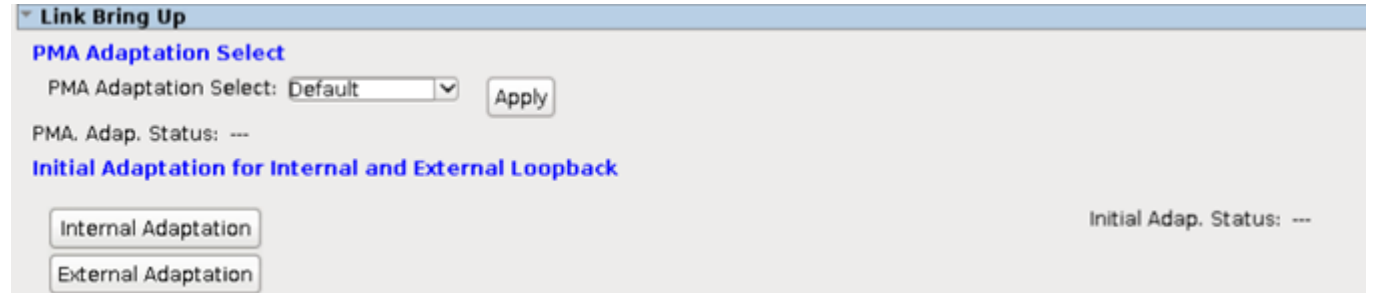
The screenshot displays the 'av\_top\_jtag\_master' web interface. At the top, there is a 'Welcome' message and a 'Collection\_1' tab. Below this, the 'IP Configuration and Other Information' section shows details like 'Variant: 25G-NRZ', 'Number of Channels: 1', 'Ethernet IP Layers: MAC+PCS', 'Auto Negotiation and Link Training: No', and 'RS-FEC: Static RS-FEC Enabled'. The 'General Commands' section includes buttons for 'Enable Internal Loopback', 'Full System Reset', 'IO System Reset', 'TX MAC and PCS Reset', and 'RX MAC and PCS Reset'. A checkbox for 'Using Quartus Generated Example Design' is checked. The 'Settings' section has a 'Channel Number to Access' dropdown set to '0'. The 'Status' tab is highlighted with a yellow box. Below it, a 'Start Reading All Status' button is visible. The 'Link Bring Up' section features a 'PMA Adaptation Select' dropdown set to 'Default' and an 'Apply' button. Below this, 'PMA, Adap. Status: ---' and 'Initial Adaptation for Internal and External Loopback' are shown, with buttons for 'Internal Adaptation' and 'External Adaptation'. The 'PCS Status' section includes a checked 'Enable PCS in Read All Status' checkbox and indicators for 'TX PCS Ready', 'RX PCS Aligned', and 'Frame Error'. The 'PHY Status' section has a checked 'Enable PHY in Read All Status' checkbox, 'PHY Lane 0', and an 'RX CDR PLL Locked' indicator. The 'MAC Settings' section is split into 'TX MAC' and 'RX MAC'. 'TX MAC' has a checked 'Enable TX MAC in Read All Status' checkbox and various parameters like 'Max. TX Frame Length', 'IPG Words to Remove', etc. 'RX MAC' has a checked 'Enable RX MAC in Read All Status' checkbox and parameters like 'Max. RX Frame Length', 'Local Fault', etc. The 'AN and LT Status' section at the bottom includes a 'Reset AN/LT Sequencer' button and checkboxes for 'Enable AN/LT in Read All Status', 'Disable Link Fail Timer', and 'Disable Max Wait Timer'. It also shows 'SEQ Mode' and 'AN Complete' indicators. Several yellow callout boxes are overlaid on the interface: 'Link Bring Up' near the PMA Adaptation Select dropdown, 'PCS Status' near the TX PCS Ready indicator, 'PHY Status' near the RX CDR PLL Locked indicator, 'TX MAC Settings' near the TX MAC section, 'RX MAC Settings' near the RX MAC section, and 'AN and LT Status' near the AN Complete indicator.

# Link Bring Up

Select adaptation mode

View adaptation status

Select internal or external adaptation



The screenshot shows a configuration panel titled "Link Bring Up". It contains the following elements:

- PMA Adaptation Select**: A section header.
- PMA Adaptation Select:** A dropdown menu currently set to "Default", followed by an "Apply" button.
- PMA. Adap. Status:** A status indicator showing "---
- Initial Adaptation for Internal and External Loopback**: A section header.
- Internal Adaptation**: A button.
- External Adaptation**: A button.
- Initial Adap. Status:** A status indicator showing "---

# PCS/PHY Status

Read current values of PHY and PCS registers

Enable/disable RX/TX Read All Status

- Reads IP registers at regular interval

Status indicators

- Locked PLLs
- RX word alignment
- TX/RX clock frequencies
- RX frame error count
- RX Bit error rate (BER) count

**PCS Status**

Enable PCS in Read All Status

TX PCS Ready:	●	TX Clock (kHz):	402840
RX PCS Aligned:	●	RX Clock (kHz):	402840
Frame Error:	0x00000000	BER Count:	0
		Hi-BER:	Not Detected

**PHY Status**

Enable PHY in Read All Status

<b>PHY Lane 0</b>		<b>PHY Lane 1</b>	
RX CDR PLL Locked:	●	RX CDR PLL Locked:	●
<b>PHY Lane 2</b>		<b>PHY Lane 3</b>	
RX CDR PLL Locked:	●	RX CDR PLL Locked:	●

# MAC Settings

Read current values of MAC registers

Enable/disable RX/TX Read All Status

View current MAC settings

- Maximum frame length
- Fault detection and reporting
- CRC calculation
- Packet length checking

MAC Settings	
<b>TX MAC</b>	
<input checked="" type="checkbox"/> Enable TX MAC in Read All Status	
Max. TX Frame Length:	1518
IPG Words to Remove:	20
Avg. Min. IPG Enforced by DIC:	12 bytes
Source Address Inserted by TX MAC:	0x1122334455
Source Address Insertion:	Client provides source address
Force Remote Fault:	Disabled
Disable Remote Fault:	Disabled
Unidirectional Link Fault Reporting:	Disabled
Link Fault Reporting:	Enabled
TX VLAN Detection:	Enabled
TX CRC Calculated Over:	Ethernet Frame
TX Preamble Passthrough:	Disabled
<b>RX MAC</b>	
<input checked="" type="checkbox"/> Enable RX MAC in Read All Status	
Max. RX Frame Length:	1518
Local Fault:	Not Detected
Remote Fault:	Not Detected
Enforce Max. RX Frame Size:	Oversized Frames not Altered
RX CRC Forwarding:	Disabled
Remove Pads From Padded Frames:	Disabled
Packet Length Check:	Disabled
Strict Preamble Check:	Disabled
SFD Check:	Disabled
RX VLAN Detection:	Enabled
RX CRC Calculated Over:	Ethernet Frame
RX Preamble Passthrough:	Disabled

# Statistics Counters Tab

The screenshot displays the 'av\_top\_jtag\_master' web interface. The main content area is divided into several sections:

- IP Configuration and Other Information:** Shows variant '25G-NRZ', 1 channel, Ethernet IP Layers (MAC+PCS), and RS-FEC (Static RS-FEC Enabled).
- General Commands:** Includes buttons for 'Full System Reset', 'IO System Reset', 'TX MAC and PCS Reset', and 'RX MAC and PCS Reset'.
- Settings:** Features a 'Channel Number to Access' dropdown set to 0.
- Statistics Counters:** A yellow box highlights this tab, which is currently selected.
- Example Design Packet Generator Settings:** Contains 'Packet Generator Modes' (e.g., 'Random Mode - Random Gap'), 'Packet Byte Size' fields, and 'Source and Destination Addresses'.
- Transmitter and Receiver Statistics:** A yellow box highlights this section, which includes a table of statistics and buttons to 'Start Reading' and 'Reset' statistics for both transmitter and receiver.
- RS-FEC:** A yellow box highlights this section, showing 'Dynamic RS-FEC' controls and 'RS-FEC Statistics'.

Statistics Counters Names	TX Statistics	RX Statistics
Frames < 64 bytes with CRC error	0	0
Oversized frames with CRC error	0	0
Packets with FCS errors	0	0
Frames >= 64 bytes with CRC error	0	0
Multicast data frames with CRC error	0	0
Broadcast data frames with CRC error	0	0
Unicast data frames with CRC error	0	0
Multicast control frames with CRC error	0	0
Broadcast control frames with CRC error	0	0
Unicast control frames with CRC error	0	0
Pause frames with CRC error	0	0
64 Byte Frames (includes CRC field)	0	0
65 - 127 Byte Frames	0	0
128 - 255 Byte Frames	0	0
256 - 511 Byte Frames	0	0
512 - 1023 Byte Frames	0	0
1024 - 1518 Byte Frames	0	0
1519 - MAX Size Frames	0	0
Oversized Frames (> MAX Size)	0	0
Multicast data frames without error	0	0

# Example Design Packet Generator Settings (Statistics Counters Tab)

Available when using design example generated by Ethernet IP core

Enable/disable MAC loopback

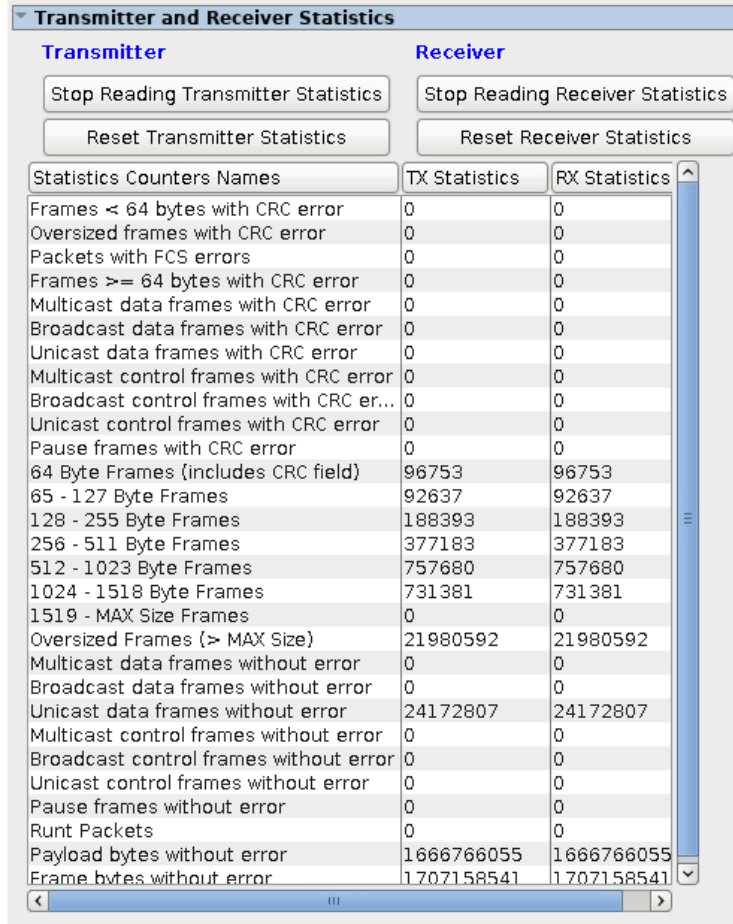
Start/stop packet generation

Choose pattern (random, fixed size and incremental)

Set source and destination MAC addresses

The screenshot displays the 'Example Design Packet Generator Settings' window. It is divided into two main sections. The left section, titled 'Packet Generator Modes', contains a checkbox for 'MAC Loopback Mode' which is unchecked. Below it, 'Packet Generator Mode' is set to 'Random Mode - Random Gap'. There are input fields for 'Packet Byte Size - Begin' and 'Packet Byte Size - End', both containing the value '0'. A 'Total Number of Packets' field also contains '0'. A 'Start Packet Generator' button is present at the bottom of this section. A note at the bottom left states: 'Note: The range of packet sizes is 64 to 9600, and that of the number of packets is 1 to 2147483647.' The right section, titled 'Source and Destination Addresses', has two columns. The first column shows 'New Source Address' as '0x000000000000' and 'Source Address' as '0x876543210ADD', with a 'Set Source Address' button. The second column shows 'New Destination Address' as '0x000000000000' and 'Destination Address' as '0x123456780ADD', with a 'Set Destination Address' button. A note at the bottom of this section reads: 'Note: Source and Dest. Address Range: 0x0 to 0xFFFFFFFF'.

# TX and RX Statistics



The screenshot shows a window titled "Transmitter and Receiver Statistics" with two main sections: "Transmitter" and "Receiver". Each section has buttons for "Stop Reading" and "Reset" statistics. Below these is a table with three columns: "Statistics Counters Names", "TX Statistics", and "RX Statistics". The table lists various frame sizes and error types with their corresponding counts for both TX and RX.

Statistics Counters Names	TX Statistics	RX Statistics
Frames < 64 bytes with CRC error	0	0
Oversized frames with CRC error	0	0
Packets with FCS errors	0	0
Frames >= 64 bytes with CRC error	0	0
Multicast data frames with CRC error	0	0
Broadcast data frames with CRC error	0	0
Unicast data frames with CRC error	0	0
Multicast control frames with CRC error	0	0
Broadcast control frames with CRC er...	0	0
Unicast control frames with CRC error	0	0
Pause frames with CRC error	0	0
64 Byte Frames (includes CRC field)	96753	96753
65 - 127 Byte Frames	92637	92637
128 - 255 Byte Frames	188393	188393
256 - 511 Byte Frames	377183	377183
512 - 1023 Byte Frames	757680	757680
1024 - 1518 Byte Frames	731381	731381
1519 - MAX Size Frames	0	0
Oversized Frames (> MAX Size)	21980592	21980592
Multicast data frames without error	0	0
Broadcast data frames without error	0	0
Unicast data frames without error	24172807	24172807
Multicast control frames without error	0	0
Broadcast control frames without error	0	0
Unicast control frames without error	0	0
Pause frames without error	0	0
Runt Packets	0	0
Payload bytes without error	1666766055	1666766055
Frame bytes without error	1707158541	1707158541

View current value of statistical counter registers

Enable/disable reading RX/TX statistical registers

- Reads IP registers at regular interval

Reset the counter values

# RS-FEC

View and write RS-FEC register values

Enable/disable RS-FEC

Perform error injection

Enable/disable reading RS-FEC statistical registers

Reset RS-FEC statistical registers

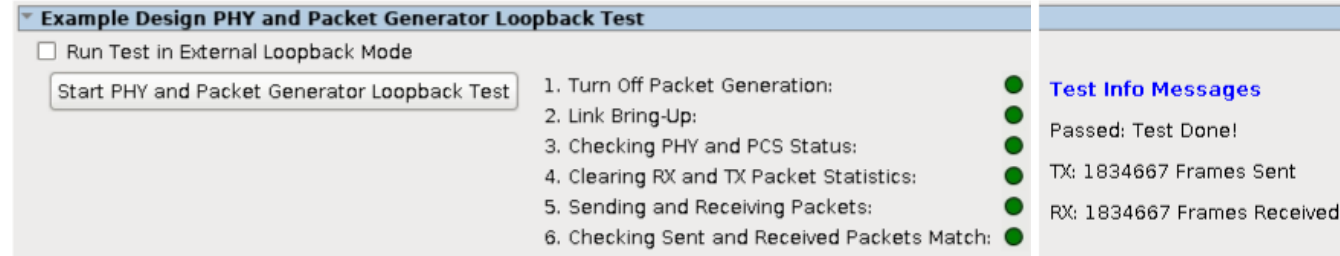
The screenshot displays the RS-FEC configuration interface. It is organized into several sections:

- Dynamic RS-FEC:** Contains a "Disable RS-FEC" button.
- Error Insertion:** This section is divided into four lanes (Lane 0, Lane 1, Lane 2, Lane 3). Each lane has:
  - Rate (Range: 0x00 - 0xFF): Input field with value 0x00.
  - Pattern (Range: 0x00 - 0xFF): Input field with value 0x00.
  - Start Error Injection button.
- RS-FEC Statistics:** Contains two buttons: "Start Reading RS-FEC Statistics" and "Reset RS-FEC Statistics". Below these buttons, the following statistics are shown:
  - Corrected Codewords: 0
  - Uncorrected Codewords: 0
- Lane Statistics:** Below the statistics section, there are four rows corresponding to Lane 0, Lane 1, Lane 2, and Lane 3. Each row displays three values:
  - Corr. Symbols: 0
  - Corr. Bits 0 to 1: 0
  - Corr. Bits 1 to 0: 0

# Testing Features Tab

The screenshot displays the 'av\_top\_itag\_master' web interface. At the top, it shows 'Welcome' and 'Collection\_1'. Below this, the 'IP Configuration and Other Information' section lists details like 'Variant: 25G-NRZ', 'Number of Channels: 1', 'Ethernet IP Layers: MAC+PCS', 'Auto Negotiation and Link Training: No', and 'RS-FEC: Static RS-FEC Enabled'. The 'General Commands' section includes buttons for 'Enable Internal Loopback', 'Full System Reset', 'IO System Reset', 'TX MAC and PCS Reset', and 'RX MAC and PCS Reset'. A checkbox for 'Using Quartus Generated Example Design' is checked. The 'Settings' section has a 'Channel Number to Access' dropdown set to '0'. Below this, there are tabs for 'Status', 'Statistics Counter', and 'Testing Features', with the latter being highlighted. The 'Testing Features' section is titled 'Example Design PHY and Packet Generator Loopback Test' and contains a 'Run Test in External Loopback Mode' checkbox, a 'Start PHY and Packet Generator Loopback Test' button, and a progress indicator with six steps: 1. Turn Off Packet Generation, 2. Link Bring-Up, 3. Checking PHY and PCS Status, 4. Clearing RX and TX Packet Statistics, 5. Sending and Receiving Packets, and 6. Checking Sent and Received Packets Match. A yellow callout box points to this section with the text 'Example Design PHY and Packet Generator Loopback Test'. To the right, there is a 'Test Info Messages' section with the text 'Press Start to Run the Test'. Below the test section are 'Read Register' and 'Write to Register' sections. The 'Read Register' section has a 'Register Address' field with '0x00000000', a 'Value Read' field with '0x0', and a 'Read Value' button. A yellow callout box labeled 'Read Register' points to this section. The 'Write to Register' section has a 'Register Address' field with '0x00000000', a 'Value to Write' field with '0x00000000', and a 'Write Value' button. A yellow callout box labeled 'Write Register' points to this section.

# Example Design PHY and Packet Generator Loopback Test



The screenshot shows a software interface for a loopback test. At the top, there is a title bar: "Example Design PHY and Packet Generator Loopback Test". Below the title bar, there is a checkbox labeled "Run Test in External Loopback Mode" which is currently unchecked. To the right of the checkbox is a button labeled "Start PHY and Packet Generator Loopback Test". Below the button, there is a list of six test steps, each followed by a green circular indicator:

1. Turn Off Packet Generation: ●
2. Link Bring-Up: ●
3. Checking PHY and PCS Status: ●
4. Clearing RX and TX Packet Statistics: ●
5. Sending and Receiving Packets: ●
6. Checking Sent and Received Packets Match: ●

To the right of the list, there is a section titled "Test Info Messages" in blue text. Below this title, the following messages are displayed:

- Passed: Test Done!
- TX: 1834667 Frames Sent
- RX: 1834667 Frames Received

Available when using design example generated by Ethernet IP core

Perform sanity check on link

Run loopback test using internal or external loopback

Must disable MAC loopback

# Write to/Read Register

Directly access registers not visible in Ethernet Toolkit UI

Enter exact register full 32-bit address

- User must manually calculate address when given base address plus register offset
- Designer must be aware of register availability and content
- Avoid reading or writing to undefined registers

**Write to Register**

Register Address:  Write Value

Value to Write:

Last value written: 0x0 to Reg. Address: 0x0

**Read Register**

Register Address:  Read Value

Value Read: 0x0

# Debugging with the Ethernet Toolkit

## Summary

# Debugging with the Ethernet Toolkit – Summary

Ethernet Toolkit is available in the Intel® Quartus® Prime Pro software and is easily enabled in your designs using Ethernet Intel FPGA IP cores

Ethernet Toolkit provides the critical visibility and control you need when analyzing and debugging designs using Ethernet Intel FPGA IP

# Resources

## Ethernet IP – Support Center

- <https://www.intel.com/content/www/us/en/programmable/support/support-resources/support-centers/ethernet-support.html>

## Ethernet Toolkit User Guide

- <https://www.intel.com/content/www/us/en/programmable/documentation/nrb1596652301528.html>

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