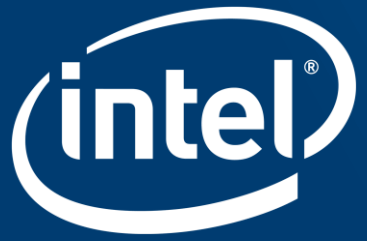


# Configuring the Intel® FPGA E-Tile Hard IP for Ethernet

# Configuring the Intel® FPGA E-Tile Hard IP for Ethernet - Objective and Agenda

Describe the method for configuring the features and functionality of the Hard IP for Ethernet found in Intel® FPGA E-Tiles

- Overview and hard IP features
- Parameterizing the IP

# Prerequisites

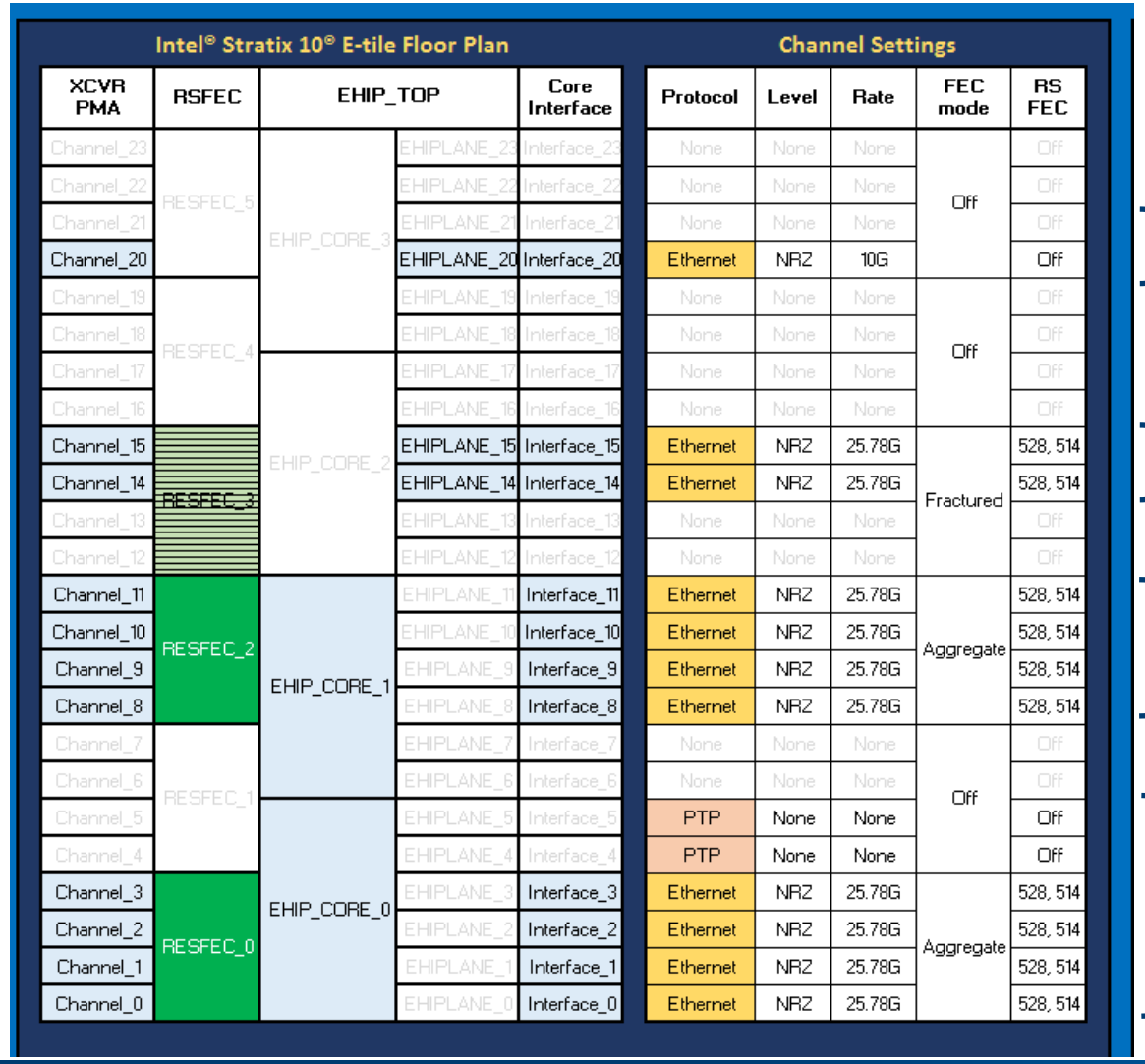
- Understanding of the Ethernet protocols
- Understanding of the FPGA design flow
- Familiarity with the Intel® FPGA E-tile and Hard IP for Ethernet architecture
  - Documentation:  E-Tile Transceiver PHY User Guide
    - https://www.intel.com/content/www/us/en/programmable/documentation/kqh1479167866037.html
  - Online training:  Intel® FPGA E-Tile Transceiver Basics
    - https://www.intel.com/content/www/us/en/programmable/support/training/course/os101116.html

# E-Tile Hard IP for Ethernet Intel® FPGA IP Core

The E-Tile Hard IP for Ethernet IP Core supports full and partial configurations of the following variants

- Single channel **10GE/25GE**
- 1 – 4 channels **10GE/25GE** with optional Reed-Solomon Forward Error Correction (RS-FEC)
- **100GE** with optional RS-FEC
- **100GE** or 1 – 4 channels **10GE/25GE** with optional RS-FEC and optional 1588 Precision Time Protocol (PTP)
- Custom PCS with optional RS-FEC

# Ethernet Hard IP Use model




Variant A: Single 10GE/25GE

Variant B: 1 to 4 10GE/25GE with optional RS-FEC

Variant C: 100GE with optional RS-FEC

Variant D: 100GE or 1 to 4 10GE/25GE with optional RS-FEC and optional PTP (6 channels total

# E-Tile Ethernet Protocol Support

| IP Version | Protocol | Details |
|---|---|---|
| 100GE | 100GBASE-KR4 | 4 x 25.78125 Gbps non-return-to-zero (NRZ) for copper backplane |
| | 100GBASE-CR4 | 4 x 25.78125 Gbps NRZ for Direct Attach Copper Cable |
| | CAUI-4 | 4 x 25.78125 Gbps NRZ lanes for Low Loss Links: Chip-to-Chip or Chip-to-Module |
| | CAUI-2 | 2 x 53.125 Gbps PAM4 lanes for Low Loss Links: Chip-to-Chip, Chip-to-Module, and DAC |
| 25GE | 25GBASE-KR | 1 x 25.78125 Gbps lane for Backplane |
| | 25GBASE-CR | 1 x 25.78125 Gbps lane for Direct Attach Copper Cable |
| | 25GBASE-R AUI | 1 x 25.78125 Gbps lane for Low Loss Connections to External PHY Modules |
| | 25GBASE-R Consortium Link | 1 x 25.78125 Gbps lane based on the 25G/50G Consortium Specification |
| 10GE | 10GBASE-KR | 1 x 10.3125 Gbps lane for Backplane |
| | 10GBASE-CR | 1 x 10.3125 Gbps lane for Direct Attach Copper Cable |

# Example E-Tile Hard IP for Ethernet IP Core Features

- Optional auto negotiation and/or link training logic
- Optional 1588v2 PTP
- RS-FEC(528,514) and RS-FEC(544,514) support for 25G and 100G Ethernet
- Frame structure control such as jumbo packet and interpacket gap (IPG) length
- Frame monitoring and statistics control such as link fault detection and reporting and CRC checking and error reporting
- Serial PMA and parallel loop-back support for self-diagnostic testing
- Interface for reading and controlling internal management registers

# Core Implementation Variations

Available on all IP core variants except Custom PCS with optional RS-FEC

- MAC and PCS
- PCS only
- Flexible Ethernet (FlexE)
- Optical Transport Network (OTN)

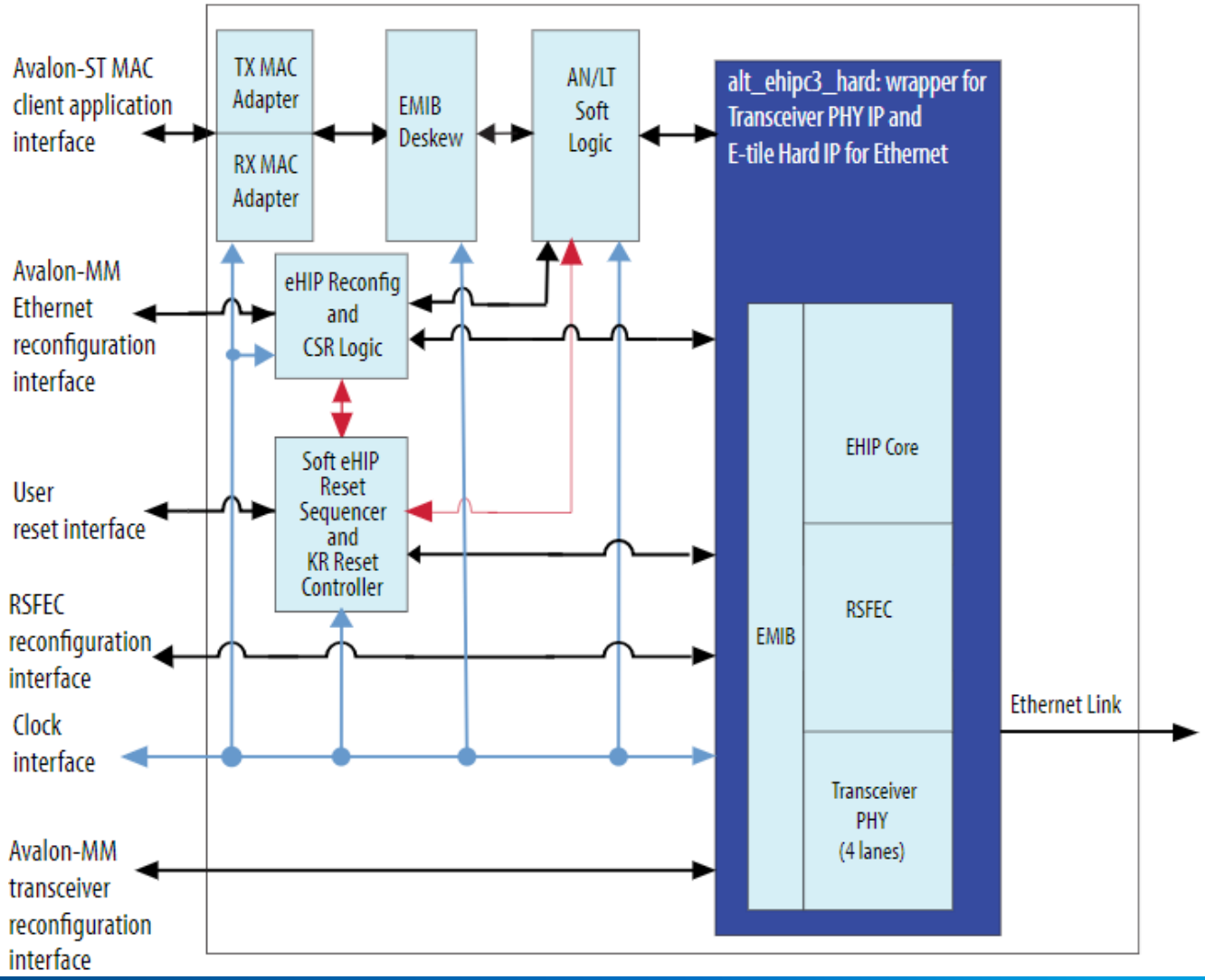
- E-tile transceivers used for PMA/PMD in all implementations

# E-tile Hard IP for Ethernet Block Diagram

The E-tile Ethernet IP consist of both hard (on-tile) and soft (in FPGA) logic

- Hard logic
  - MAC/PCS/PMA
  - RS-FEC
  - PTP
- Soft logic
  - Auto-negotiation and link training logic
  - Reset controller and sequencer
  - Reconfiguration and CSR logic
  - RX and TX adapters

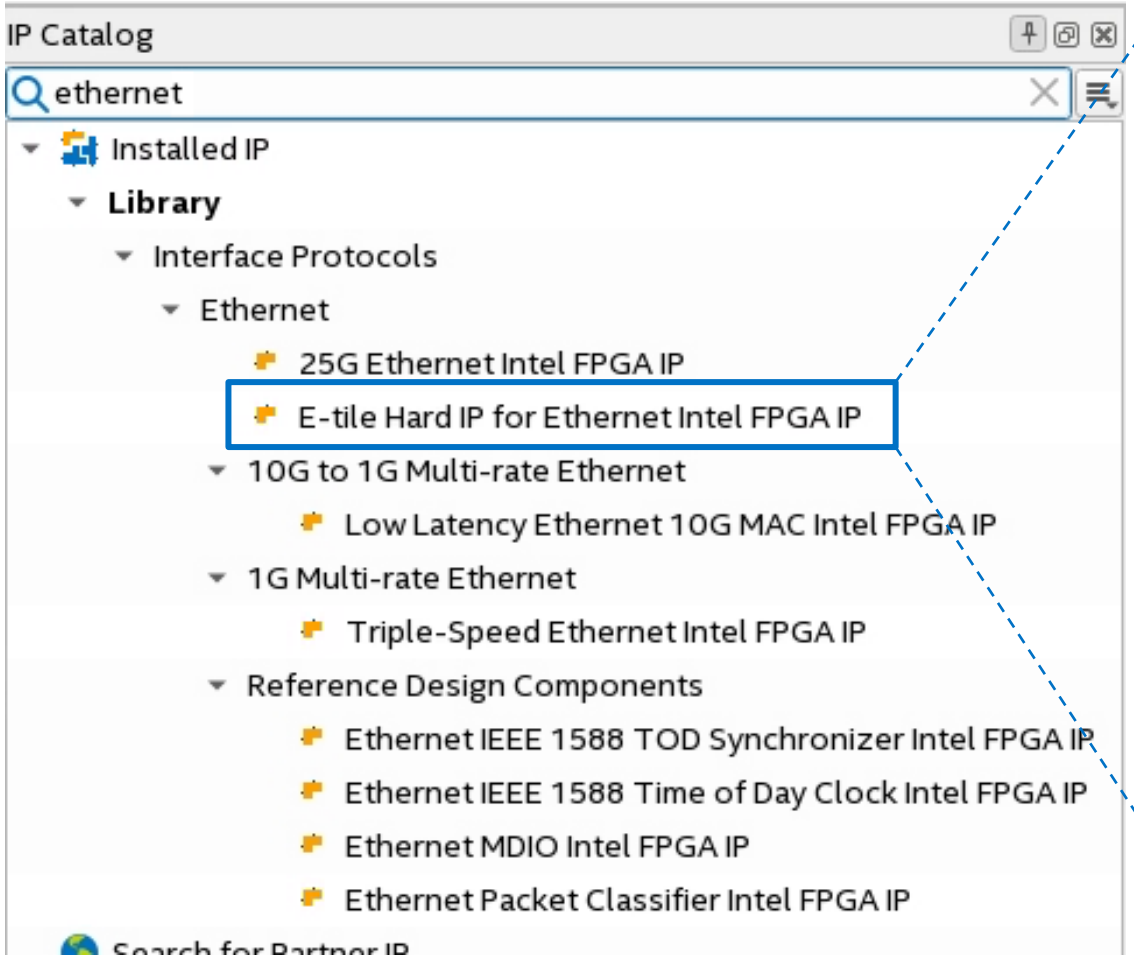
*Example 100GE with RS-FEC Block Diagram*

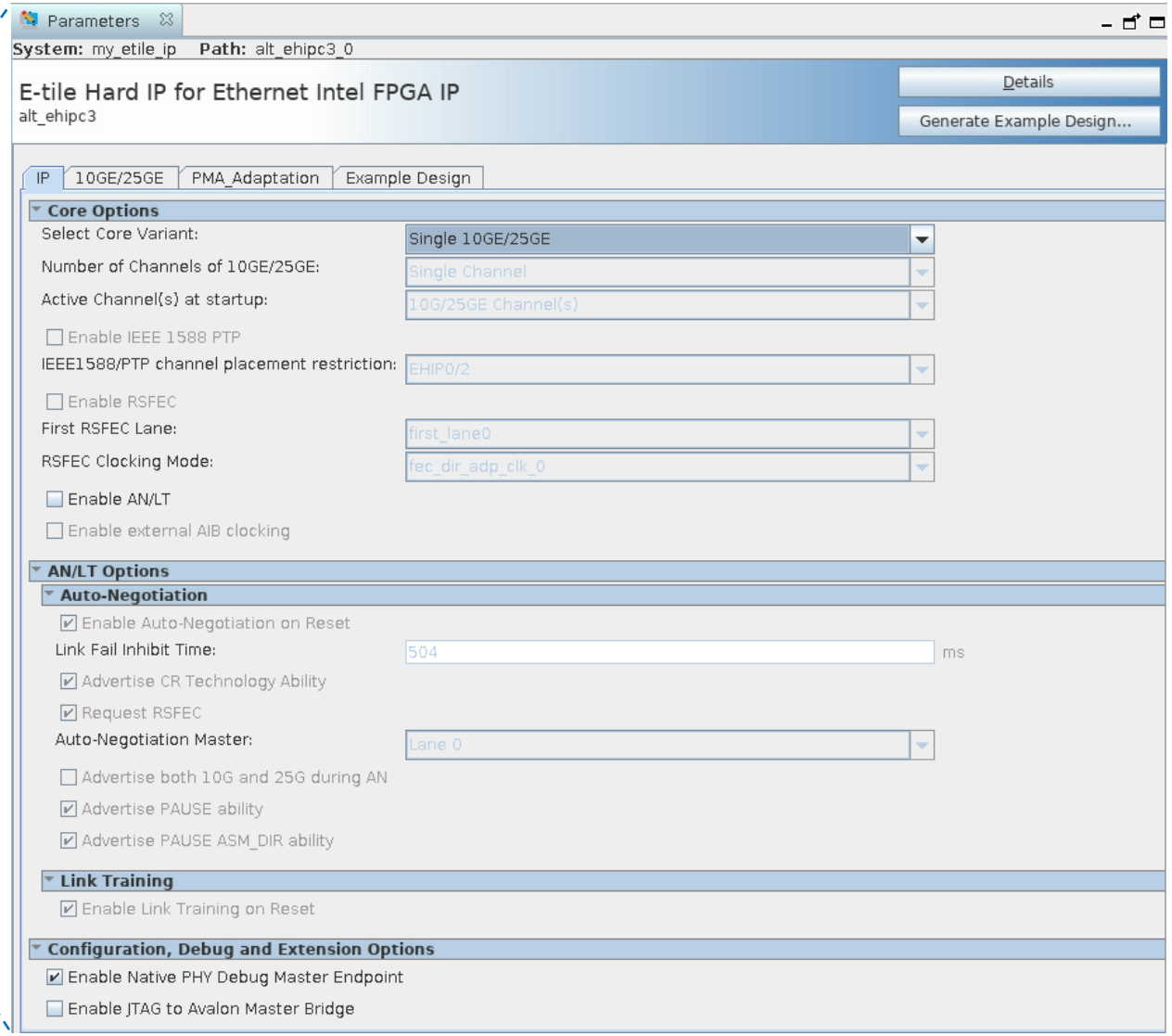


# Configuring the Intel® Stratix® 10 FPGA E-Tile Hard IP for Ethernet

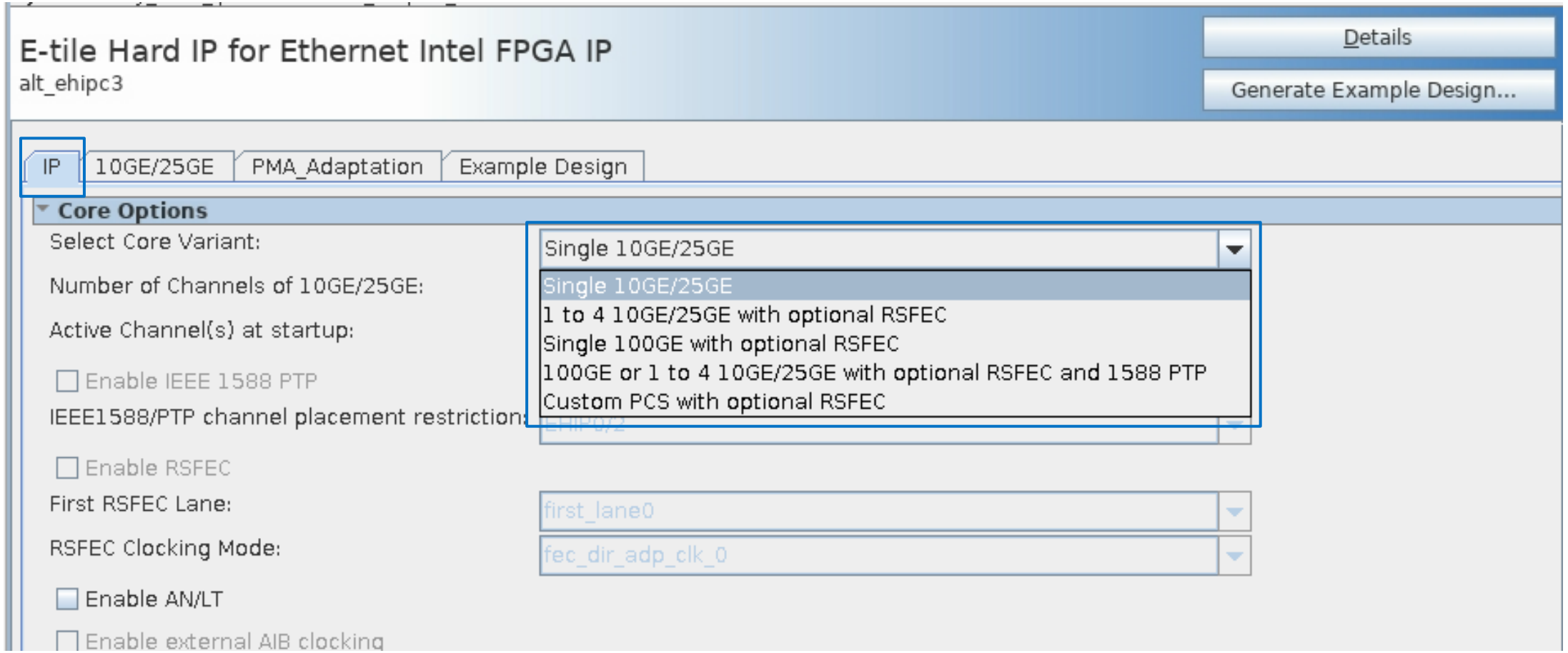
Parameterizing the E-Tile Hard IP for Ethernet

# E-tile Hard IP for Ethernet IP Intel FPGA Parameter Editor

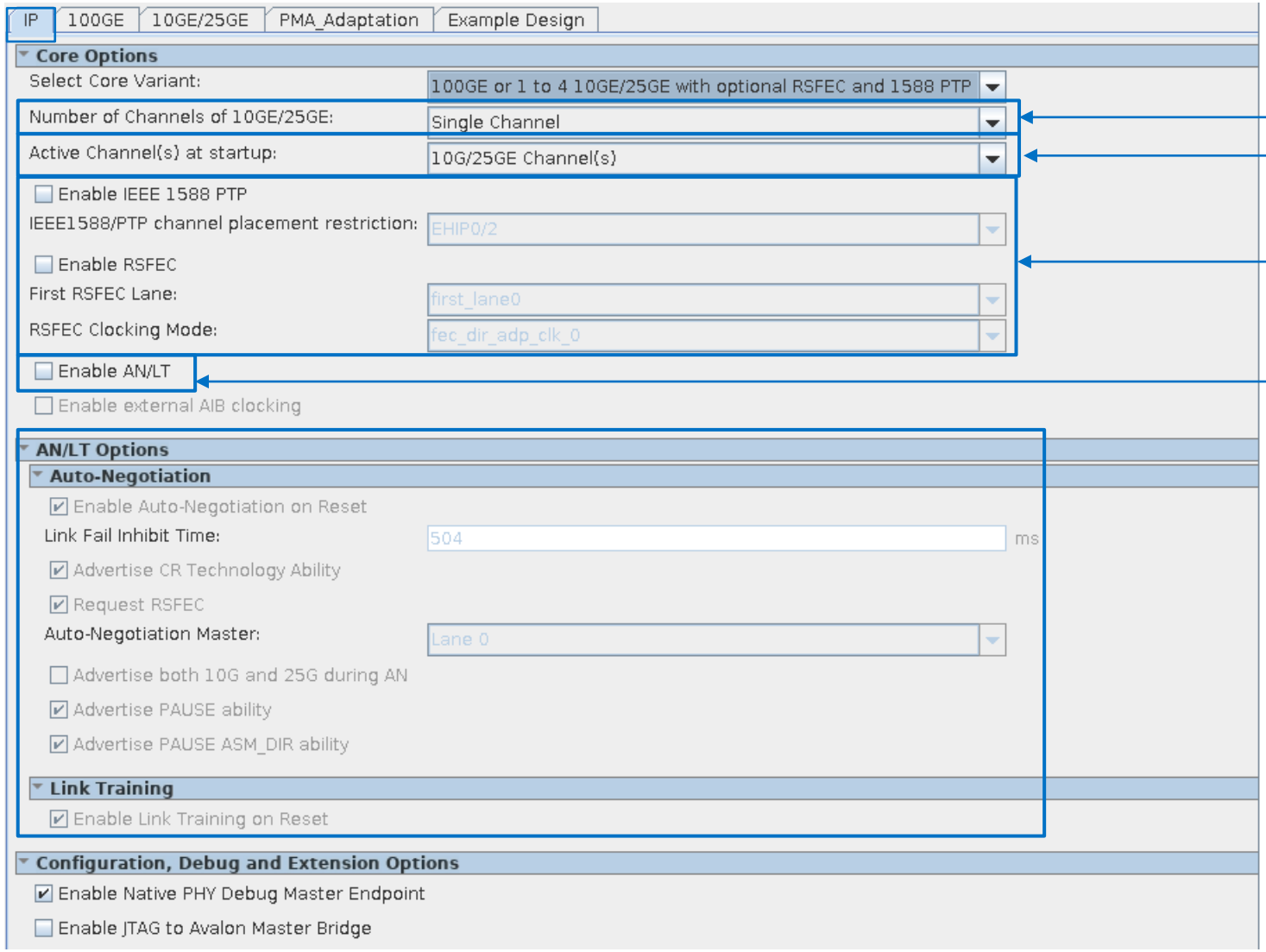


# Parameter Editor – IP Tab



# Parameter Editor – IP Tab (cont.)



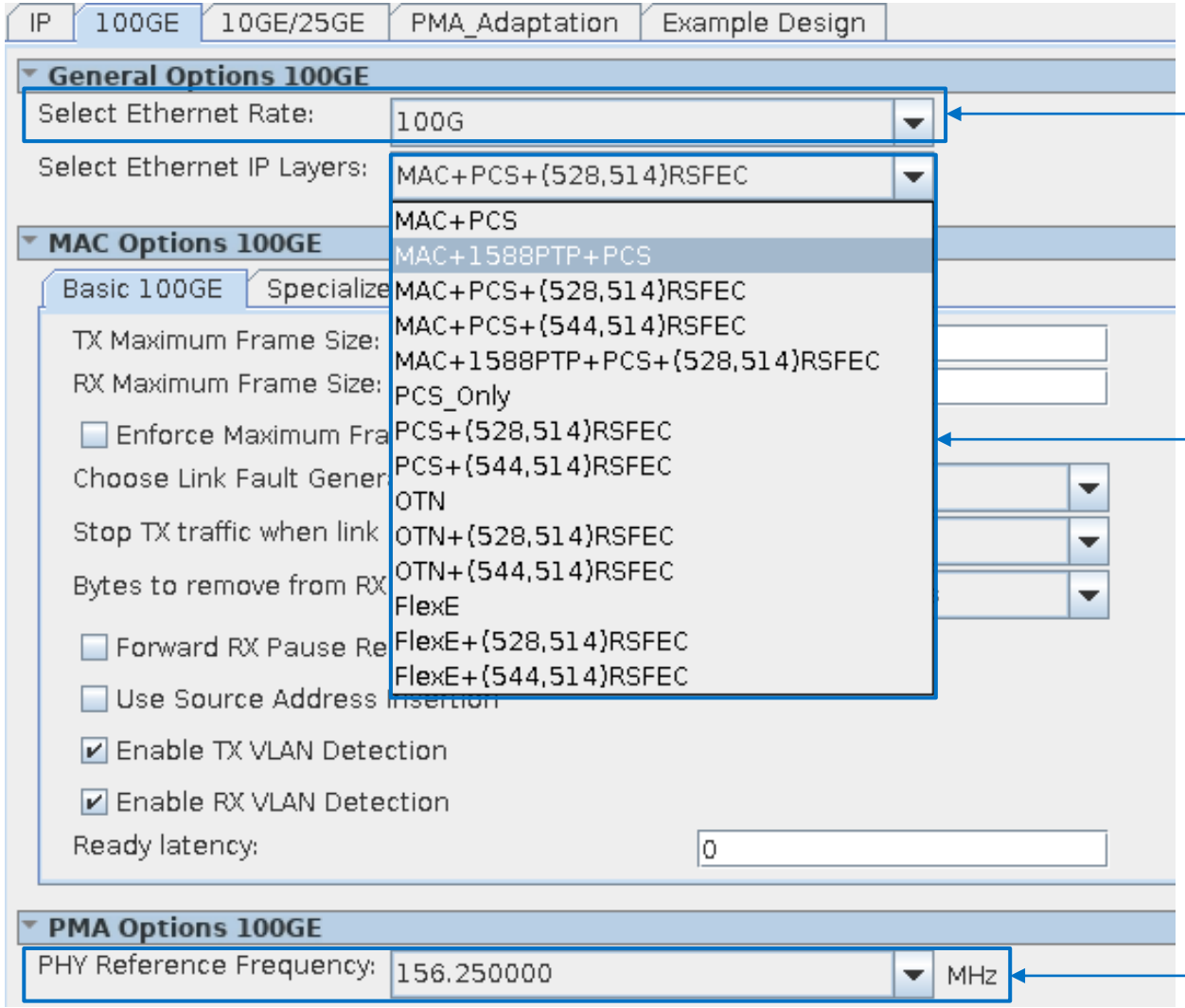

Choose # of 10GE/25GE channels

Choose Active channel at start up

Enables RS-FEC and PTP

Enables AN/LT

# Parameter Editor– 100GE Tab



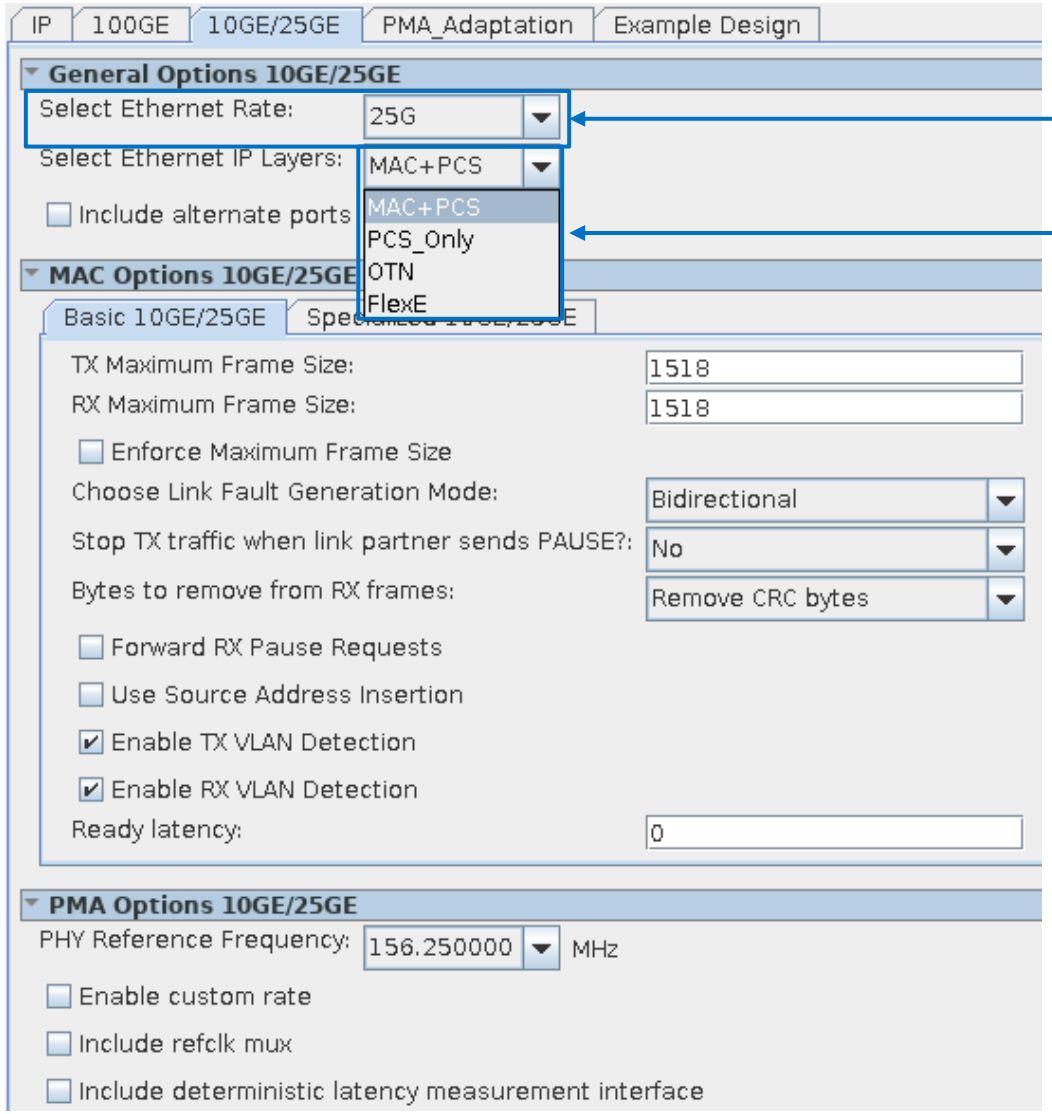

Ethernet rate fixed at 100G

Choose core variation and RS-FEC version

Select from list of PHY reference clock frequencies

** For the **100GE or 1 to 4 10GE/25GE with optional RSFEC and 1588 PTP variant**, requires setting the **Active Channel at Startup** option on the IP tab to **100GE Channel***

# Parameter Editor – 10GE/25GE Tab

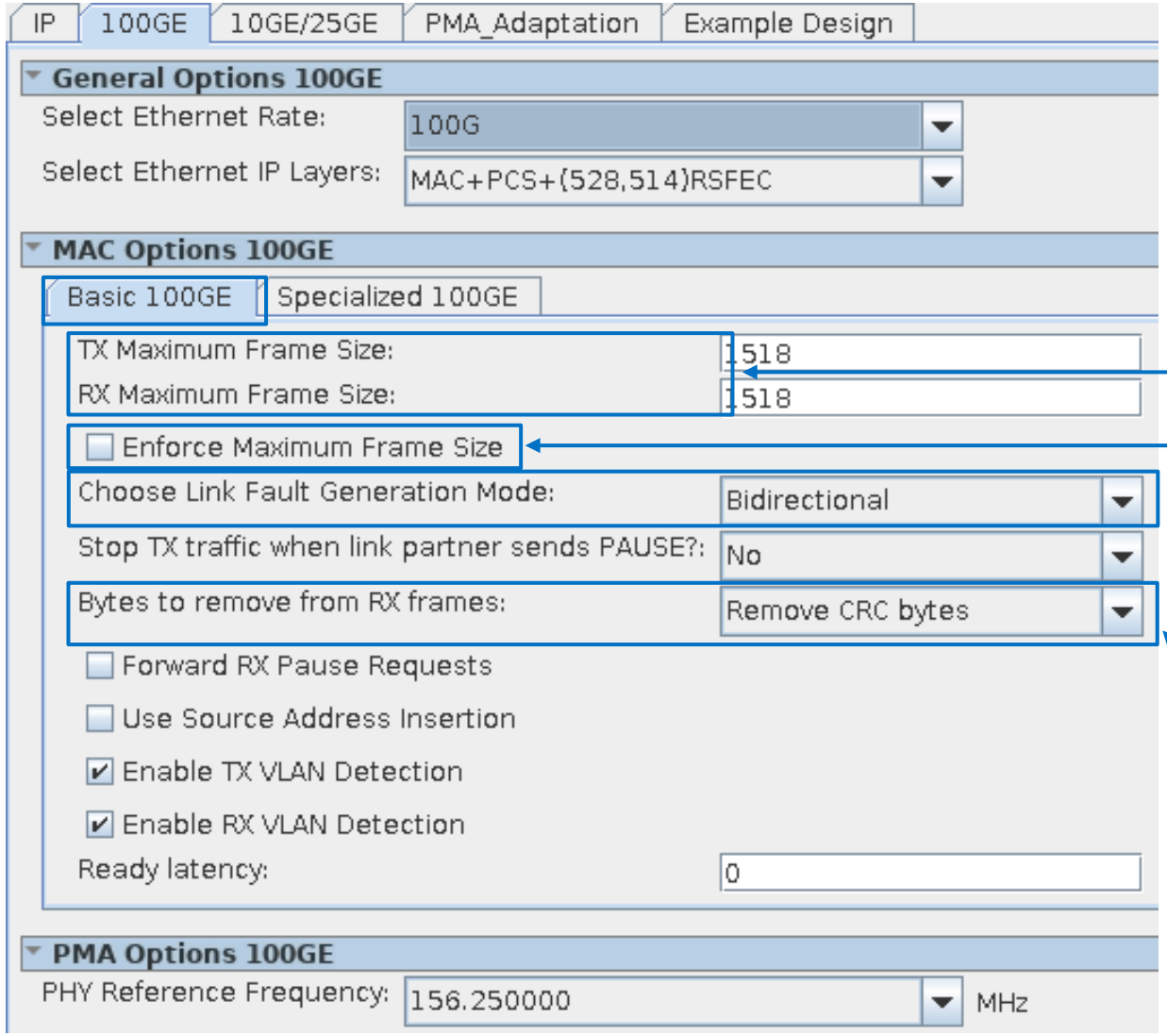



Select between 10G and 25G for Ethernet rate*

Choose core variation

** For the **100GE or 1 to 4 10GE/25GE with optional RSFEC and 1588 PTP variant**, requires setting the **Active Channel at Startup** option on the IP tab to **10GE/25GE Channel***

# Parameter Editor – Basic MAC Options



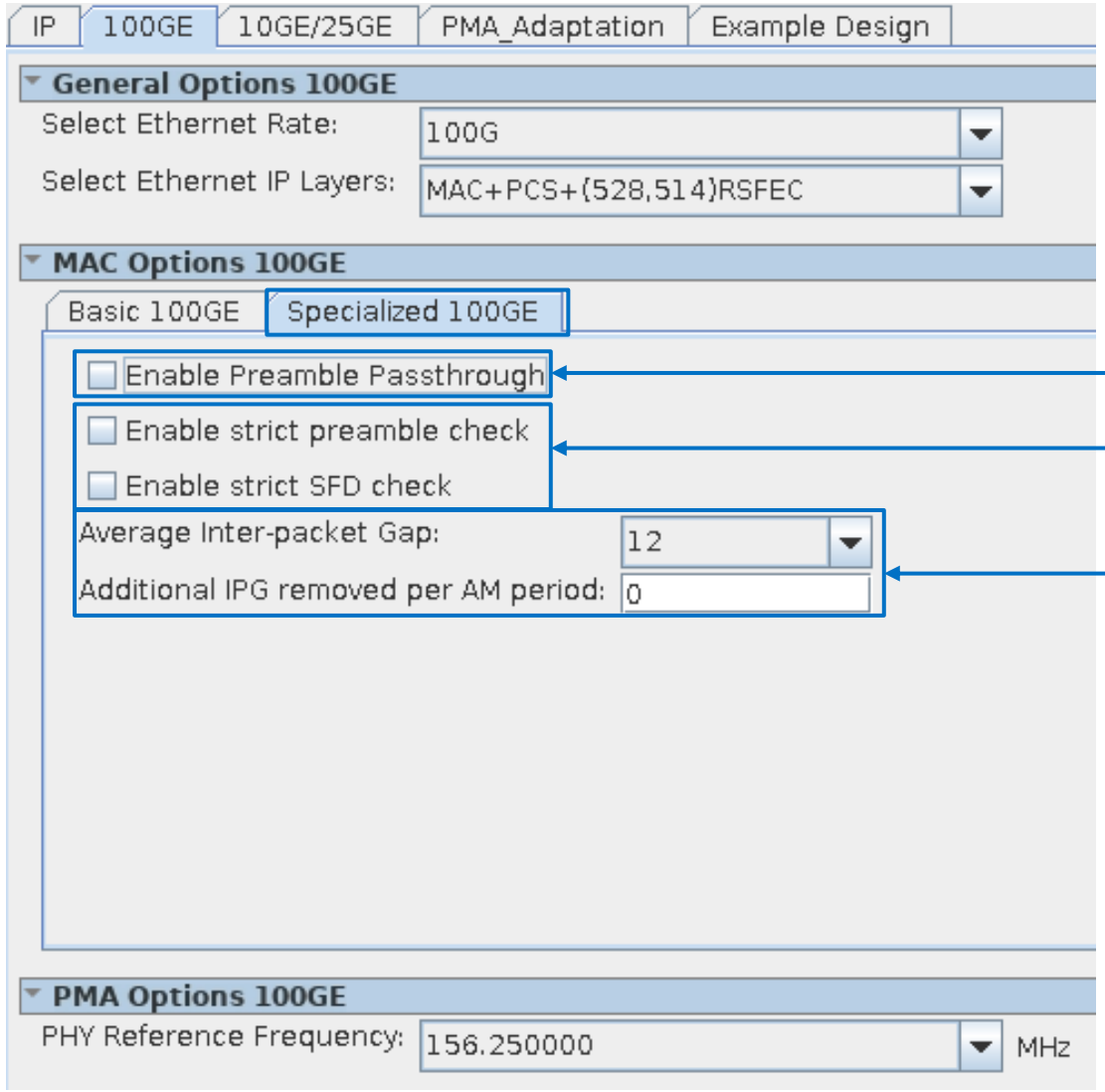

Choose the maximum frame size

Truncates packet to max RX frame size and increments oversized packets counter

If Unidirectional, in response to local fault, transmits remote fault ordered sets. No response to incoming remote fault ordered sets

Enables removal of CRC and CRC/PAD bytes form received frames before passing to RX MAC client

# Parameter Editor – Specialized MAC Options

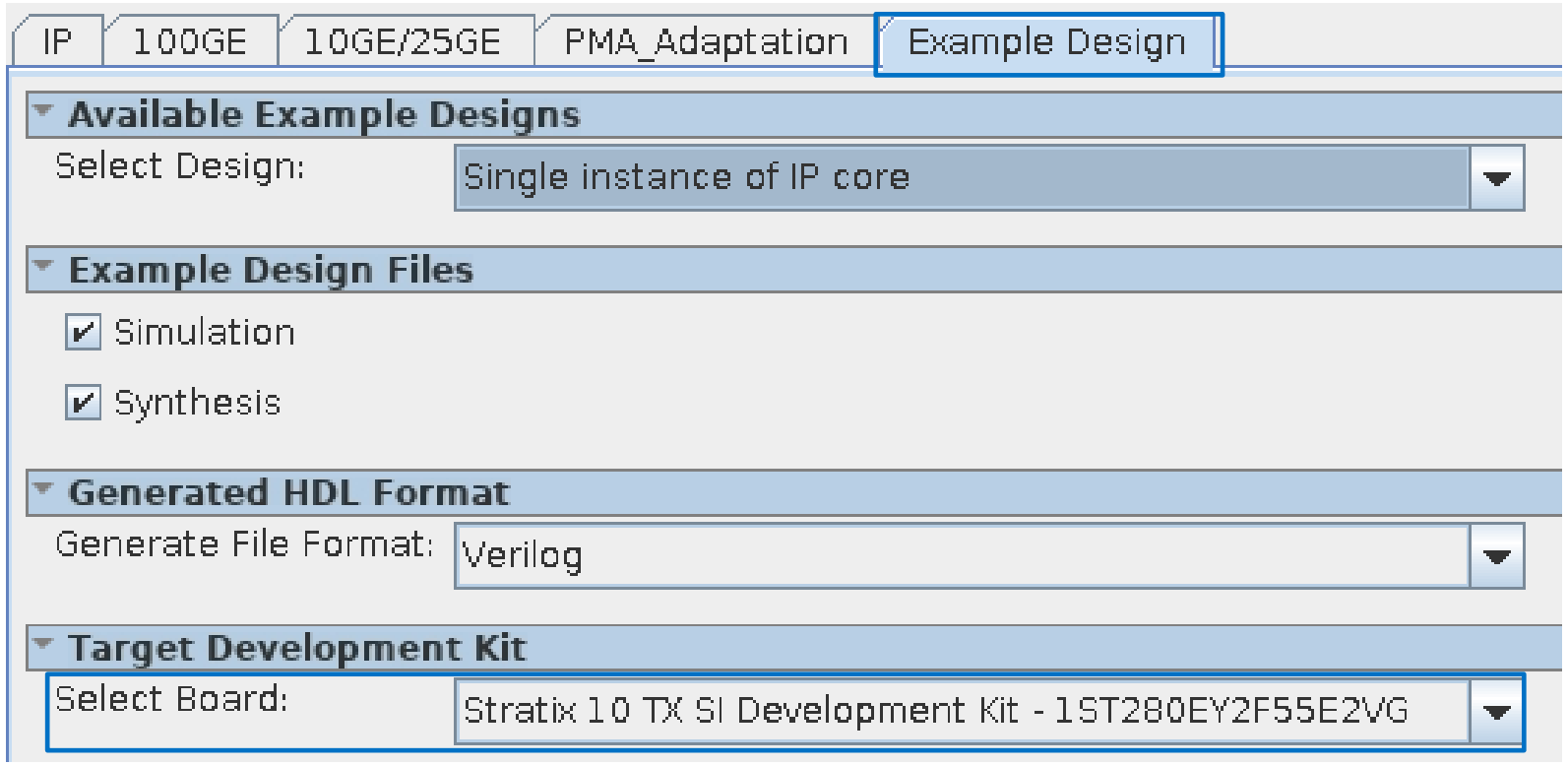



Preamble / start of frame delimiter sent to and received from core

Protection against spurious start frames

Interpacket gap control

# Parameter Editor – Example Design



# Configuring the Intel® FPGA E-Tile Hard IP for Ethernet

Summary

# Configuring the Intel® FPGA E-Tile Hard IP for Ethernet - Summary

- The E-Tile Hard IP for Ethernet Intel® FPGA IP Core enables the Intel FPGA E-tiles for 10, 25 or 100G Ethernet operation
- The E-tile Hard IP for Ethernet Intel FPGA IP Parameter Editor allows for easy selection of all configurable Ethernet MAC, PCS and PMA options

# Intel® Stratix® 10 FPGA E-Tile Hard IP for Ethernet Resources

- Documentation
  - E-Tile Transceiver PHY User Guide
    - https://www.intel.com/content/www/us/en/programmable/documentation/kqh1479167866037.html

# Debugging with the Ethernet Toolkit

# Debugging with the Ethernet Toolkit Objectives

Describe the features and functionality of the Ethernet Toolkit found in the Intel® Quartus® Prime Pro software

Set up and employ the Ethernet Toolkit to perform dynamic debugging and analysis on an Ethernet system

# Ethernet Toolkit

The Ethernet Toolkit is Intel® FPGA on-chip debugging tool for analyzing real-time status of Ethernet Intel FPGA IP

# Ethernet Toolkit

The Ethernet Toolkit is Intel® FPGA on-chip debugging tool for analyzing real-time status of Ethernet Intel FPGA IP

Runs on System Console platform

Interfaces with Ethernet IP through FPGA's JTAG connection

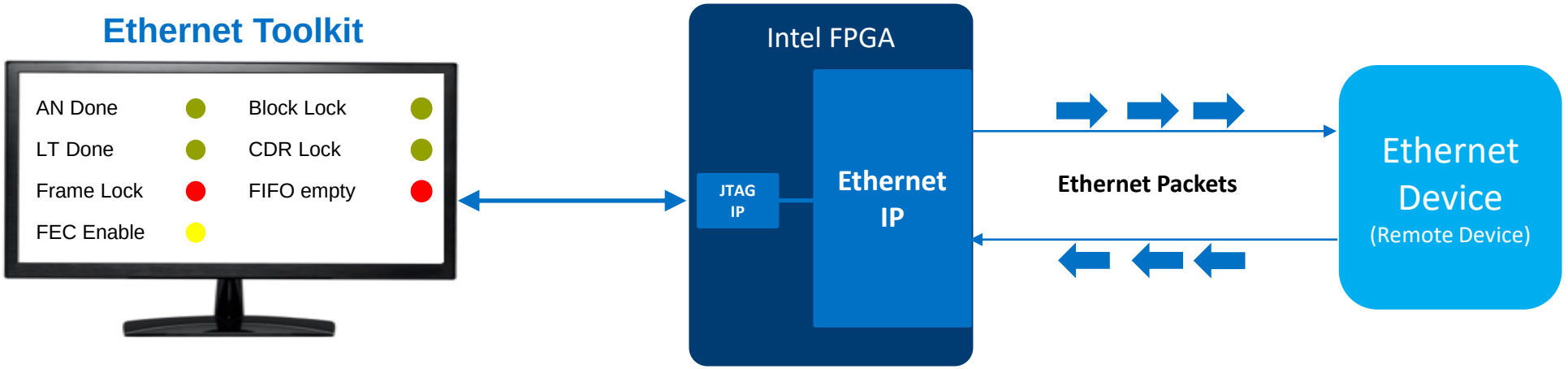
Continuously monitors IP functions through its registers

Provides graphical interface for accessing Ethernet IP and link information

** For more details on using the System Console, see the online training entitled System Console*

# Ethernet Toolkit Diagram

The Ethernet Toolkit is Intel® FPGA on-chip debugging tool for analyzing real-time status of Ethernet Intel FPGA IP



# Ethernet Toolkit Advantages

Real-time link updates

Register information decoded automatically

Lightweight

No need for additional equipment

Easy to use graphical interface

Free with Intel Quartus Prime Pro software

# Ethernet Toolkit User Functions

Verify link status

Assert MAC and channel resets

Read Ethernet IP status registers

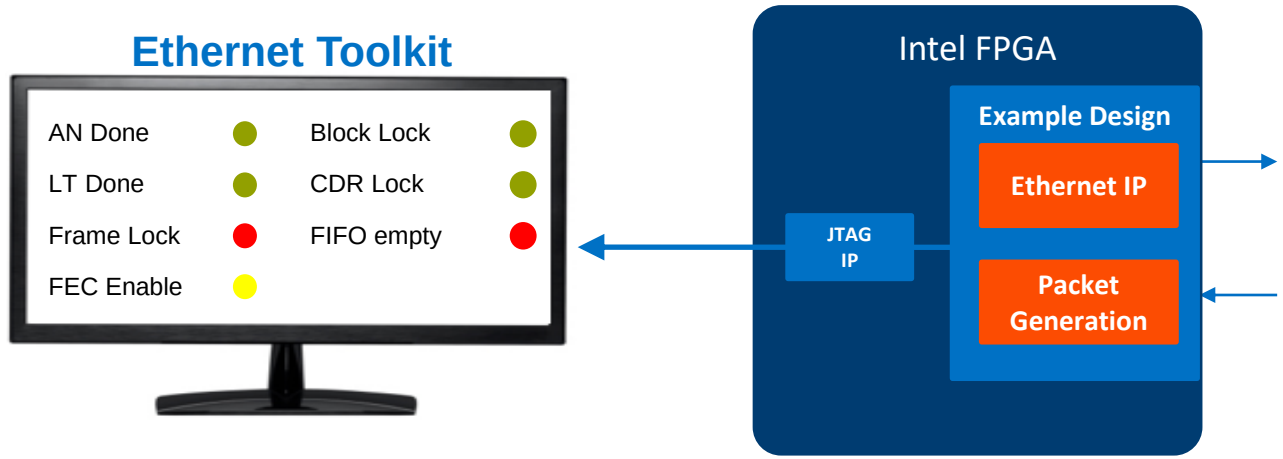
Read and Write Ethernet IP configuration registers

Read TX/RX channel statistics registers

# IP Example Design Ethernet Toolkit Support

## Additional Ethernet Toolkit functionality enabled when example designs used

- Control packet generator/checker
- Run predefined test procedures
- Enable/disable MAC loopback
- Set source/destination MAC addresses



# Ethernet Toolkit, Software and IP Support – Intel® Stratix® 10 FPGAs

| Supported Device Family | Transceiver Tile Type | IP Core Name | Data Rate(s) (Gbps) | Initial Software Version Support | Initial IP Version Support |
|---|---|---|---|---|---|
| Intel® Stratix® 10 | L-Tile | 10GBASE-KR PHY Intel® Stratix® 10 FPGA IP | 10 | 20.1 | 19.1.0 |
| | | Low Latency 40G Ethernet Intel FPGA IP | 40 | 20.1 | 19.1.0 |
| | | Low Latency 100G Ethernet Intel FPGA IP | 100 | 20.1 | 19.1.1 |
| | H-Tile | 10GBASE-KR PHY Intel® Stratix® 10 FPGA IP | 10 | 20.1 | 19.1.0 |
| | | Low Latency 40G Ethernet Intel FPGA IP | 40 | 20.1 | 19.1.0 |
| | | Low Latency 100G Ethernet Intel FPGA IP | 100 | 20.1 | 19.1.1 |
| | | H-Tile Hard IP for Ethernet Intel FPGA IP | 100 | 20.1 | 19.2.0 |
| | E-Tile | Low Latency E-Tile 40G Ethernet Intel FPGA IP | 40 | 20.1 | 19.1.1 |
| | | E-Tile Hard IP for Ethernet Intel FPGA IP | 10/25/100 | 20.1 | 19.3.0 |
| Intel Stratix 10 GX 10M | H-Tile | Low Latency 40G for ASIC Proto Ethernet Intel FPGA IP | 40 | 20.1 | 19.1.0 |

# Ethernet Toolkit, Software and IP Support – Intel® Agilex™ FPGAs

| Supported Device Family | Transceiver Tile Type | IP Core Name | Data Rate(s) (Gbps) | Initial Software Version Support | Initial IP Version Support |
|---|---|---|---|---|---|
| Intel® Agilex™ | H-Tile | Low Latency 100G Ethernet Intel FPGA IP | 100 | 20.1 | 19.1.1 |
| | | H-Tile Hard IP for Ethernet Intel FPGA IP | 100 | 20.1 | 19.2.0 |
| | E-Tile | Low Latency E-Tile 40G Ethernet Intel FPGA IP | 40 | 20.1 | 19.1.1 |
| | | E-Tile Hard IP for Ethernet Intel FPGA IP | 10/25/100 | 20.1 | 19.3.0 |

** Always check the latest Ethernet Toolkit documentation for current or additional IP and tile support.*

# Debugging with the Ethernet Toolkit

## Ethernet Toolkit Flow

# Ethernet Toolkit Flow

Set up the Ethernet Toolkit

Launch the Ethernet Toolkit

# Ethernet Toolkit Flow

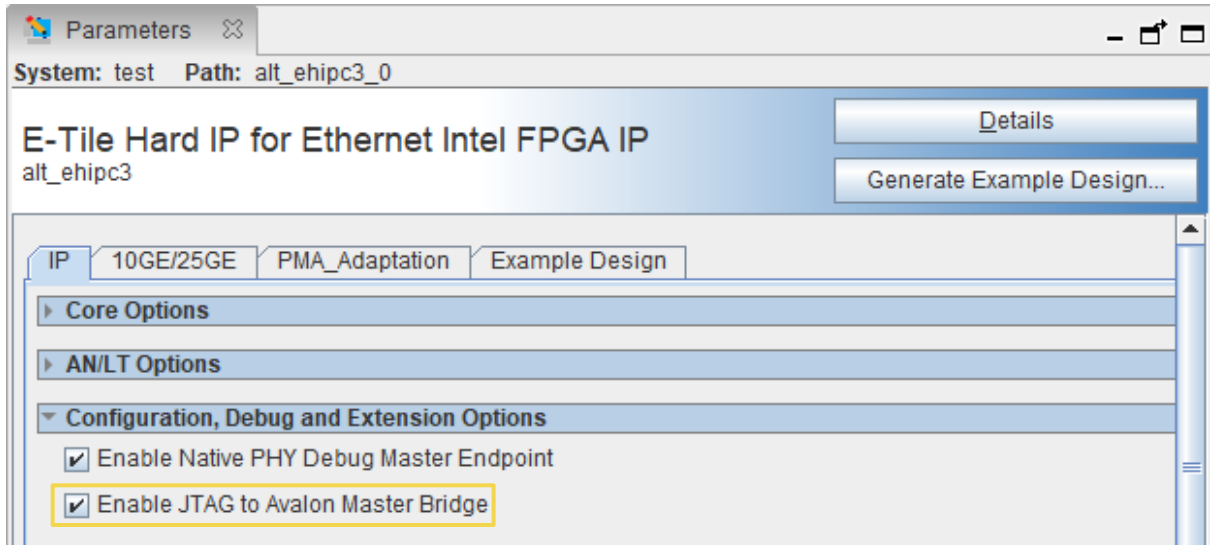
## Set up the Ethernet Toolkit

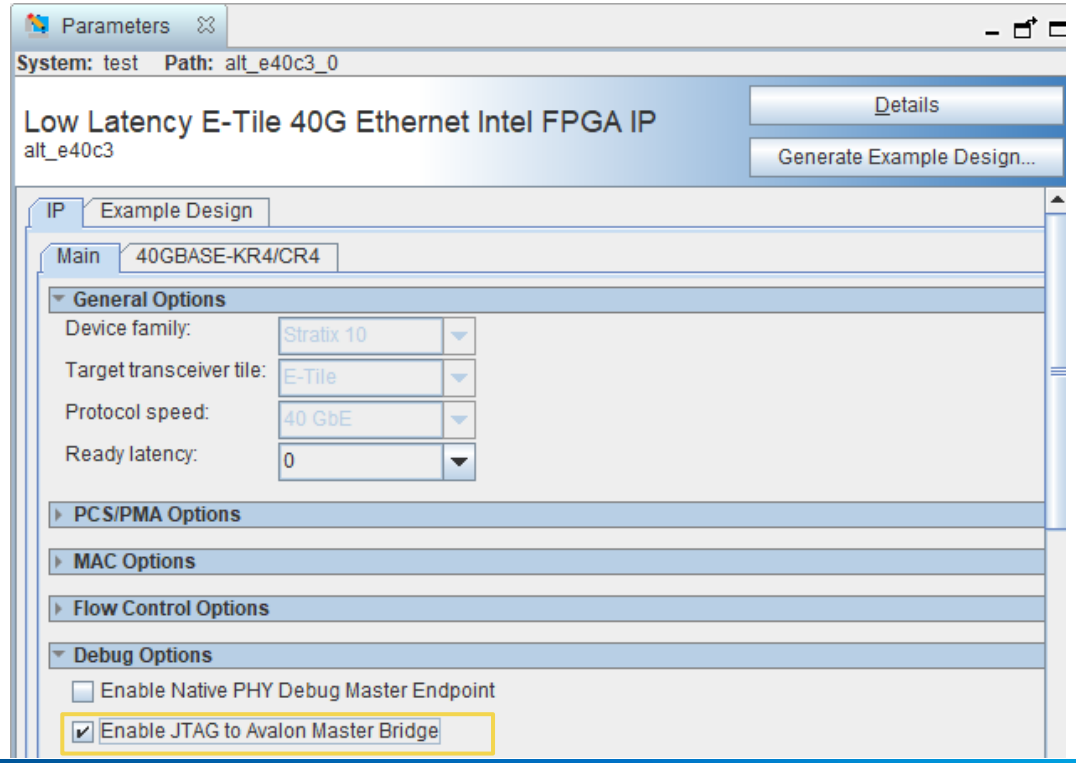
- Enable JTAG to Avalon Bridge
- Generate Ethernet IP example design (optional)
- Compile design and configure FPGA

## **Launch** the Ethernet Toolkit

# Enable JTAG to Avalon Bridge

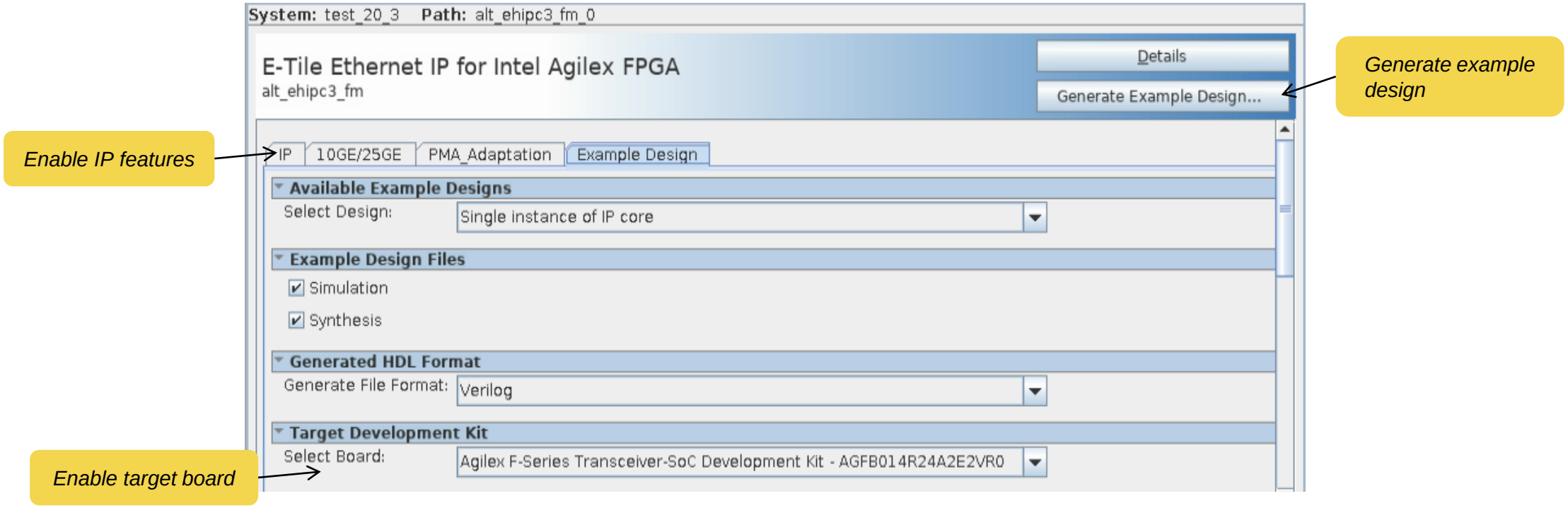
Creates the logic necessary for the Ethernet Toolkit to perform memory accesses into the IP register space over JTAG



# Generate Ethernet IP Example Design (Optional)

## Each Ethernet IP generates hardware ready example designs



# Ethernet Toolkit Flow

Set up the Ethernet Toolkit

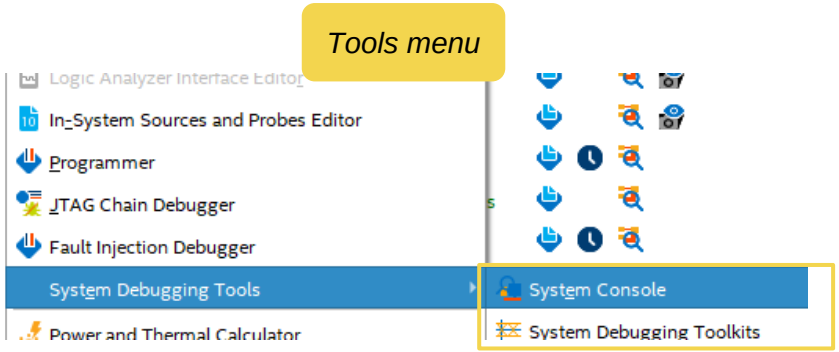
## Launch the Ethernet Toolkit

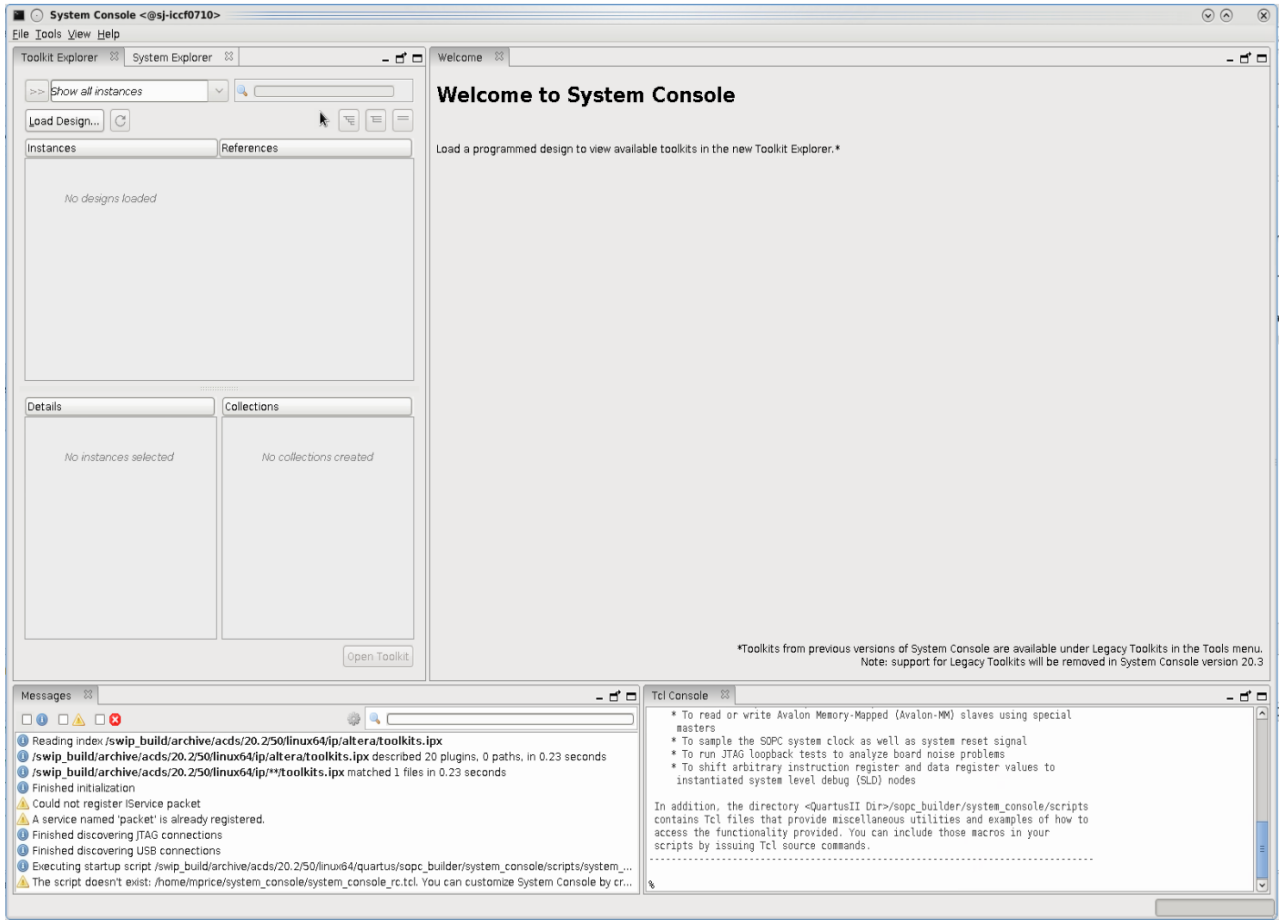
1. Launch System Console
2. Load Design
3. Select Ethernet IP instance for control and open Ethernet Toolkit
4. Run checks and tests

# 1. Launch System Console

## Open the System Console or System Debugging Toolkits

- Intel® Quartus® Prime Pro software Tools menu → System Debugging Tools submenu

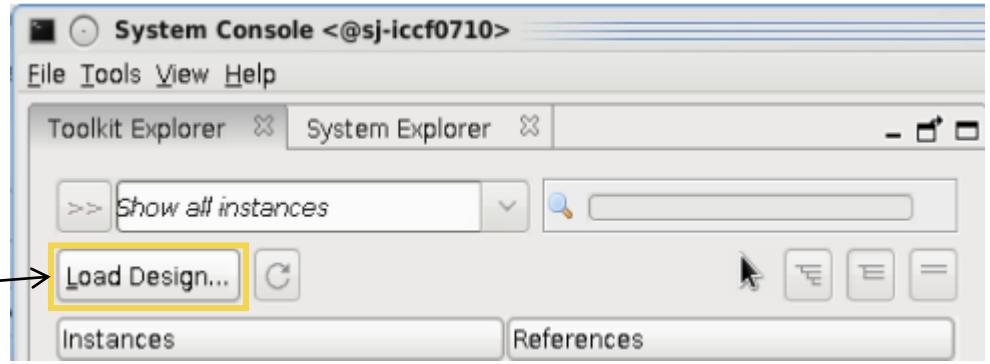


# 2. Load Design

## Load your Ethernet IP design project(s) into System Console

- Click Load Design button
- Project will auto-load if Ethernet Toolkit is launched from Intel® Quartus® Prime Pro software with project open
- Load multiple projects if testing multiple interfaces/devices/boards

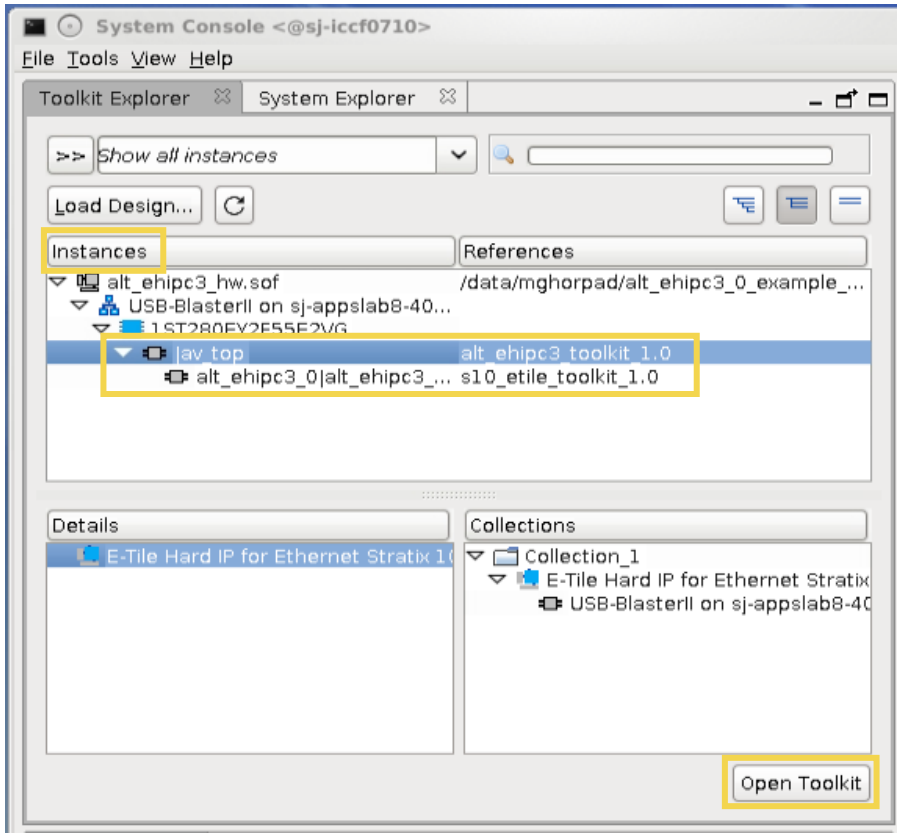


# 3. Select Ethernet IP instance for control and Open Toolkit

Supported Ethernet IP instances in design automatically recognized by System Console and listed in the Instances section

Select target Ethernet IP from list of IP instances

Click Open Toolkit



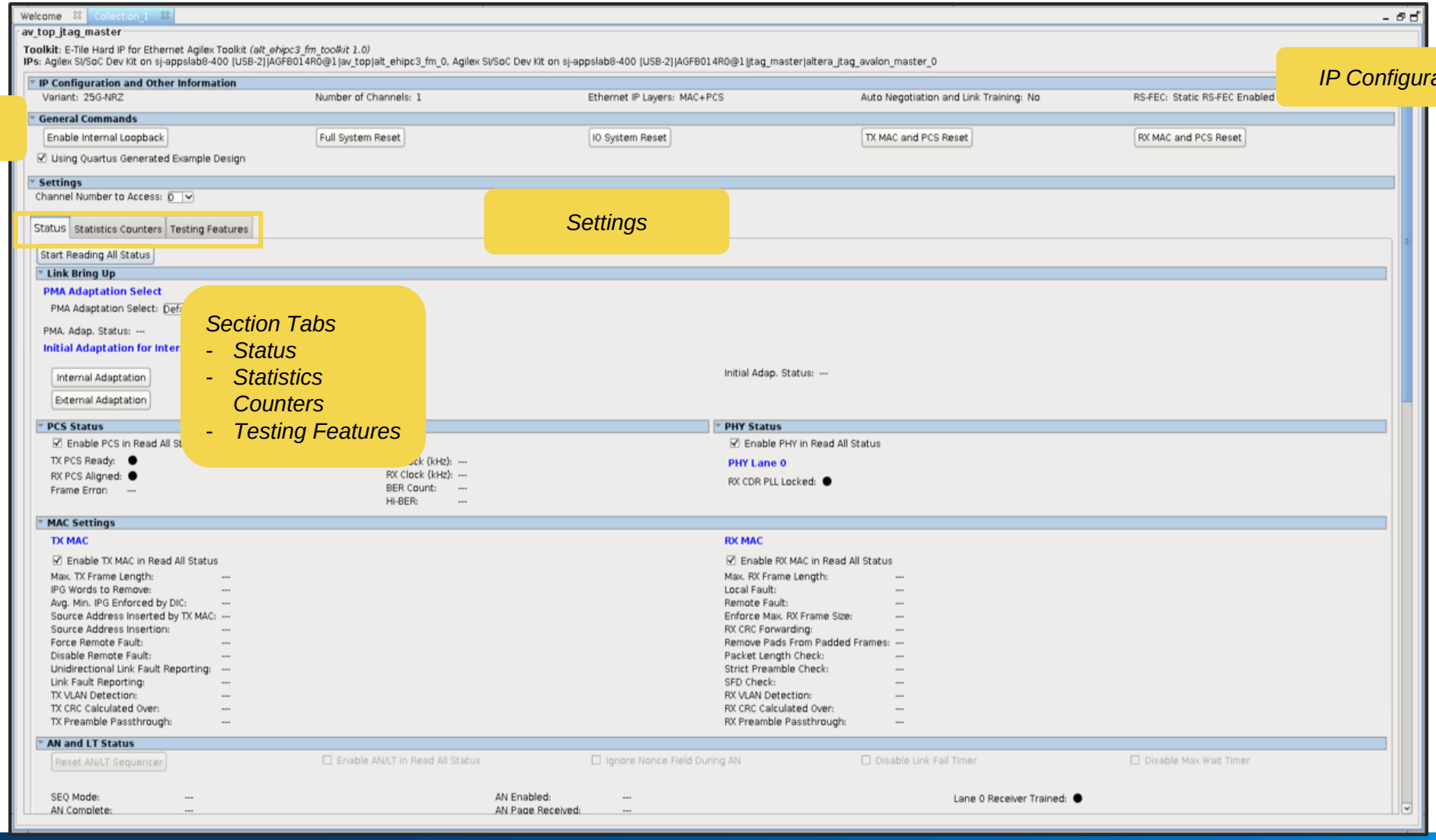
# 4. Run Checks and Tests

## Use IP registers to interact with Ethernet IP components

- Resets
- MAC
- PCS/PMA
- RS-FEC
- Auto Negotiation (AN) /Link Training (LT) logic

** Available information changes based on IP core variation and IP options enabled.*

# Ethernet Toolkit User Interface




*General Commands*

*IP Configuration*

*Settings*

*Section Tabs*
- *Status*
- *Statistics Counters*
- *Testing Features*

# IP Configuration


## Verify IP settings

- IP core variant
- IP Ethernet components and features enabled

# General Commands

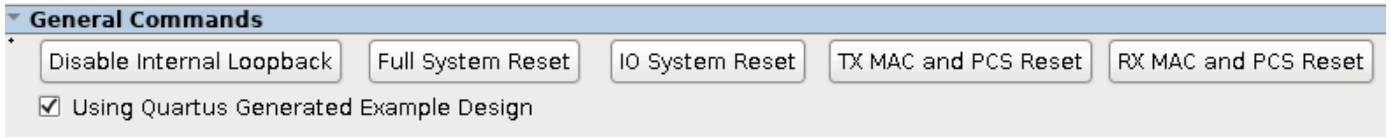
Enable/disable loopback

System reset

Reset

- PMA
- TX MAC and PCS
- RX MAC and PCS

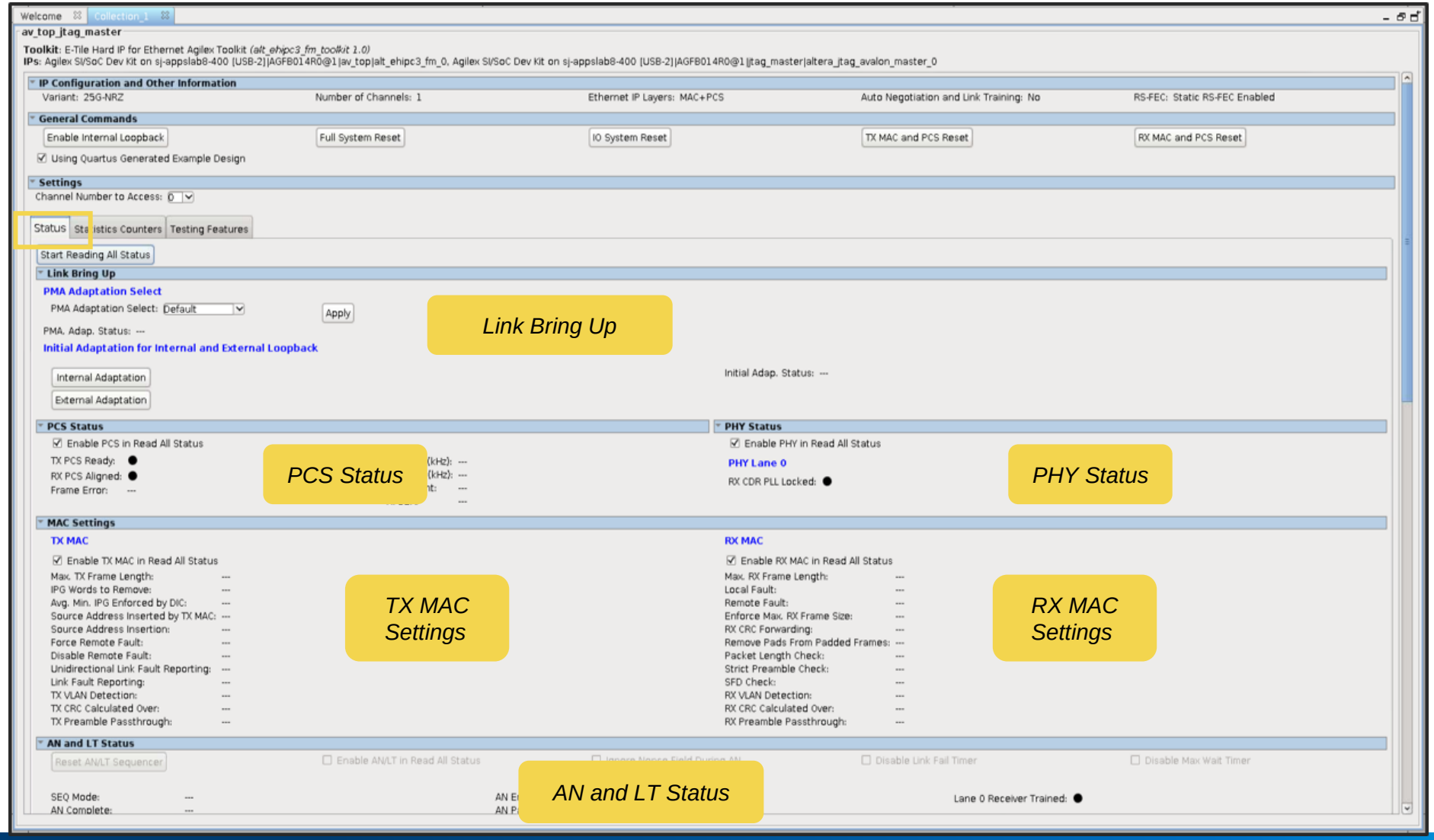
Enable example design control



# Settings


Select the channel number within Ethernet IP for register access

# Status Tab

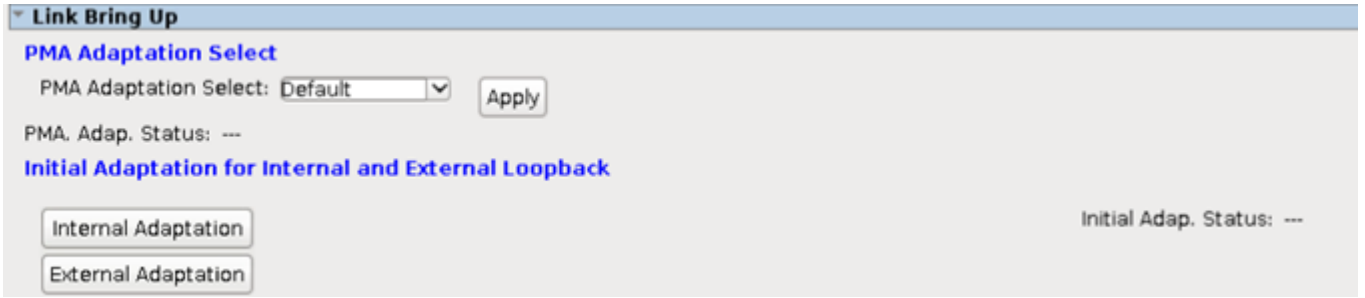

Welcome
Collection_1
av_top_jtag_master
Toolkit: E-Tile Hard IP for Ethernet Agilex Toolkit (alt_ehipc3_fm_toolkit 1.0)
IPs: Agilex SiSoC Dev Kit on sj-appslab8-400 [USB-2]|AGFB014R0@1|av_top|alt_ehipc3_fm_0, Agilex SiSoC Dev Kit on sj-appslab8-400 [USB-2]|AGFB014R0@1|jtag_master|altera_jtag_avalon_master_0
IP Configuration and Other Information
Variant: 25G-NRZ
Number of Channels: 1
Ethernet IP Layers: MAC+PCS
Auto Negotiation and Link Training: No
RS-FEC: Static RS-FEC Enabled
General Commands
Enable Internal Loopback
Full System Reset
IO System Reset
TX MAC and PCS Reset
RX MAC and PCS Reset
Using Quartus Generated Example Design
Settings
Channel Number to Access:
Status
Statistics Counters
Testing Features
Start Reading All Status
Link Bring Up
PMA Adaptation Select
PMA Adaptation Select: Default
Apply
PMA. Adap. Status: ---
Initial Adaptation for Internal and External Loopback
Internal Adaptation
External Adaptation
Initial Adap. Status: ---
Link Bring Up
PCS Status
Enable PCS in Read All Status
TX PCS Ready:
RX PCS Aligned:
Frame Error: ---
PCS Status
PHY Status
Enable PHY in Read All Status
PHY Lane 0
RX CDR PLL Locked:
PHY Status
MAC Settings
TX MAC
Enable TX MAC in Read All Status
Max. TX Frame Length: ---
IPG Words to Remove: ---
Avg. Min. IPG Enforced by DIC: ---
Source Address Inserted by TX MAC: ---
Source Address Insertion: ---
Force Remote Fault: ---
Disable Remote Fault: ---
Unidirectional Link Fault Reporting: ---
Link Fault Reporting: ---
TX VLAN Detection: ---
TX CRC Calculated Over: ---
TX Preamble Passthrough: ---
TX MAC Settings
RX MAC
Enable RX MAC in Read All Status
Max. RX Frame Length: ---
Local Fault: ---
Remote Fault: ---
Enforce Max. RX Frame Size: ---
RX CRC Forwarding: ---
Remove Pads From Padded Frames: ---
Packet Length Check: ---
Strict Preamble Check: ---
SFD Check: ---
RX VLAN Detection: ---
RX CRC Calculated Over: ---
RX Preamble Passthrough: ---
RX MAC Settings
AN and LT Status
Reset AN/LT Sequencer
Enable AN/LT in Read All Status
Disable Link Fail Timer
Disable Max Wait Timer
SEQ Mode: ---
AN Complete: ---
Lane 0 Receiver Trained:
AN and LT Status

# Link Bring Up

Select adaptation mode

View adaptation status

Select internal or external adaptation



# PCS/PHY Status

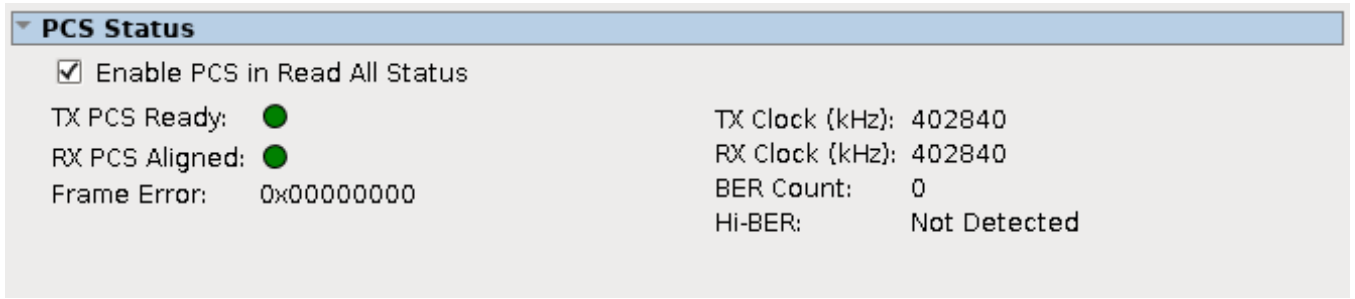
## Read current values of PHY and PCS registers

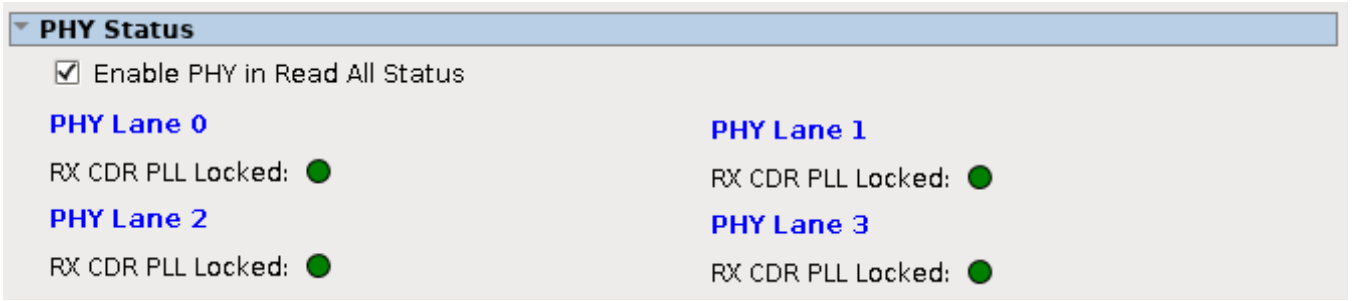
## Enable/disable RX/TX Read All Status

- Reads IP registers at regular interval

## Status indicators

- Locked PLLs
- RX word alignment
- TX/RX clock frequencies
- RX frame error count
- RX Bit error rate (BER) count



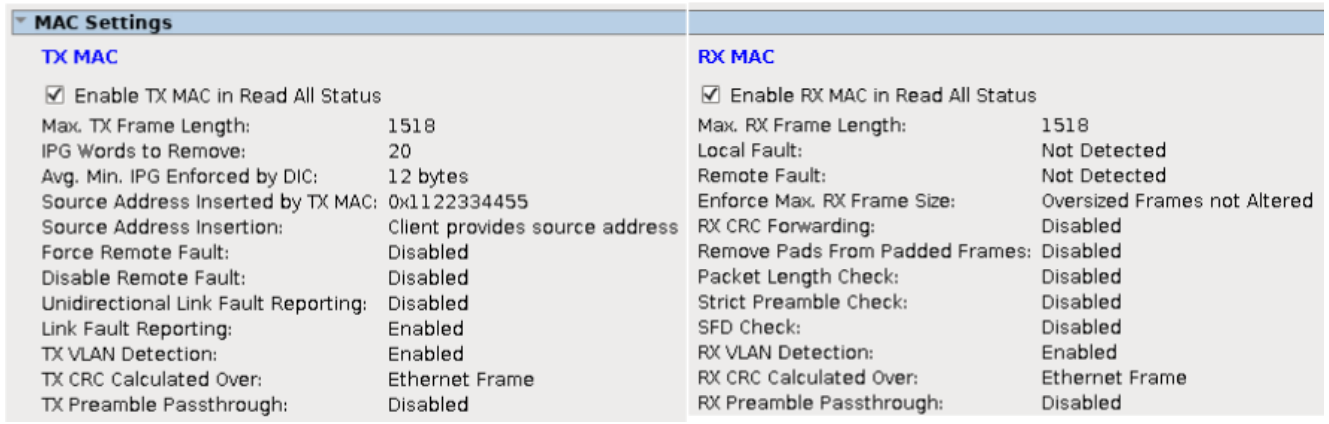
# MAC Settings

Read current values of MAC registers

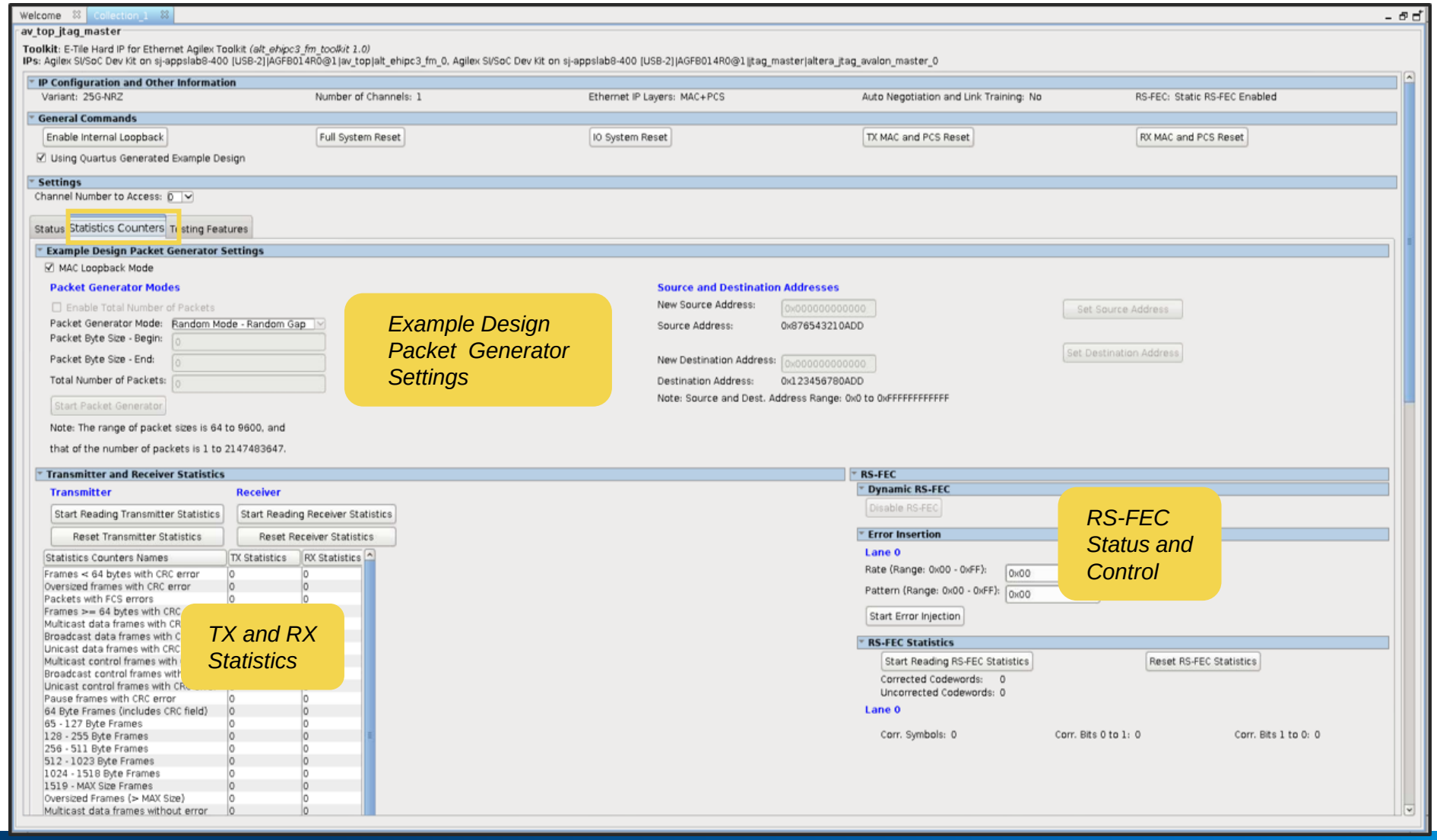
Enable/disable RX/TX Read All Status

View current MAC settings

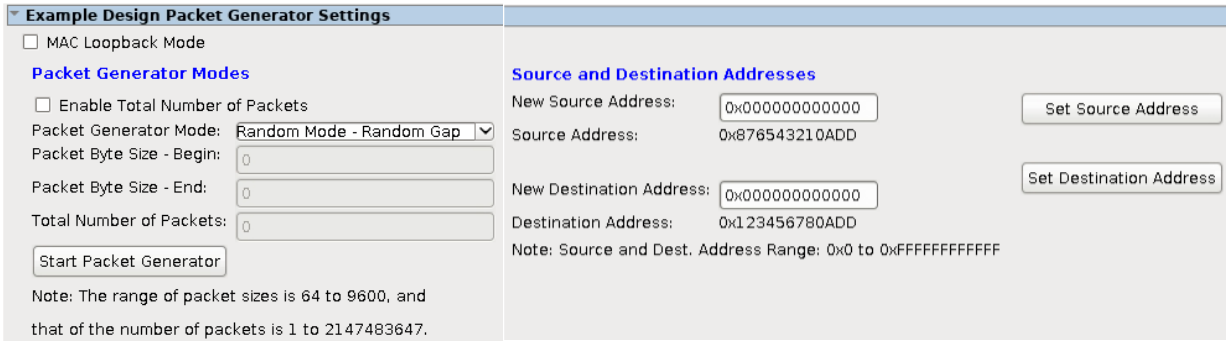
- Maximum frame length
- Fault detection and reporting
- CRC calculation
- Packet length checking



# Statistics Counters Tab

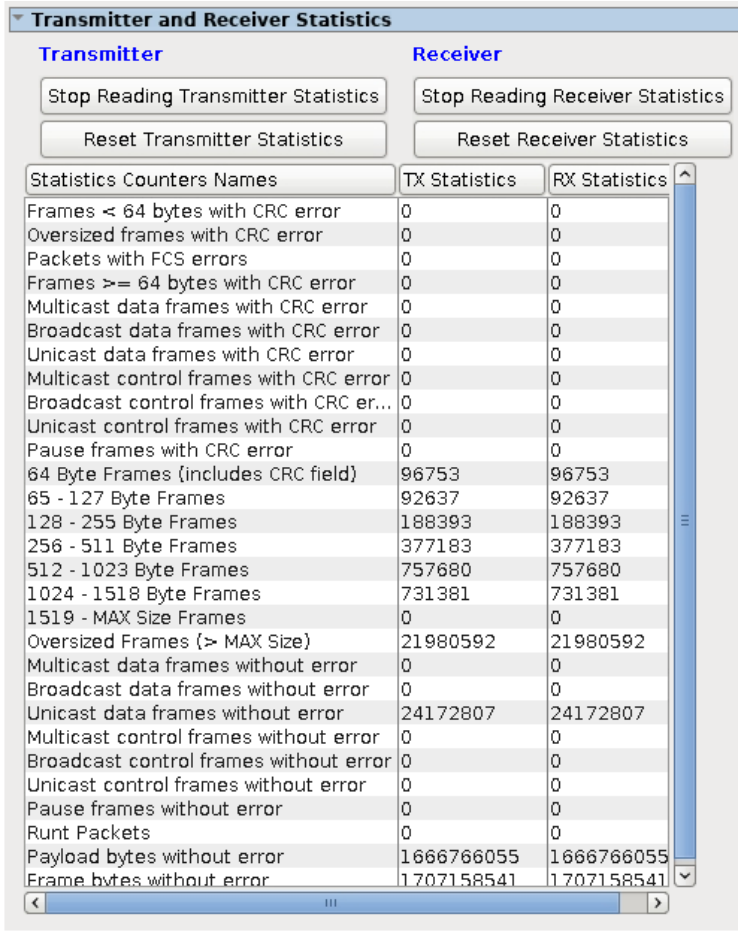


# Example Design Packet Generator Settings (Statistics Counters Tab)




- Available when using design example generated by Ethernet IP core
- Enable/disable MAC loopback
- Start/stop packet generation
- Choose pattern (random, fixed size and incremental)
- Set source and destination MAC addresses

# TX and RX Statistics




| Statistics Counters Names | TX Statistics | RX Statistics |
|---|---|---|
| Frames < 64 bytes with CRC error | 0 | 0 |
| Oversized frames with CRC error | 0 | 0 |
| Packets with FCS errors | 0 | 0 |
| Frames >= 64 bytes with CRC error | 0 | 0 |
| Multicast data frames with CRC error | 0 | 0 |
| Broadcast data frames with CRC error | 0 | 0 |
| Unicast data frames with CRC error | 0 | 0 |
| Multicast control frames with CRC error | 0 | 0 |
| Broadcast control frames with CRC er... | 0 | 0 |
| Unicast control frames with CRC error | 0 | 0 |
| Pause frames with CRC error | 0 | 0 |
| 64 Byte Frames (includes CRC field) | 96753 | 96753 |
| 65 - 127 Byte Frames | 92637 | 92637 |
| 128 - 255 Byte Frames | 188393 | 188393 |
| 256 - 511 Byte Frames | 377183 | 377183 |
| 512 - 1023 Byte Frames | 757680 | 757680 |
| 1024 - 1518 Byte Frames | 731381 | 731381 |
| 1519 - MAX Size Frames | 0 | 0 |
| Oversized Frames (> MAX Size) | 21980592 | 21980592 |
| Multicast data frames without error | 0 | 0 |
| Broadcast data frames without error | 0 | 0 |
| Unicast data frames without error | 24172807 | 24172807 |
| Multicast control frames without error | 0 | 0 |
| Broadcast control frames without error | 0 | 0 |
| Unicast control frames without error | 0 | 0 |
| Pause frames without error | 0 | 0 |
| Runt Packets | 0 | 0 |
| Payload bytes without error | 1666766055 | 1666766055 |
| Frame bytes without error | 1707158541 | 1707158541 |

View current value of statistical counter registers

Enable/disable reading RX/TX statistical registers

- Reads IP registers at regular interval

Reset the counter values

# RS-FEC

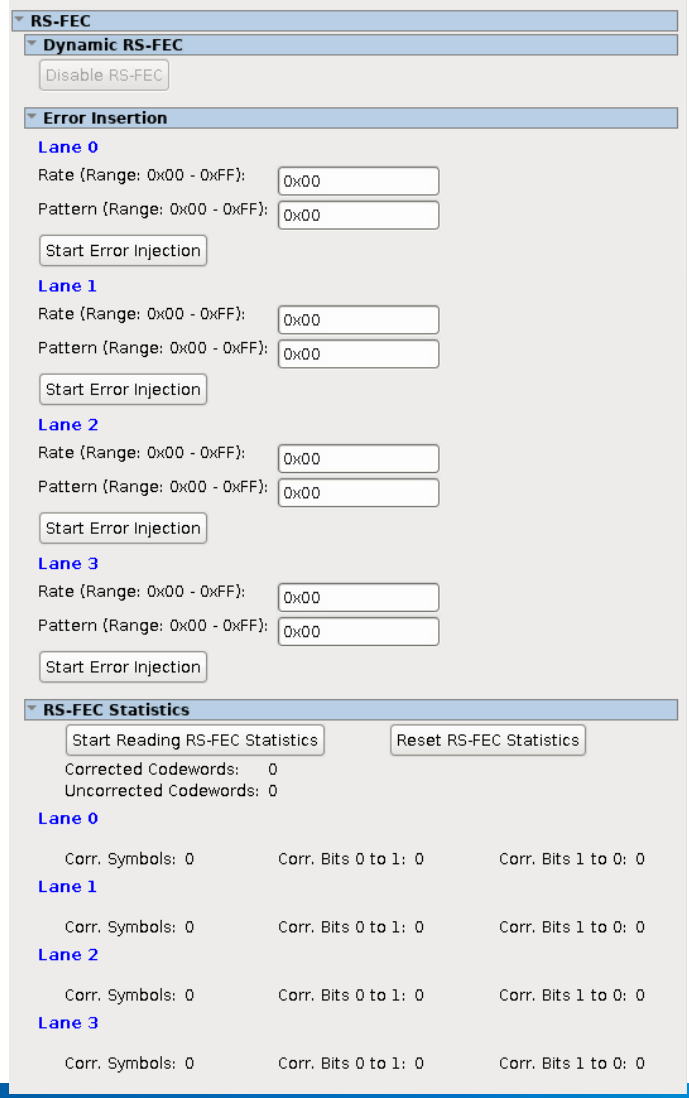
View and write RS-FEC register values

Enable/disable RS-FEC

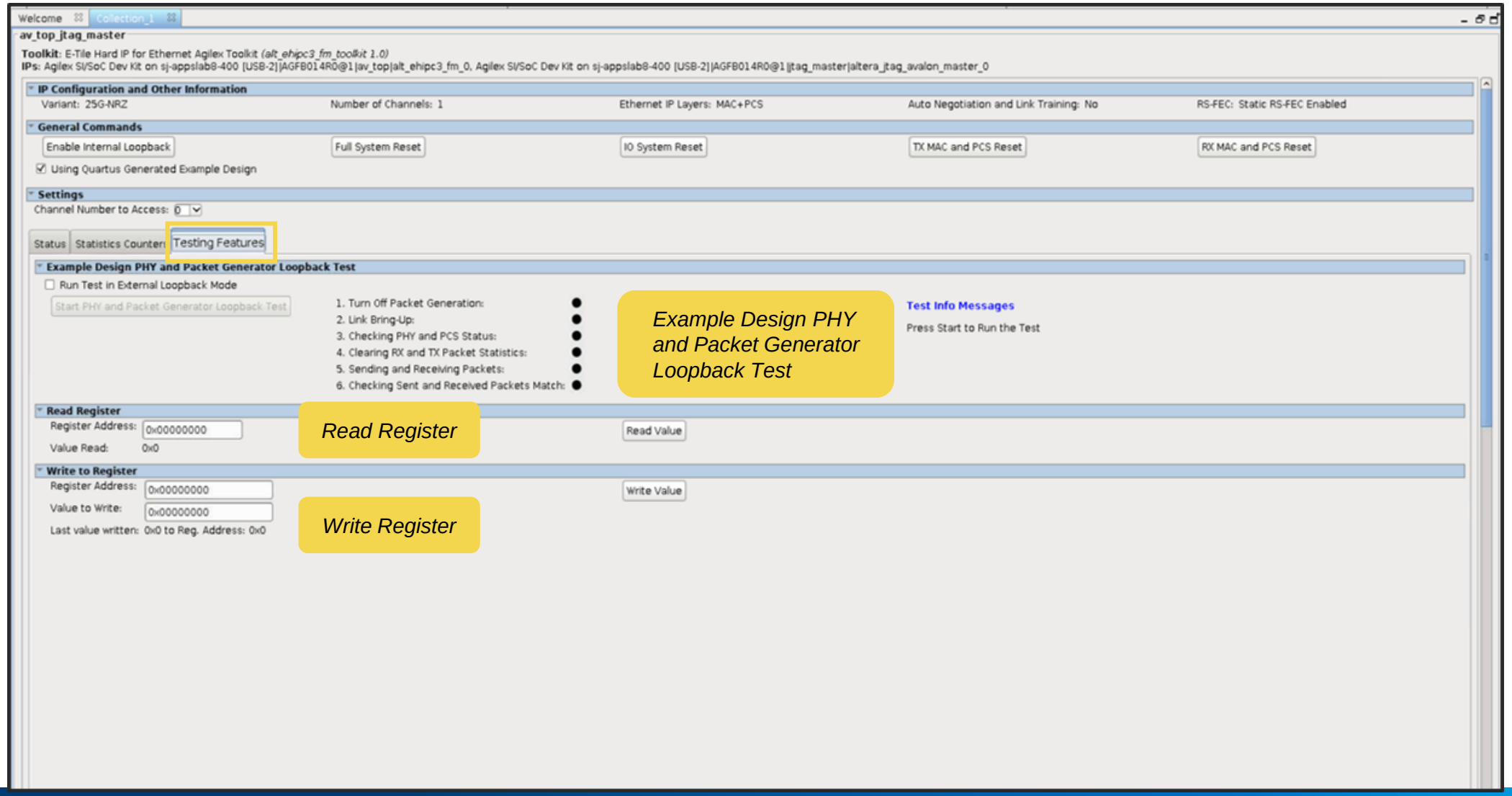
Perform error injection

Enable/disable reading RS-FEC statistical registers

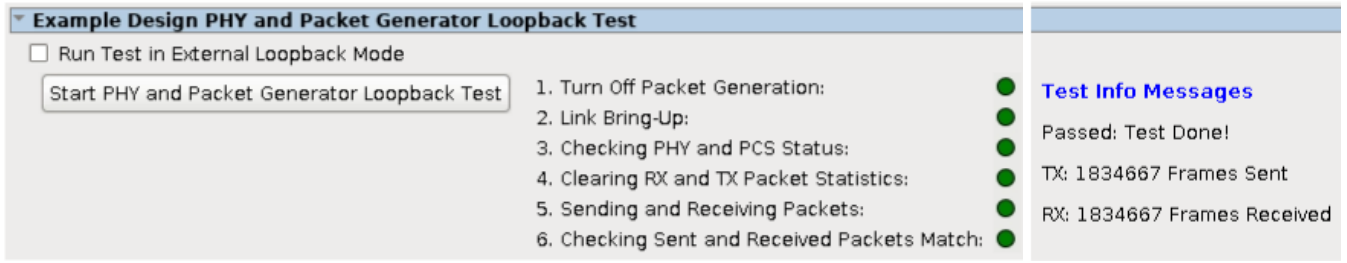
Reset RS-FEC statistical registers



# Testing Features Tab



# Example Design PHY and Packet Generator Loopback Test




Available when using design example generated by Ethernet IP core

Perform sanity check on link

Run loopback test using internal or external loopback

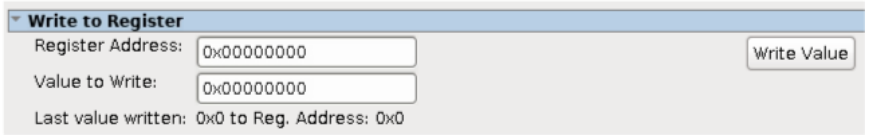
Must disable MAC loopback

# Write to/Read Register

## Directly access registers not visible in Ethernet Toolkit UI

## Enter exact register full 32-bit address

- User must manually calculate address when given base address plus register offset
- Designer must be aware of register availability and content
- Avoid reading or writing to undefined registers




# Debugging with the Ethernet Toolkit

## Summary

# Debugging with the Ethernet Toolkit – Summary

Ethernet Toolkit is available in the Intel® Quartus® Prime Pro software and is easily enabled in your designs using Ethernet Intel FPGA IP cores

Ethernet Toolkit provides the critical visibility and control you need when analyzing and debugging designs using Ethernet Intel FPGA IP

# Resources

## Ethernet IP – Support Center

- https://www.intel.com/content/www/us/en/programmable/support/support-resources/support-centers/ethernet-support.html

## Ethernet Toolkit User Guide

- https://www.intel.com/content/www/us/en/programmable/documentation/nrb1596652301528.html

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