

Signal Chain Integrity

Optimizing the Performance of the RF Signal Chain

Central Apps Webinar Series

Larry Prestia

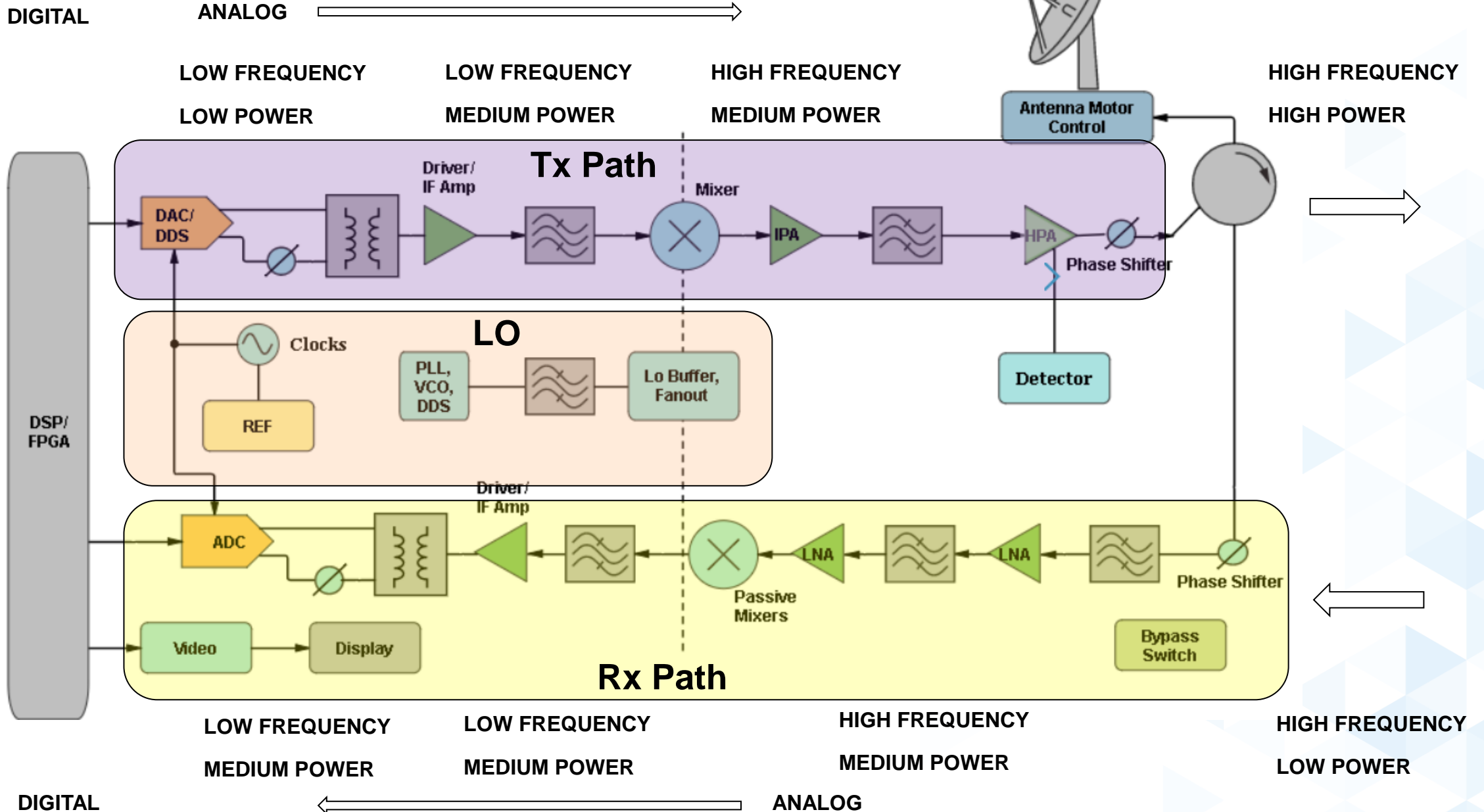


Agenda

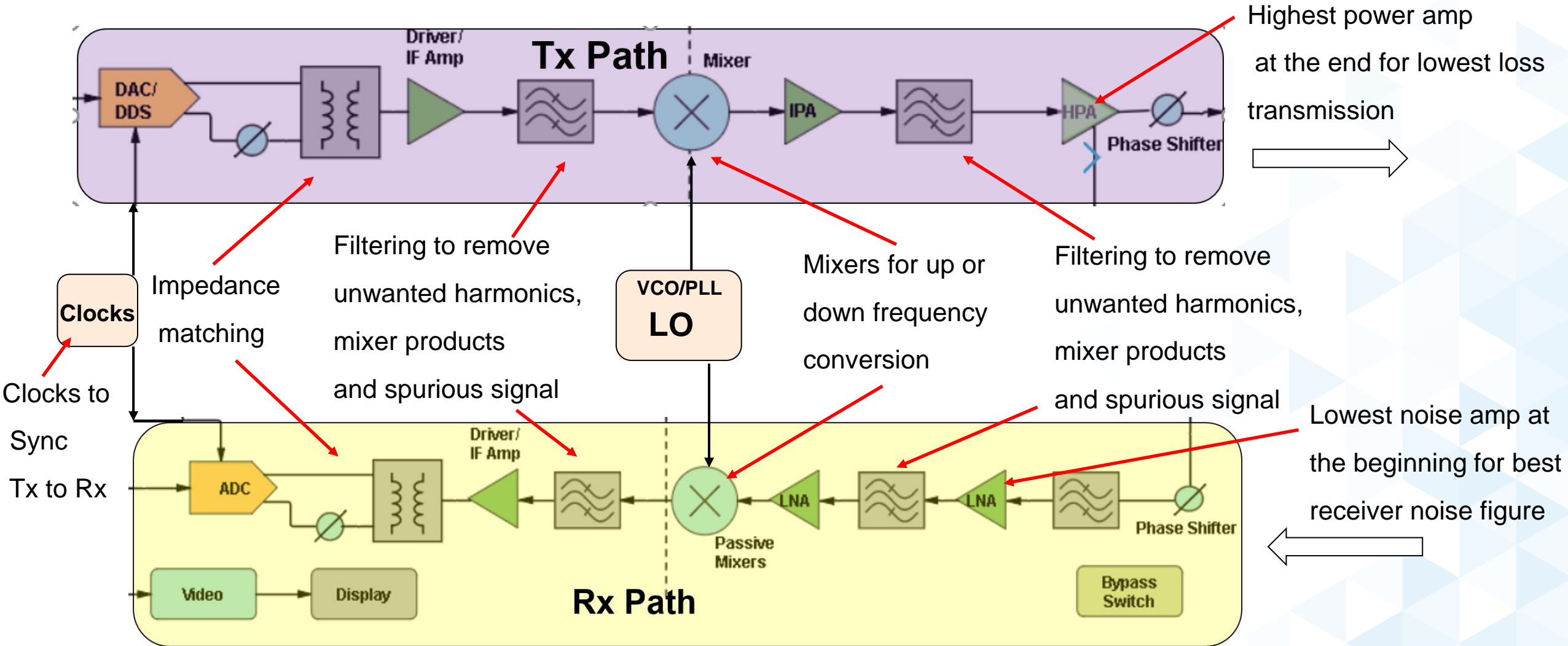
- RF Signal Chains
 - Radar and communications signal chains
 - Design goals
- Technology Consideration
 - GaAs vs. SOI switch
 - GaAs vs. GaN power amplifier
- Level of Integration
 - Integration advantages
- Component Matching
 - Mismatch power loss
 - Interstage matching
- PCB Layout Technology
 - Shielding and isolation
 - Layout guidelines
- Dynamic Range
 - RF performance improvements
- Improving the Signal Chain Performance
- Tools

RF Signal Chain

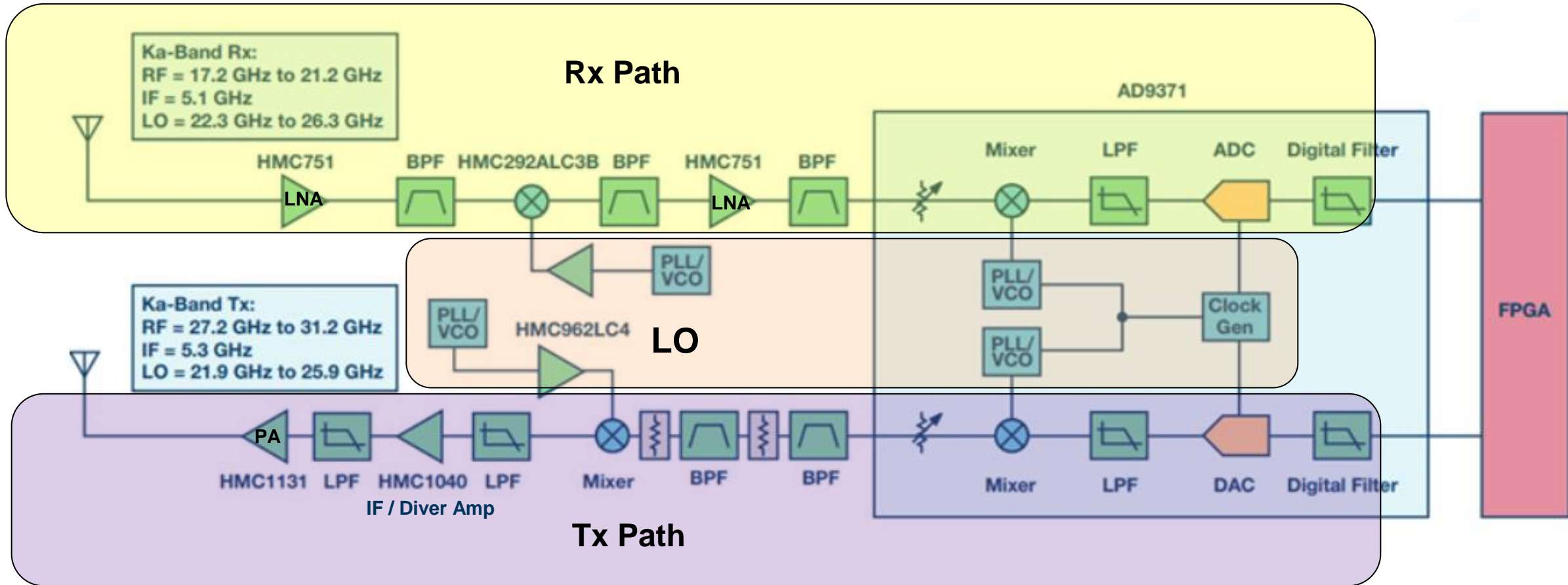
Super Heterodyne Radar Signal Chain



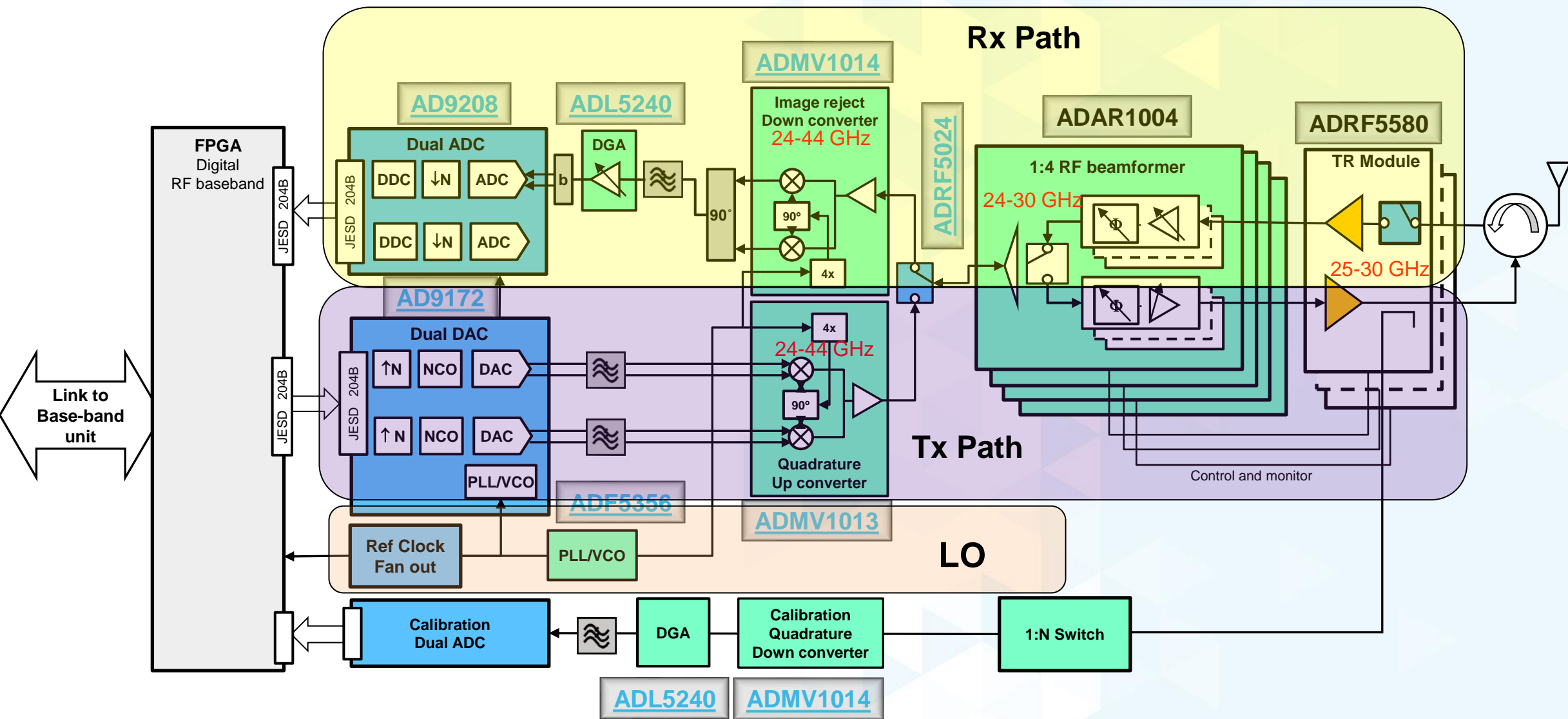
RF Signal Chain Lineup



SATCOM Signal Chain



5G Signal Chain (24 GHz – 30 GHz)



Design and Optimization Goals

- Smallest Size / Weight
- Lowest Cost
- Best RF Performance for the Application
- Lowest Power Consumption
- Ease of Use

Process Technology Considerations

Gallium Arsenide(GaAs)? Gallium Nitride (GaN)?
Silicon (Si)? Silicon Germanium(SiGe)? Silicon on Insulator (SOI)?

We consider the best technology to use by...

- Foundry Availability
- Frequency / Speed
- Power level required for the application
- Noise and linearity considerations
- Amount of integration capability
- Cost vs. throughput

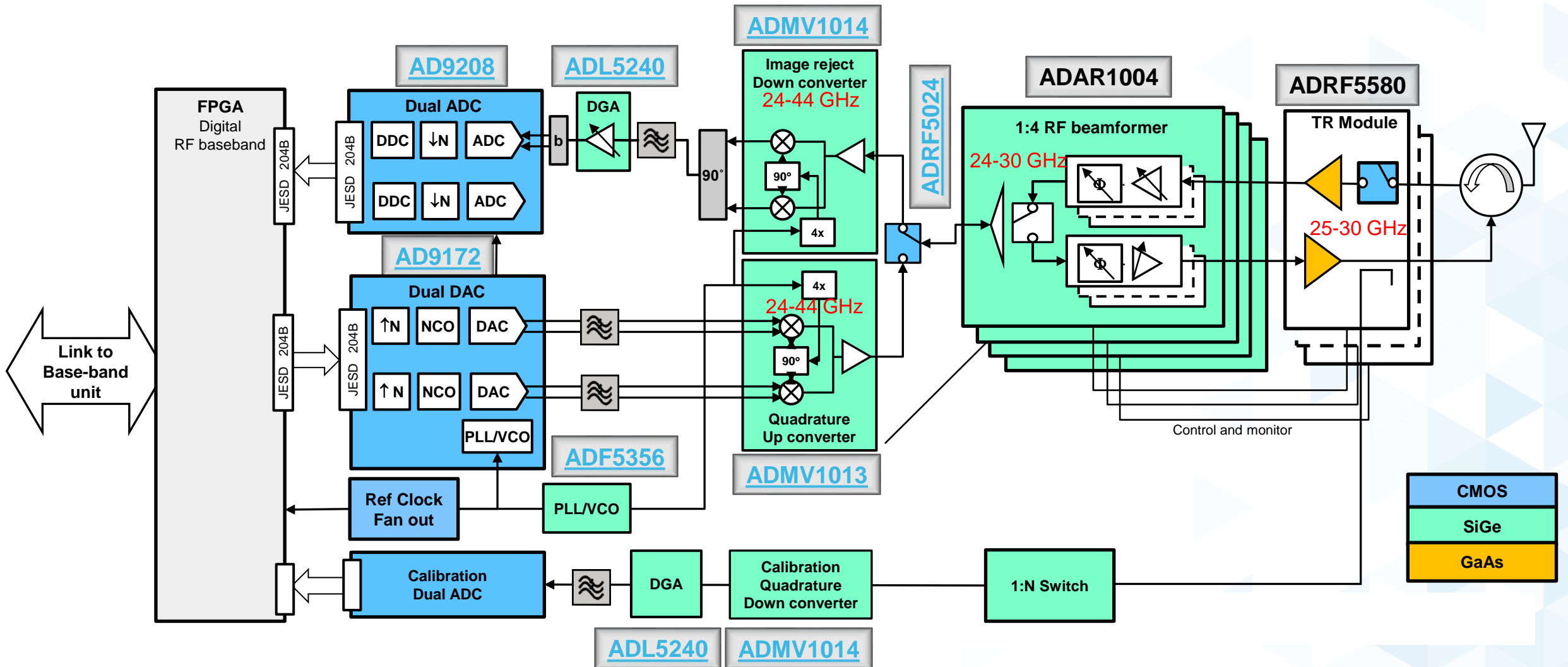
GaAs? GaN? Si? SiGe? SOI? – Application Specific

RF Fabrication

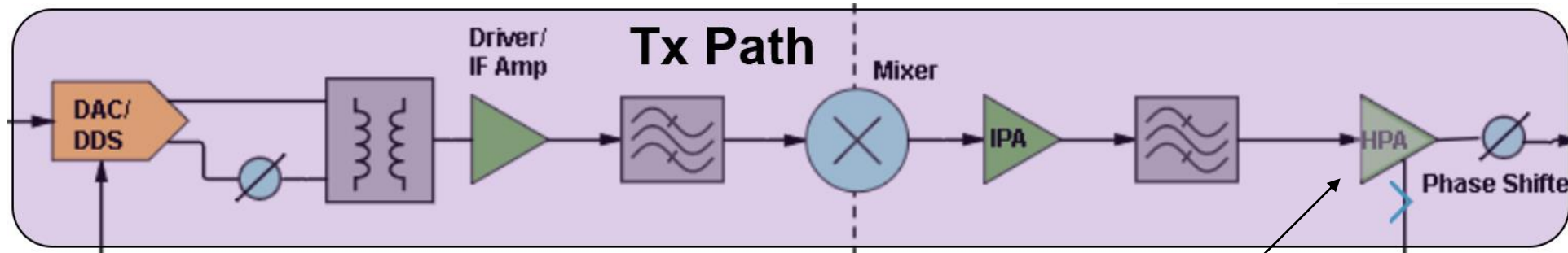
Foundry

<u>Technology</u>	<u>Availability</u>	<u>Frequency</u>	<u>Power</u>	<u>Linearity</u>	<u>Cost</u>	<u>Integration</u>
Silicon	High	Low	Low	Medium	Low	High
Silicon Germanium	Low	Low to High	Medium	High	High	High
Silicon on Insulator	High	Low to High	Medium	High	Low	High
GaAs	Medium	High	Medium	Low	Low	Low
GaN	Low	High	High	Low	High	Low

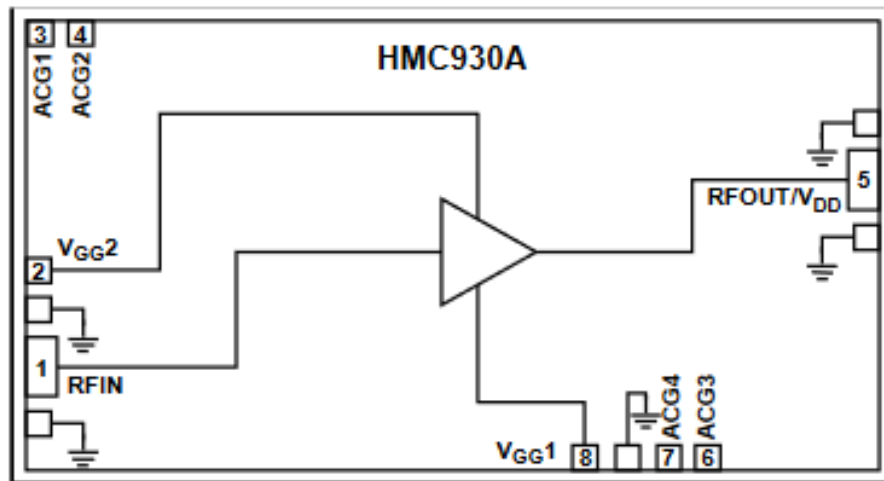
GaAs? GaN? Si? SiGe? SOI? – Mixed Technologies



Power Amplifier GaAs vs. GaN – Application Specific Example



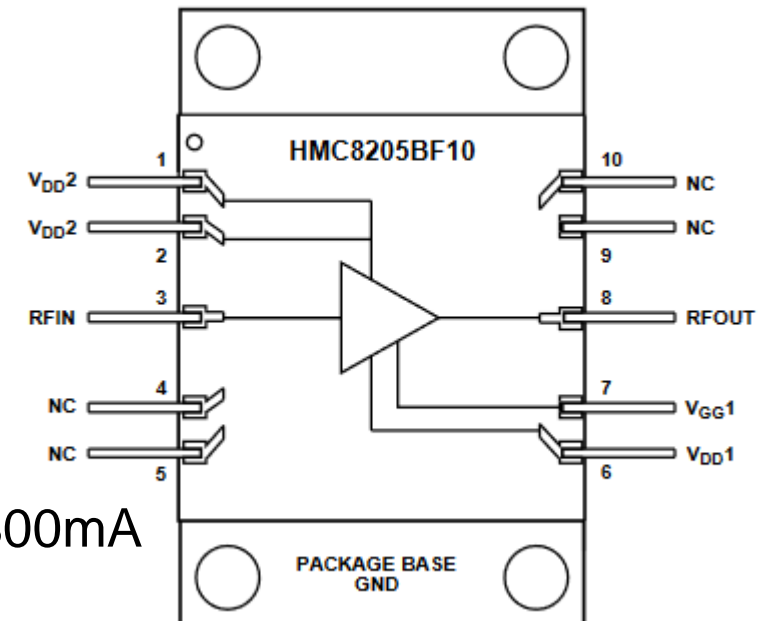
**GaAs, pHEMT, MMIC,
0.25 W Power Amplifier, DC to 40 GHz**



10V @ 175mA

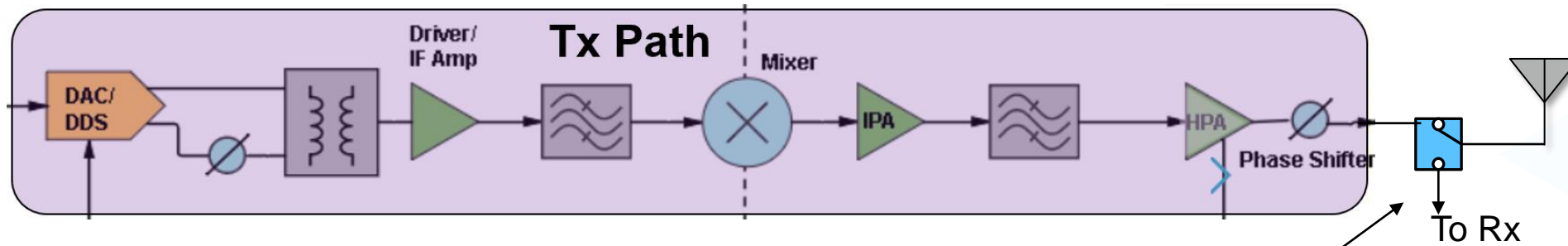
**0.3 GHz to 6 GHz, 35 W, GaN
Power Amplifier**

OR



50V @ 1300mA

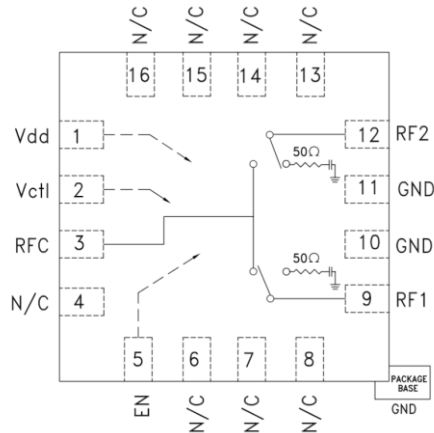
T/R Switch GaAs vs SOI – Technology Advancement



GaAs

**HIGH ISOLATION SPDT
NON-REFLECTIVE SWITCH, DC - 6 GHz**

HMC849



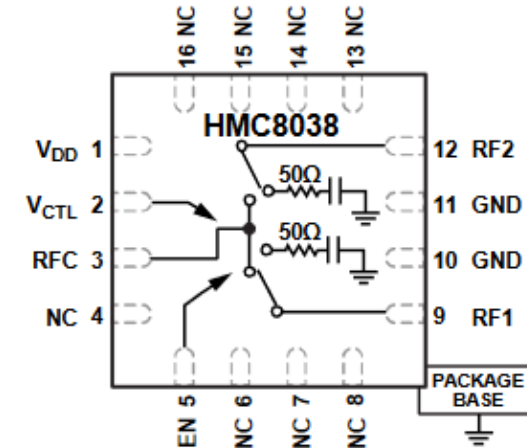
IP3 = 52 dBm

Input P1dB = 33 dBm

SOI

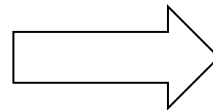
**High Isolation, Silicon SPDT,
Nonreflective Switch, 0.1 GHz to 6.0 GHz**

HMC8038



IP3 = 60 dBm

Input P1dB = 36 dBm



Level of Integration

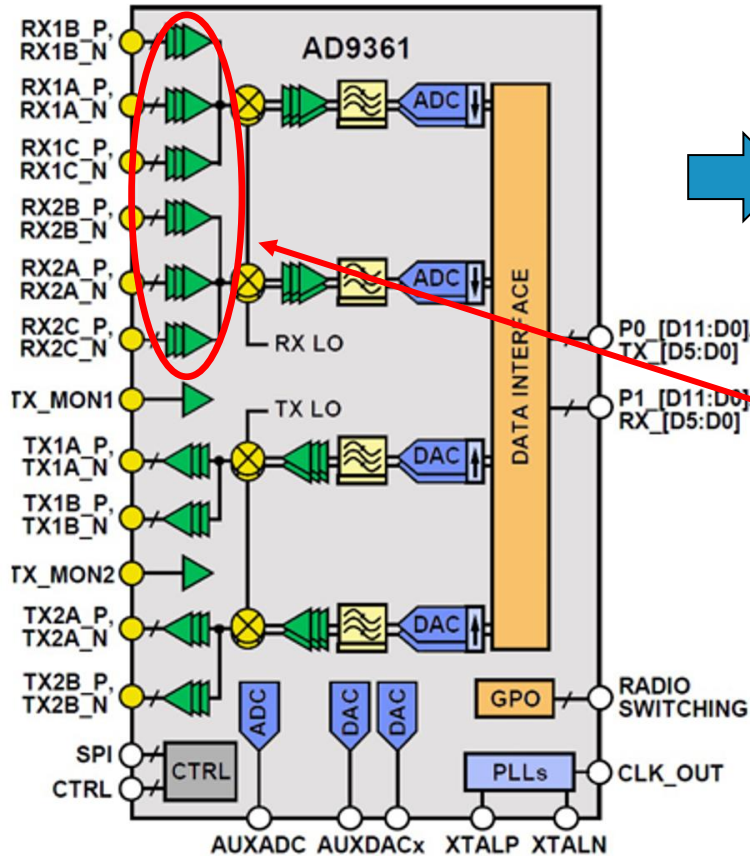
Level of Integrations

- Chip level
- Module Level
- System Level

Chip level Integration – Application Specific Example

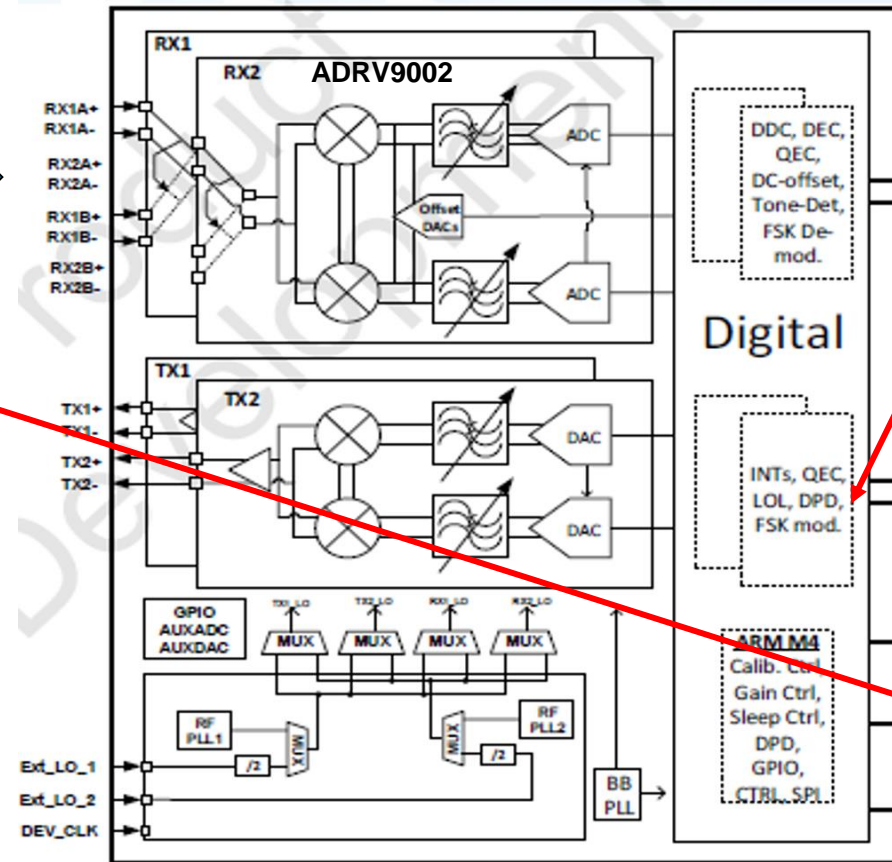
Fixed Cell Site

CATALINA – AD9361



Mobile Cell Site

NAVASSA – ADRV9002

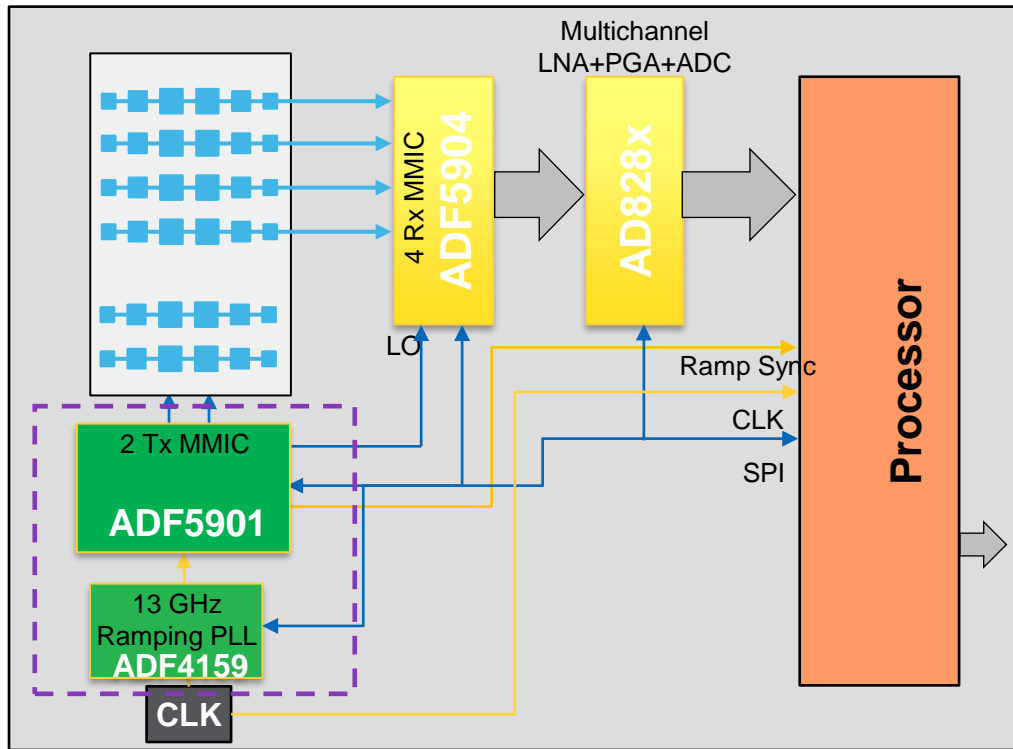


Added digital predistortion to improve dynamic range

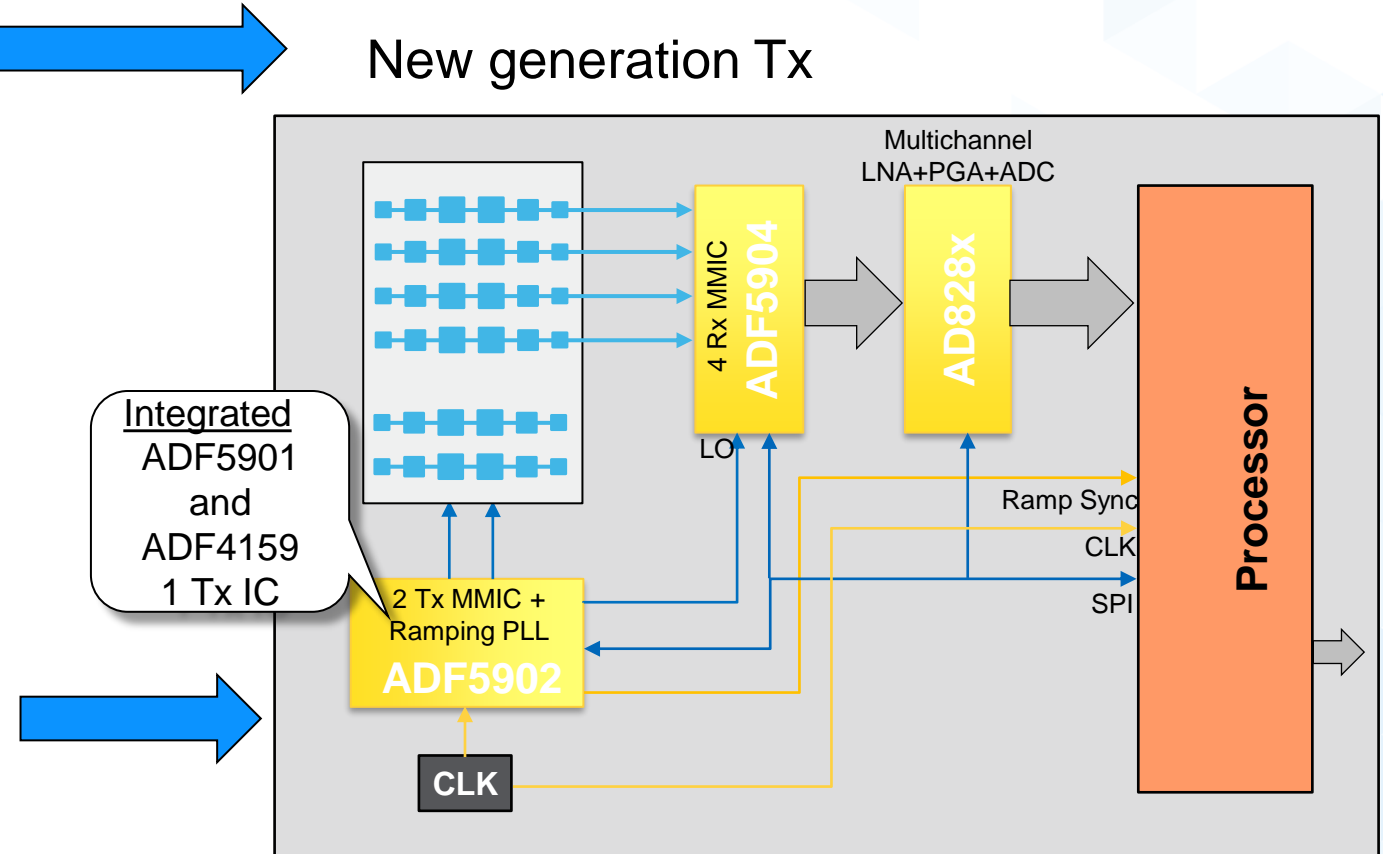
Remove LNAs to increase agility and flexibility

Chip Level Integration - 24 GHz Radar System ADF5901 and ADF4159 into ADF5902

Current generation Tx



New generation Tx



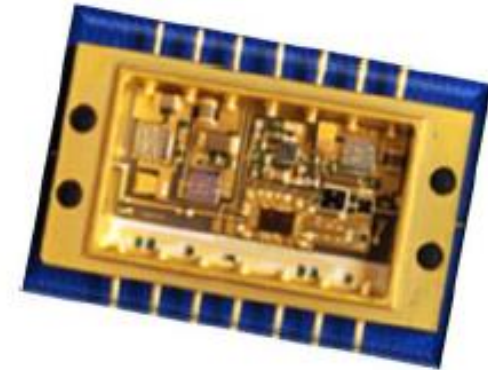
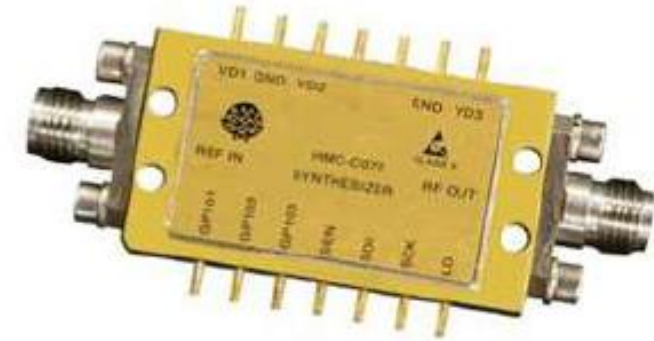
Module Level Integration – High Reliability Products

Integrated Die & Passives

- Amplifier
- VCO
- Diodes
- Prescaler
- Synthesizer
- Voltage Regulators
- Op Amp

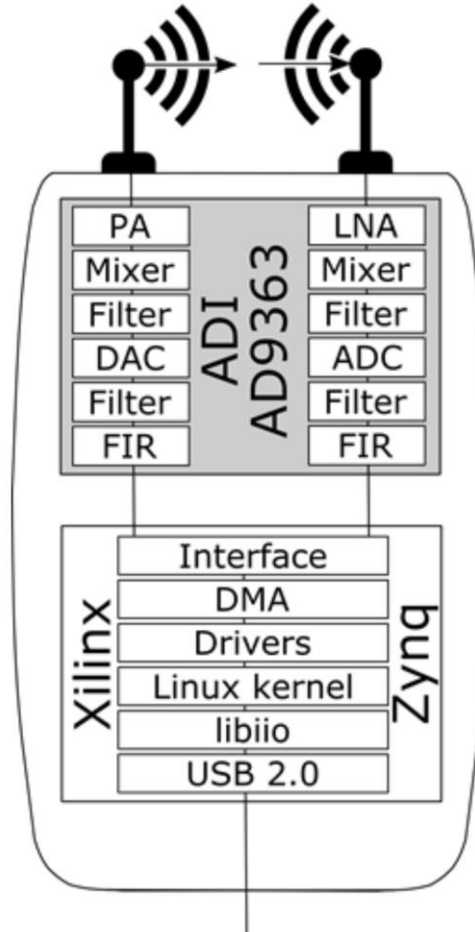
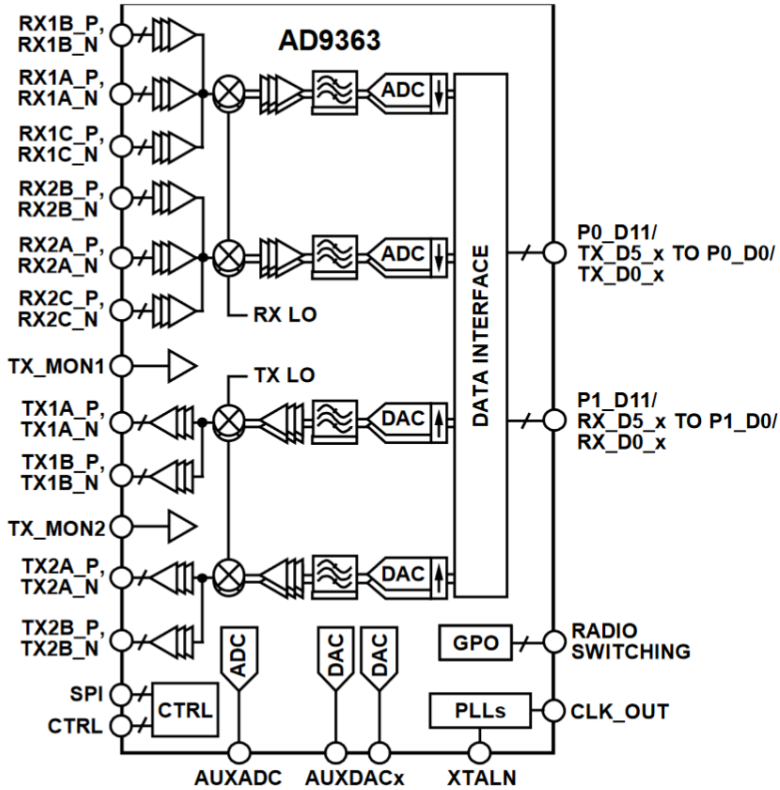
Features

- Octave Bandwidth
- Commercial & Hi Rel version
- Contains MMIC that are only available within ADI in die form



System Level Integration

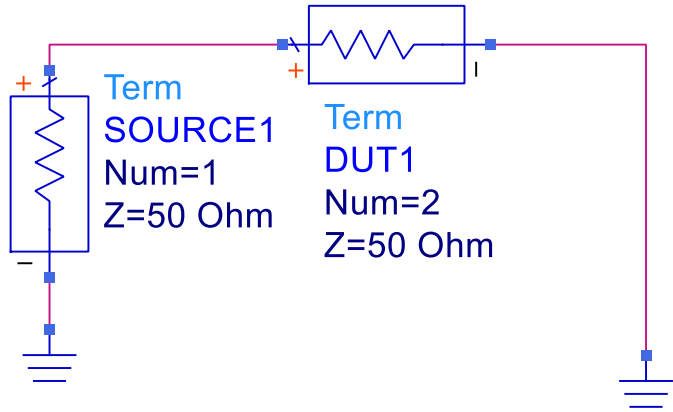
ADALM-PLUTO – Fully integrated SDR with software



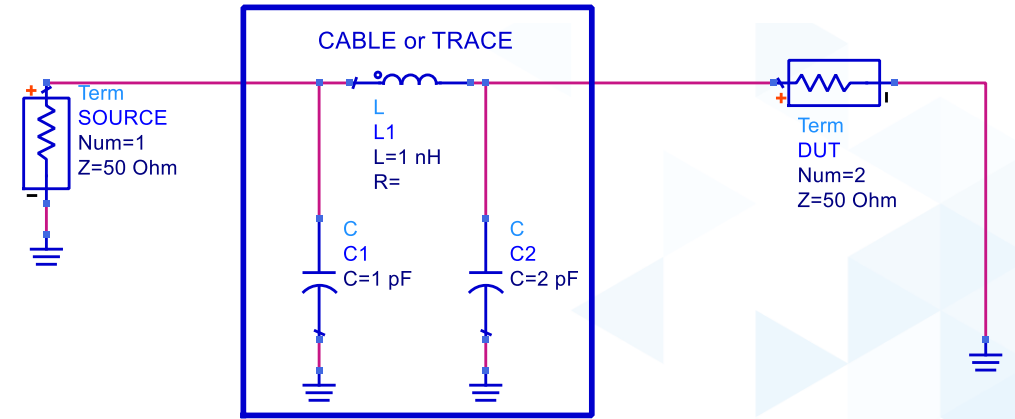
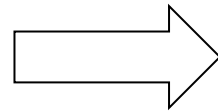
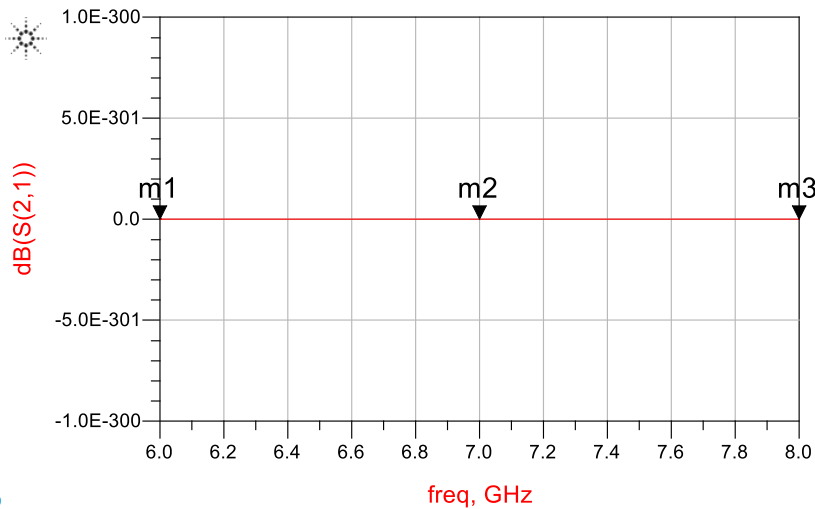
Component Matching

Component Matching

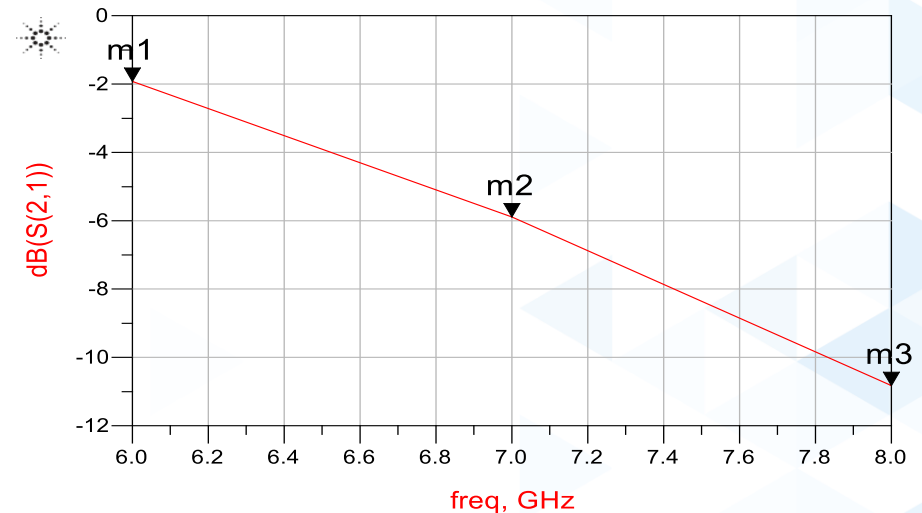
- When 2 impedances are different and connected, reflections can occur causing power loss.



m1 freq=6.000GHz dB(S(2,1))=0.000	m2 freq=7.000GHz dB(S(2,1))=0.000	m3 freq=8.000GHz dB(S(2,1))=0.000
-----------------------------------------	-----------------------------------------	-----------------------------------------



m1 freq=6.000GHz dB(S(2,1))=-1.923	m2 freq=7.000GHz dB(S(2,1))=-5.891	m3 freq=8.000GHz dB(S(2,1))=-10.828
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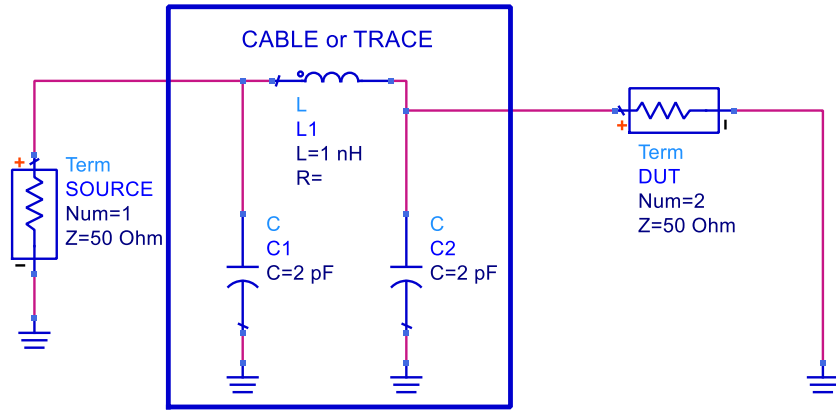


Component Matching – Power Loss

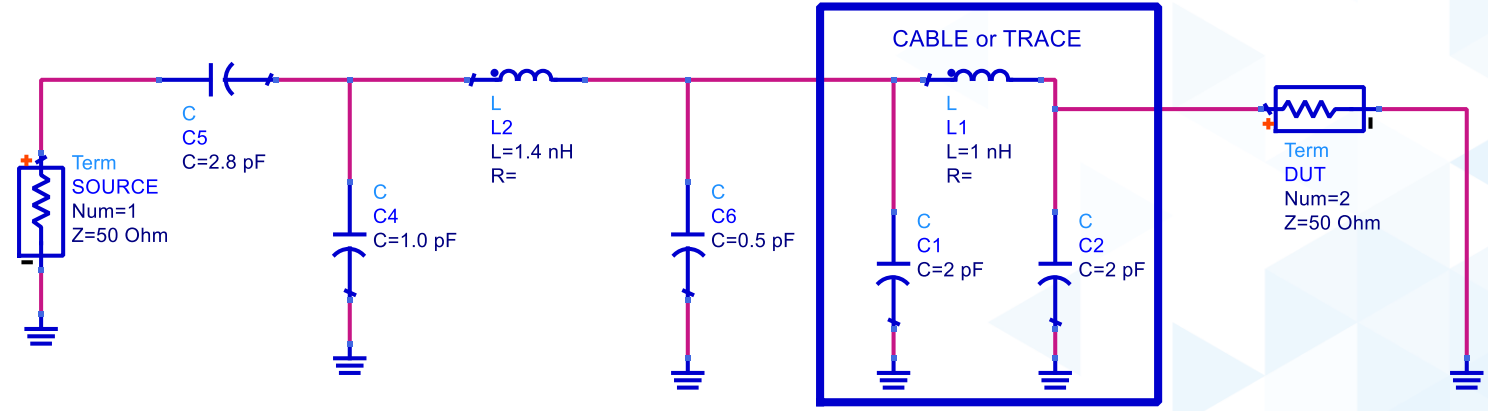
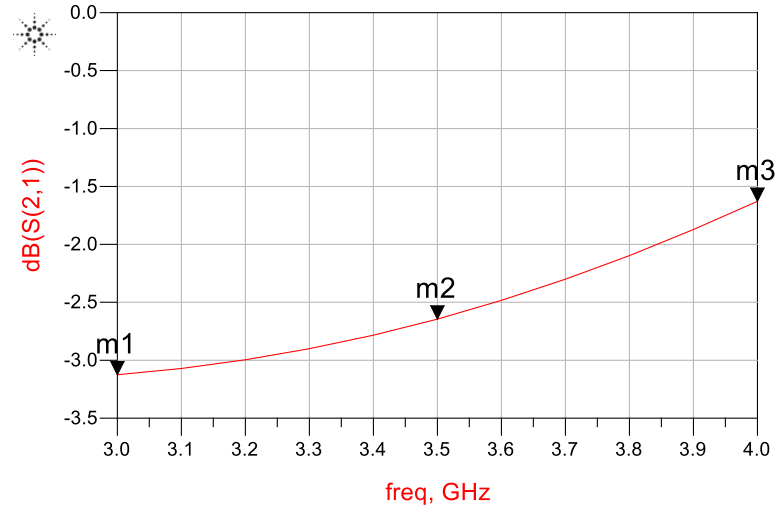
Source Impedance (ohms)	Load impedance (ohms)	Reflected Power (%)	Through Power (%)
50	1000	81.86	18.14
50	50.00	0.00	100.00
50	33.33	4.00	96.00
50	25.00	11.11	88.89
50	20.00	18.36	81.64
50	16.66	25.00	75.00
50	11.30	36.00	64.00
50	10.00	44.45	55.55
50	5.00	66.95	33.05

Component Matching

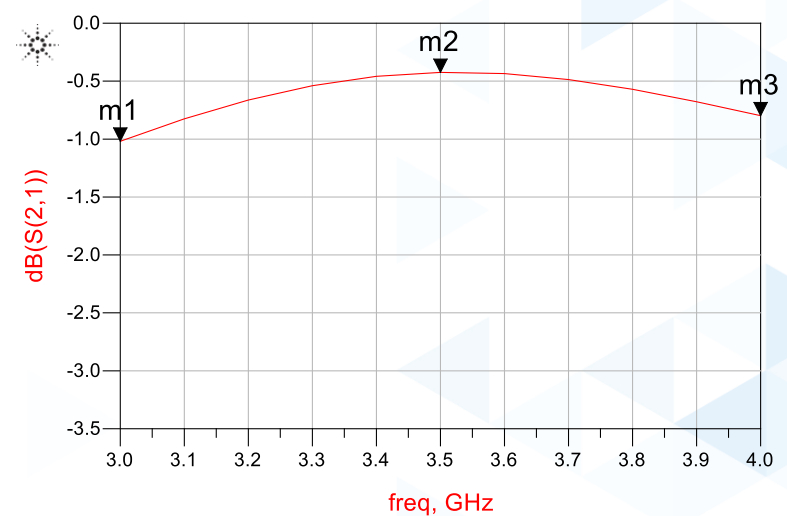
- Proper impedance matching by components or transmission line design can reduce or eliminate reflections.



m1 freq=3.000GHz dB(S(2,1))=-3.126	m2 freq=3.500GHz dB(S(2,1))=-2.645	m3 freq=4.000GHz dB(S(2,1))=-1.628
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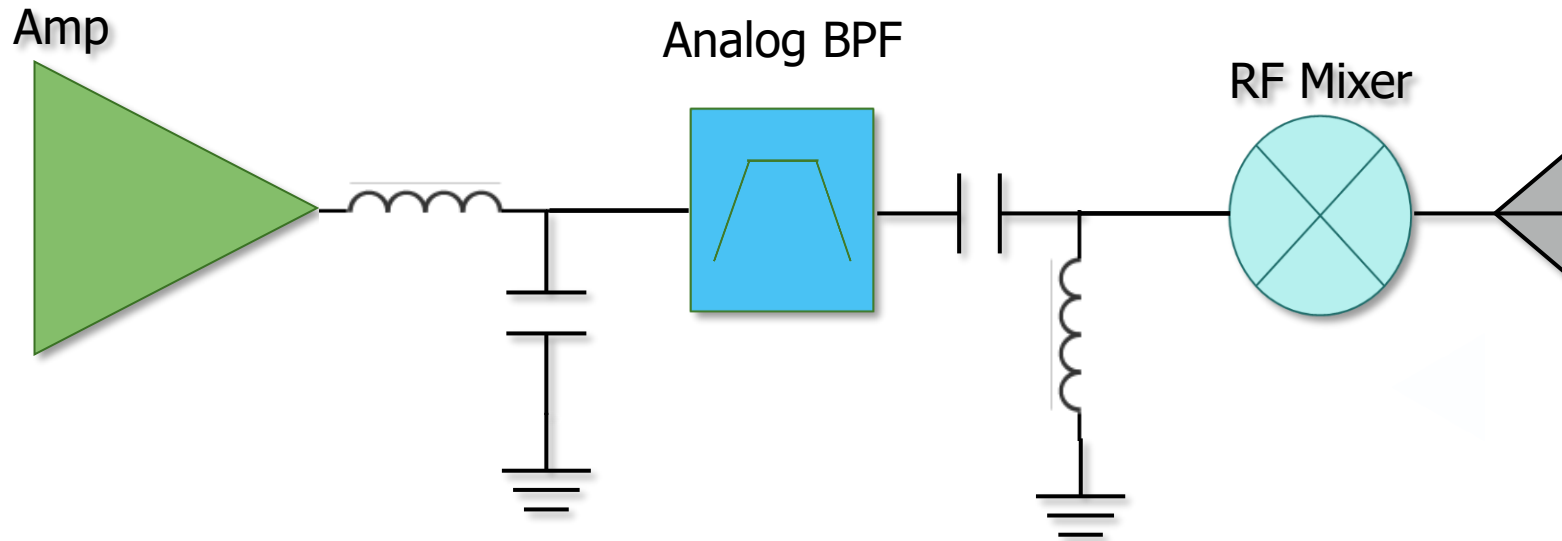


m1 freq=3.000GHz dB(S(2,1))=-1.019	m2 freq=3.500GHz dB(S(2,1))=-0.424	m3 freq=4.000GHz dB(S(2,1))=-0.799
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Inter-Stage Component Matching

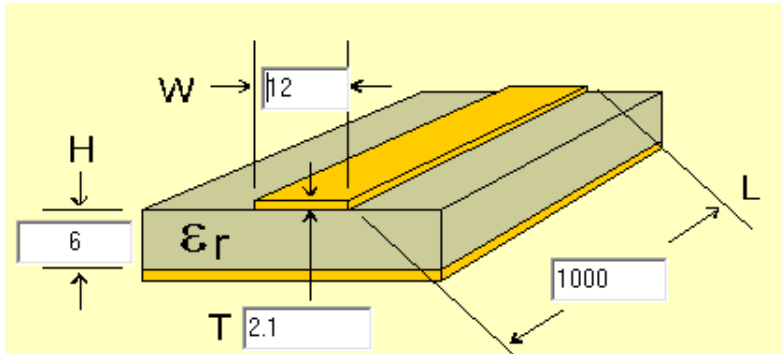
- Inter-Stage matching can be very challenging. Very often it is difficult to determine the magnitude of loss due to integrated interstage matching.



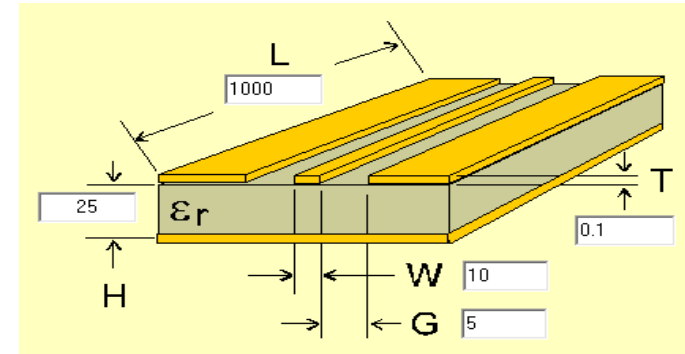
PCB Layout Technology

Printed Circuit Board - Technology

Microstrip – Lowest loss at high frequencies

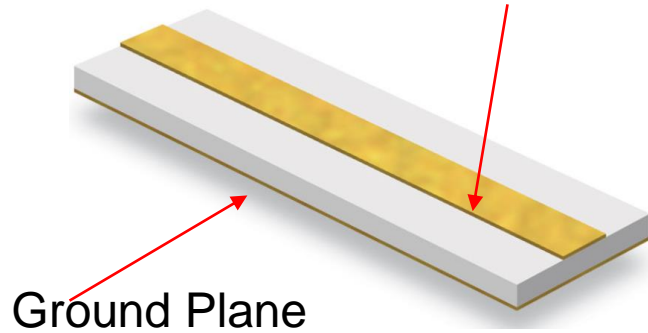


Coplanar – Best isolation



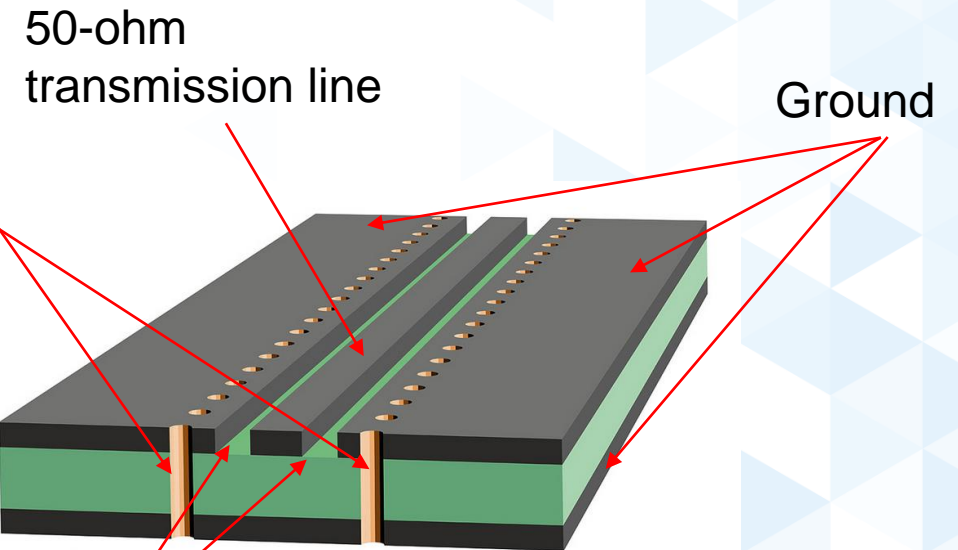
No vias used as no top-level ground exist.

50-ohm transmission line



Ground Plane

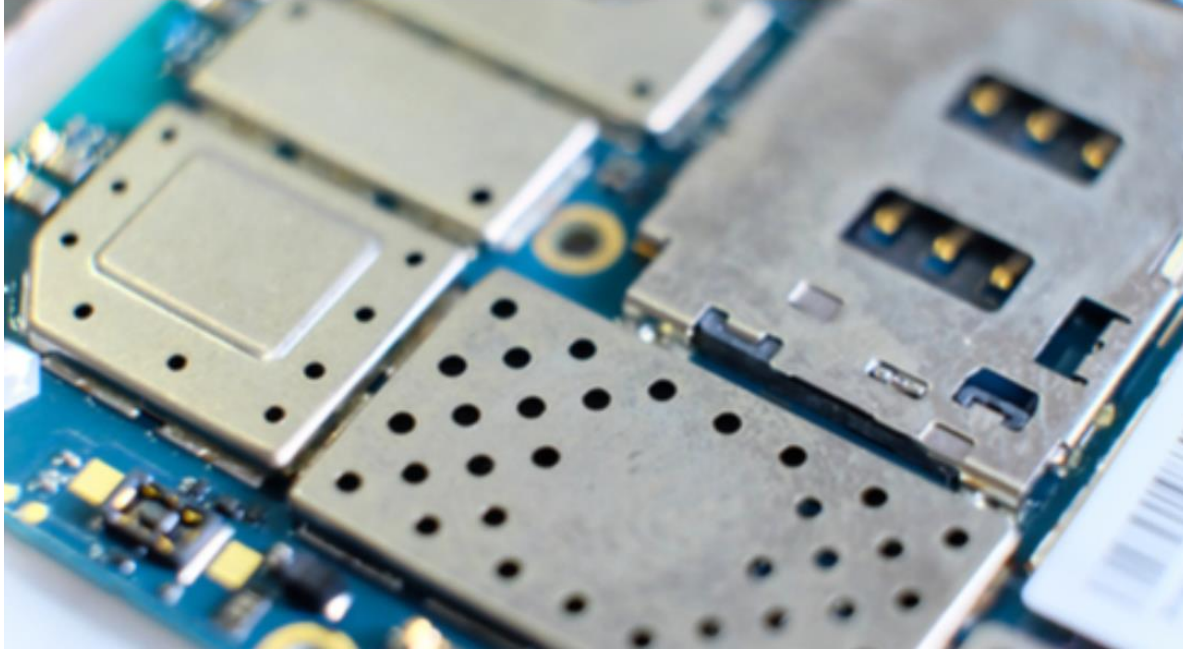
Copper plated via fences connects top ground planes to bottom ground plane



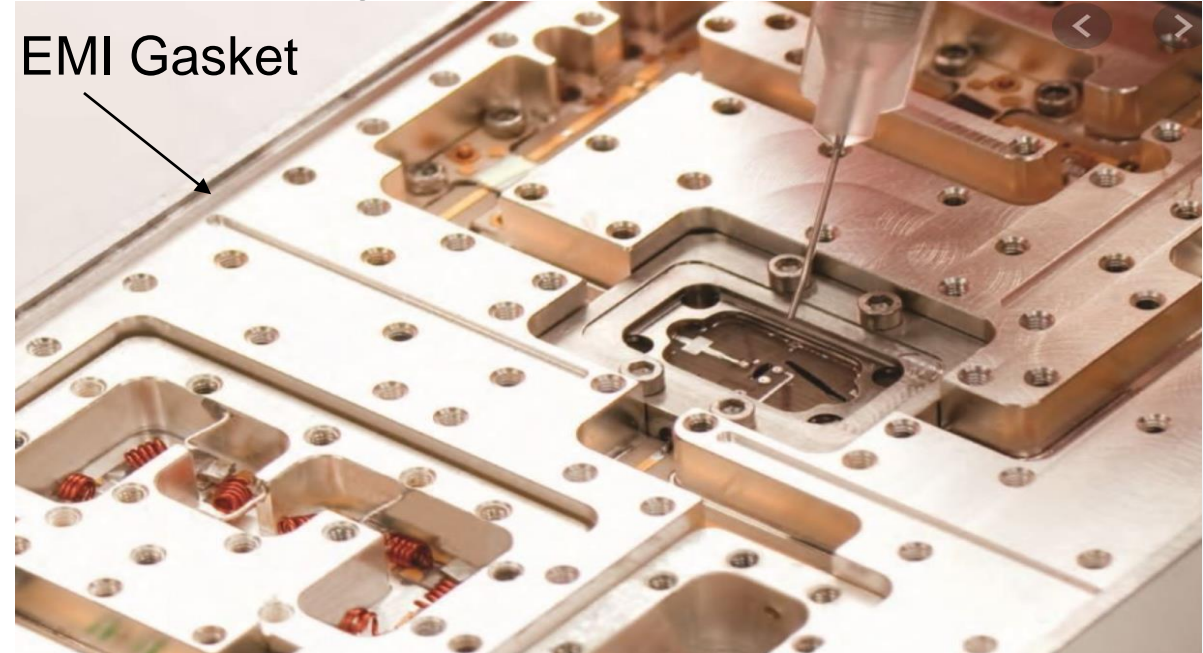
Gap - No copper

RF Printed Circuit Board – Shielding and Isolation

Metal shielding placed over components and traces



Machined module housings isolating sensitive high frequency circuits



- ▶ RF shieldings and metal housings separates transmit and receive signals
- ▶ EMI gaskets prevents outside signals from interfering
- ▶ RF shielding isolates RF signals from DC power and digital / clock signals

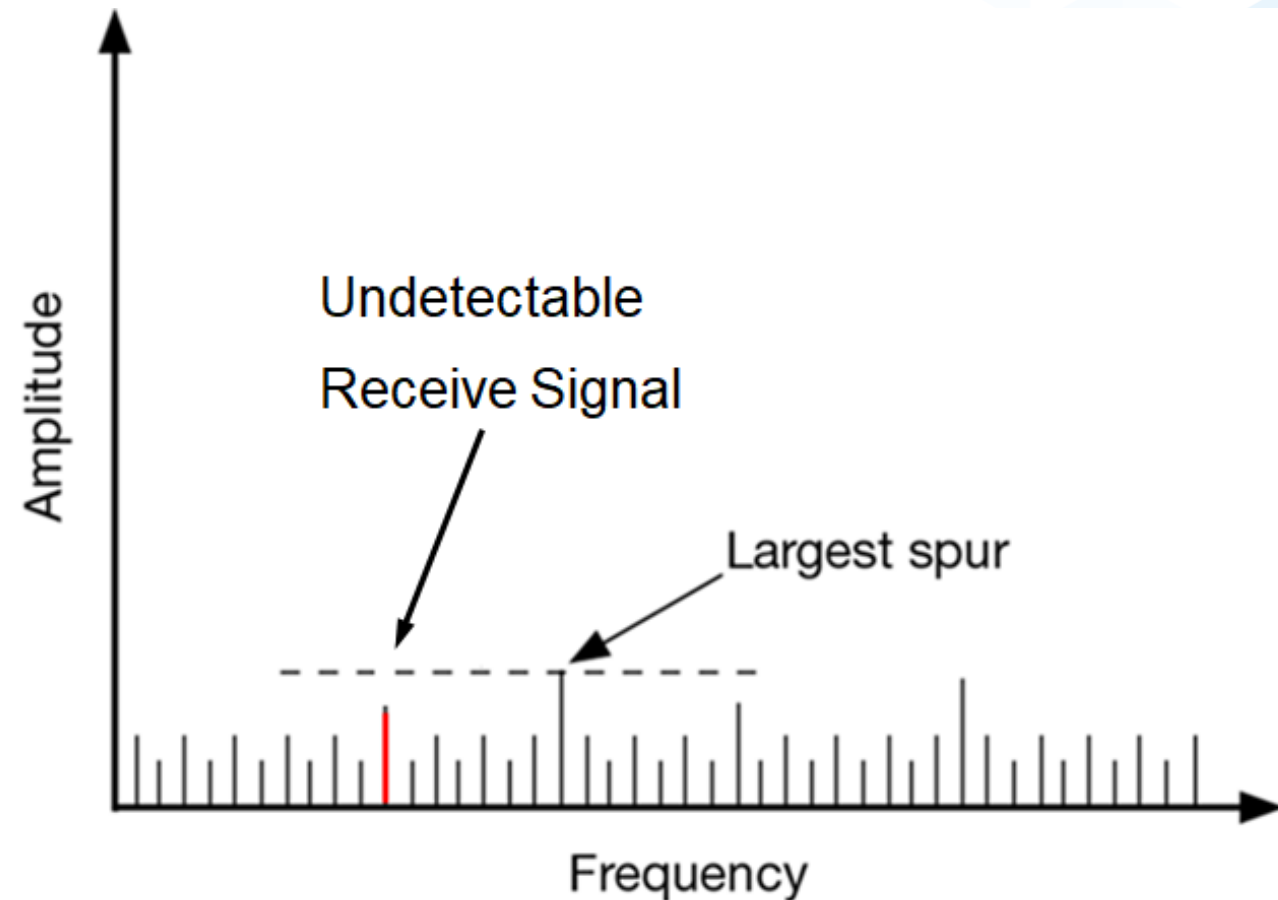
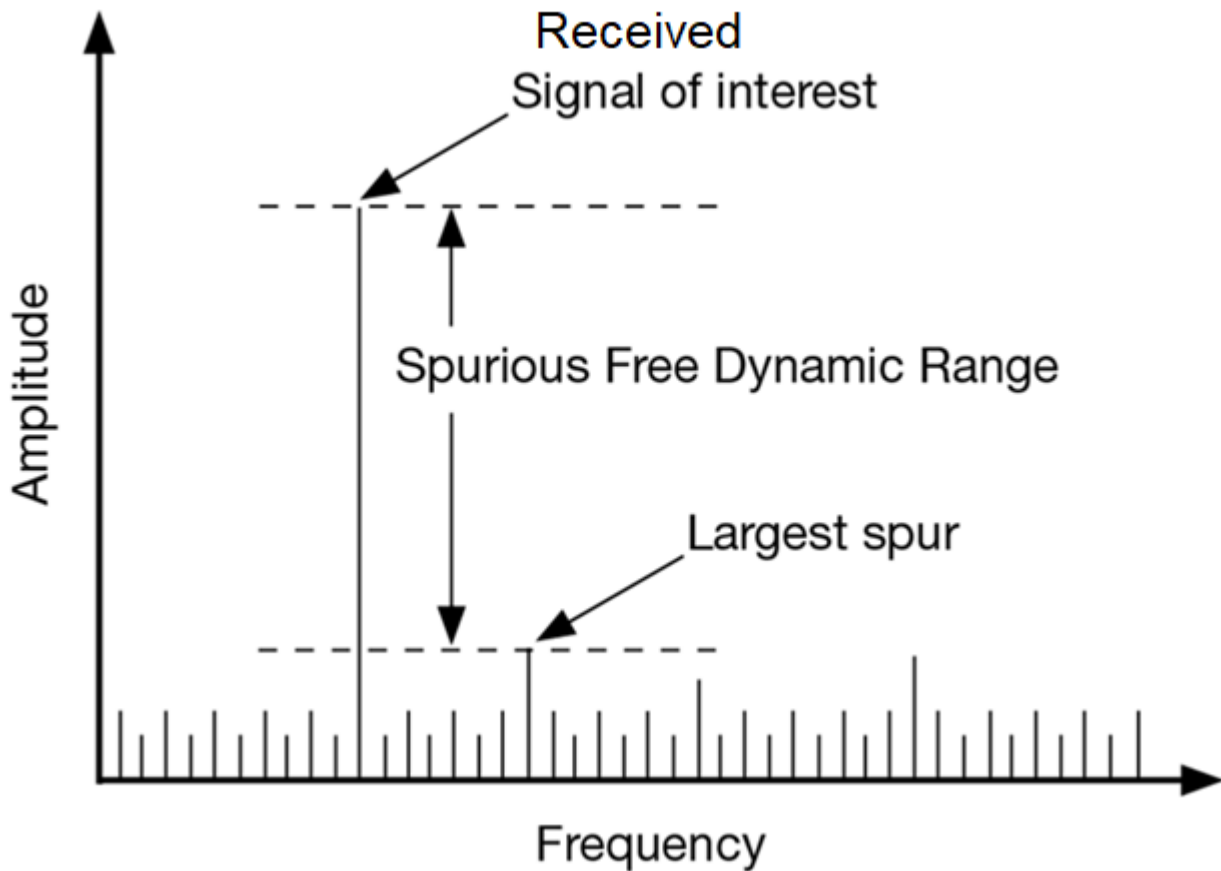
Printed Circuit Board Signal Integrity Guidelines

- No sharp 90-degree corners on RF traces. Only use these under specific conditions after EM modeling (ie. stubs, filters, DC taps, etc)
- Always keep an RF ground plane directly under the RF signal layer
- Use coplanar technology when RF isolation is critical. Use microstrip when losses are critical.
- When isolation is required between 2 RF signals on the same layer, it is best to have them perpendicular to each other
- When isolation is required between 2 parallel RF signals, provide at least 4 trace width spacings from trace edge to trace edge.
- Use lots of ground vias. Use at least 2 rows of offset ground vias on each side of coplanar traces whenever possible.
- To isolate RF components (ie, TX to RX), shielding is always the best option.

Dynamic Range

Dynamic Range – What is it?

Dynamic range is the measurement of a receiver's ability to process a range of input powers from the antenna. If the signal is too weak, it can't be picked out from the noise.



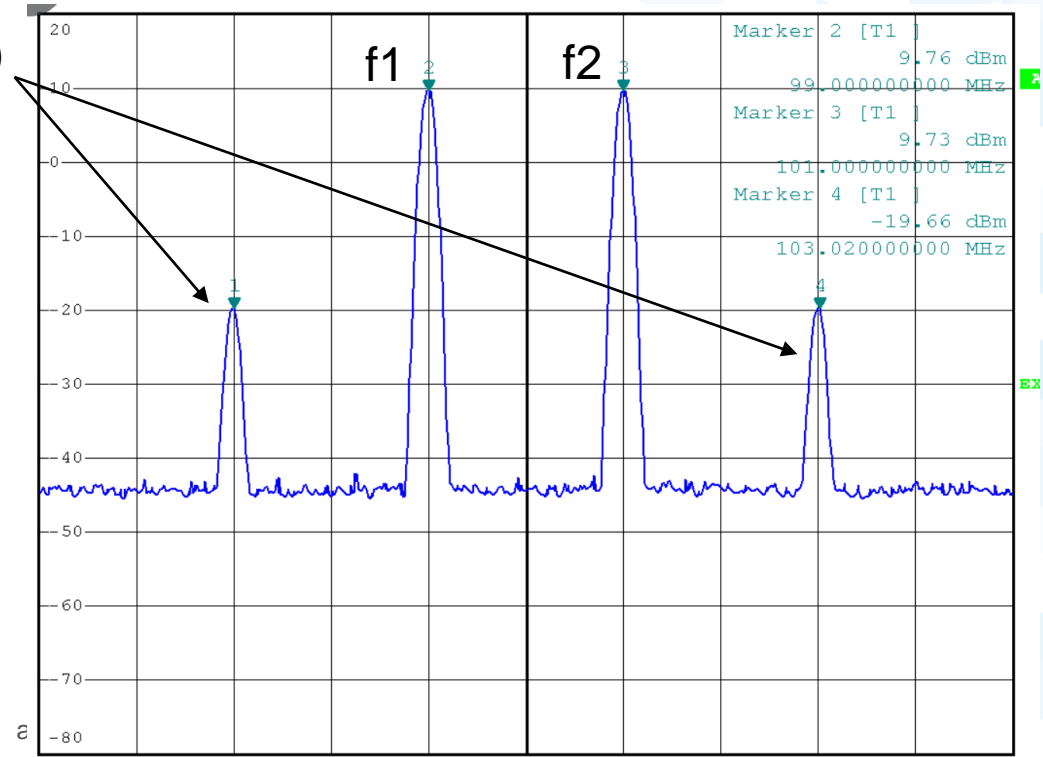
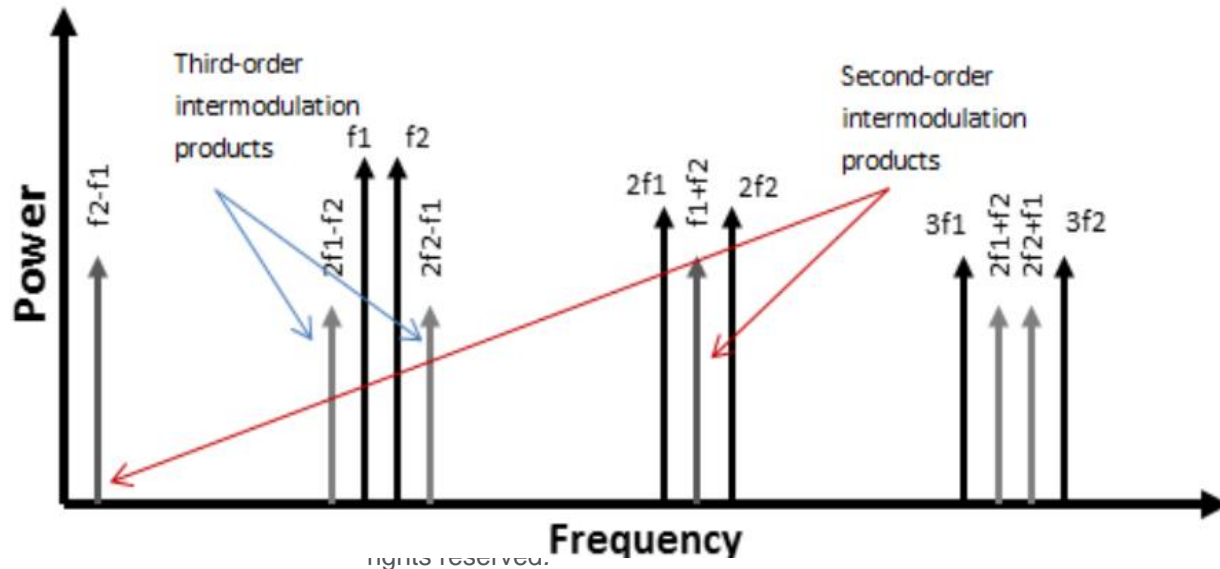
Dynamic Range – Optimization

- Improve linearity
- Lower noise level
- Reduce spurious signals
- Minimize transmit and receive path losses

Dynamic Range – Linearity

2nd or 3rd Order Intercept Points (IP2 or IP3), also known as linearity measurements, measures spurious related signals created when multiple tones are presented to a device or a receive signal chain. These spurious products, also known as intermodulation distortion products (IMD), are often within a desired receiver's bandwidth reducing dynamic range. Greater distance between transmitted signal and IMD signals, better the IP2 / IP3 !!

Third-order
Intermodulation
Products (IMD)

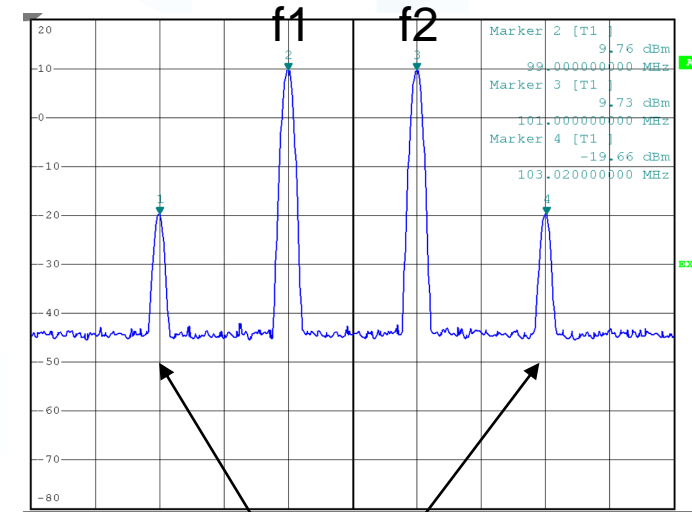


Dynamic Range – Linearity

Output 3rd order intercept (OIP3) =
 $(f1(\text{dBm}) - \text{lower } 3^{\text{rd}} \text{ intermod product (dBm)})/2 + f1(\text{dBm})$ &
 $(f2(\text{dBm}) - \text{upper } 3^{\text{rd}} \text{ intermod product (dBm)})/2 + f2(\text{dBm})$

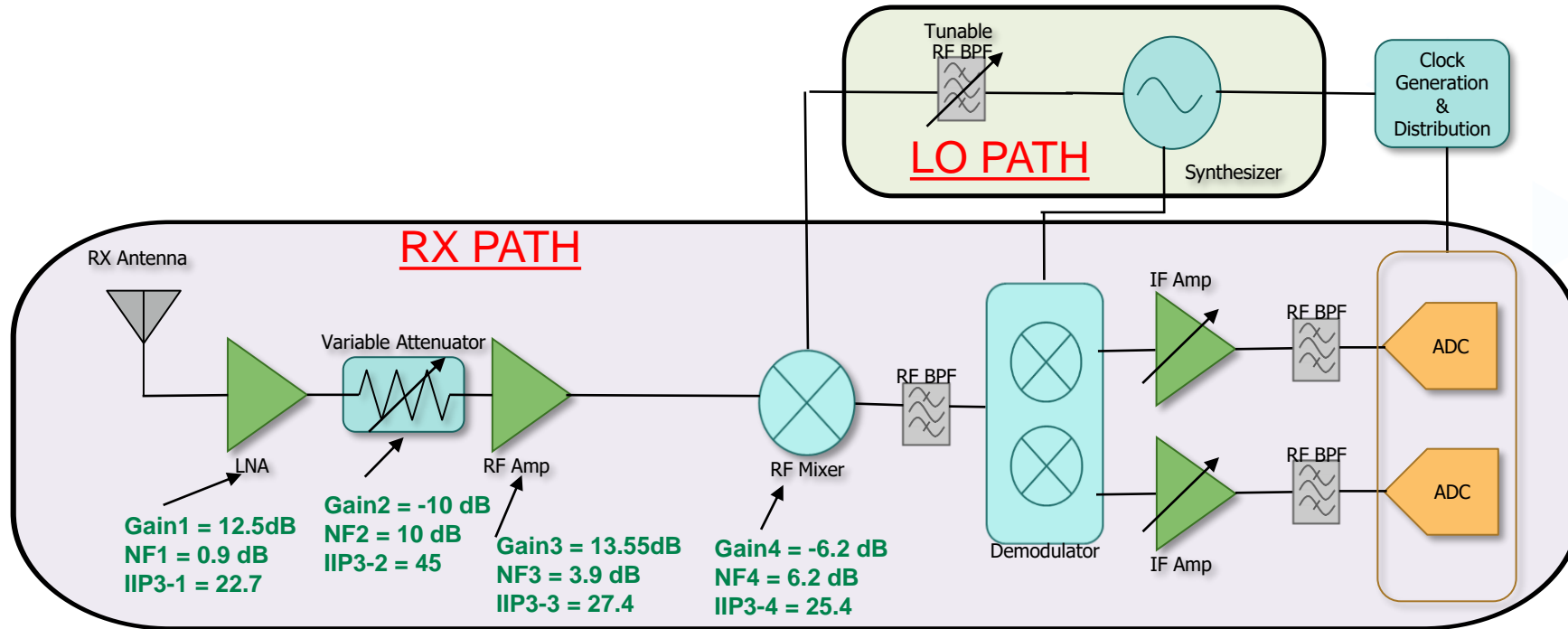
Example... $f1(\text{output power}) = 20 \text{ dBm}$, lower 3rd intermod = 4 dBm
 $\text{OIP3} = ((20 - 4)/2) + 20$
 $\text{OIP3} = 28 \text{ dBm}$

For Input 3rd order intercept (IIP3) =
 $(f1(\text{dBm}) - \text{lower } 3^{\text{rd}} \text{ intermod product (dBm)})/2 + \text{input power(dBm)}$ &
 $(f2(\text{dBm}) - \text{upper } 3^{\text{rd}} \text{ intermod product (dBm)})/2 + \text{input power(dBm)}$



Third-order
Intermodulation
Products (IMD)

Dynamic Range – Cascaded Intermodulation

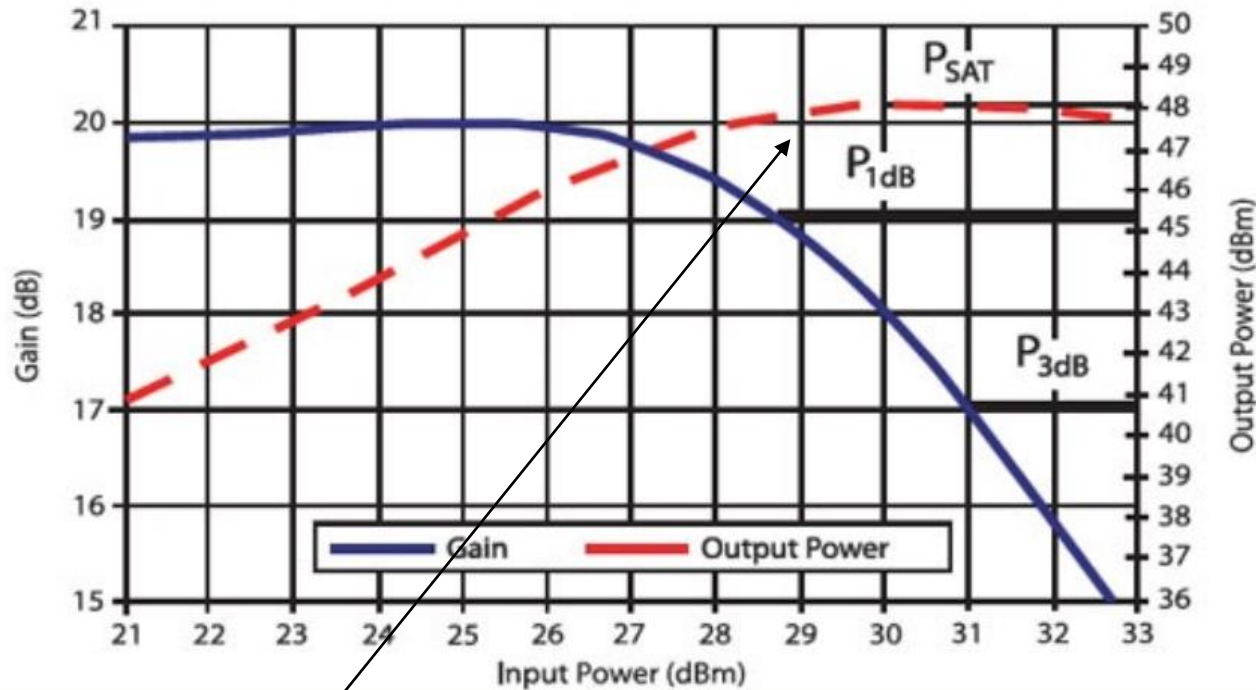


$$\text{Total Input IP3 (mW)} = 1 / (1/(\text{IIP3}(1)*G2*G3*G4)) + (1/(\text{IIP3}(2)*G3*G4)) + (1/(\text{IIP3}(3) *G4)) + (1/(\text{IIP3}(4)))$$

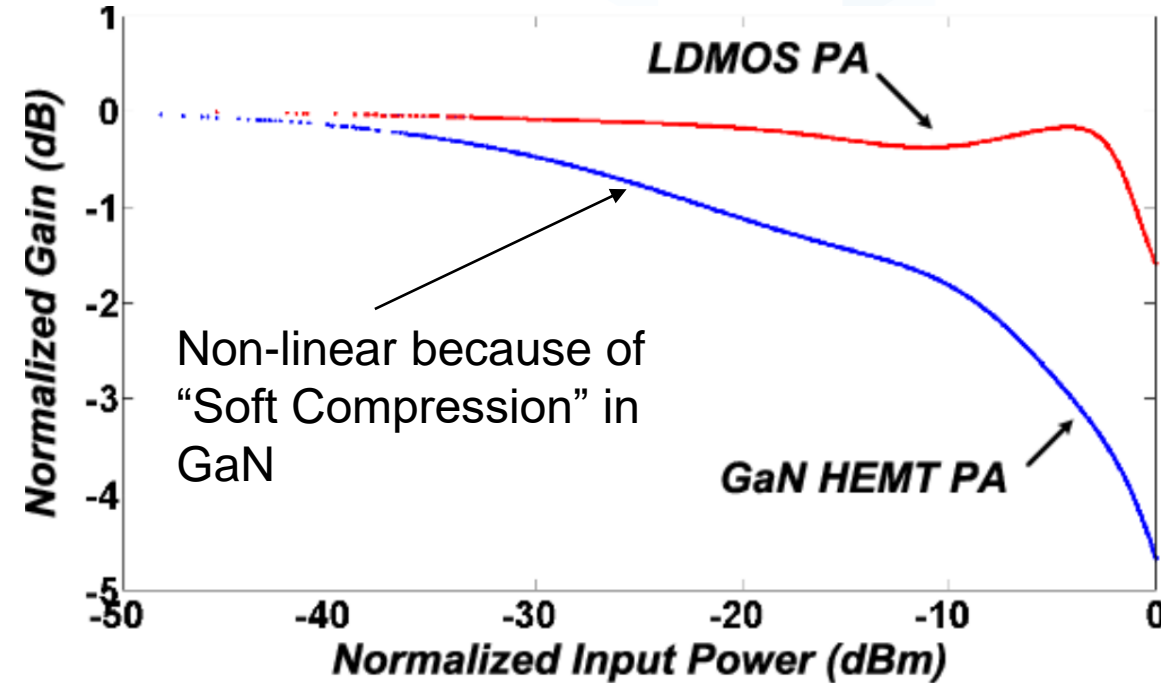
$$\text{Input IP3(dBm)} = 10 \log (\text{IIP3 in mW})$$

Dynamic Range – Power Handling and Compression

1dB compression (P_{1dB}) helps determine how much usable power the part can deliver. It can also tell us the linear and non-linear input / output power levels in the signal chain

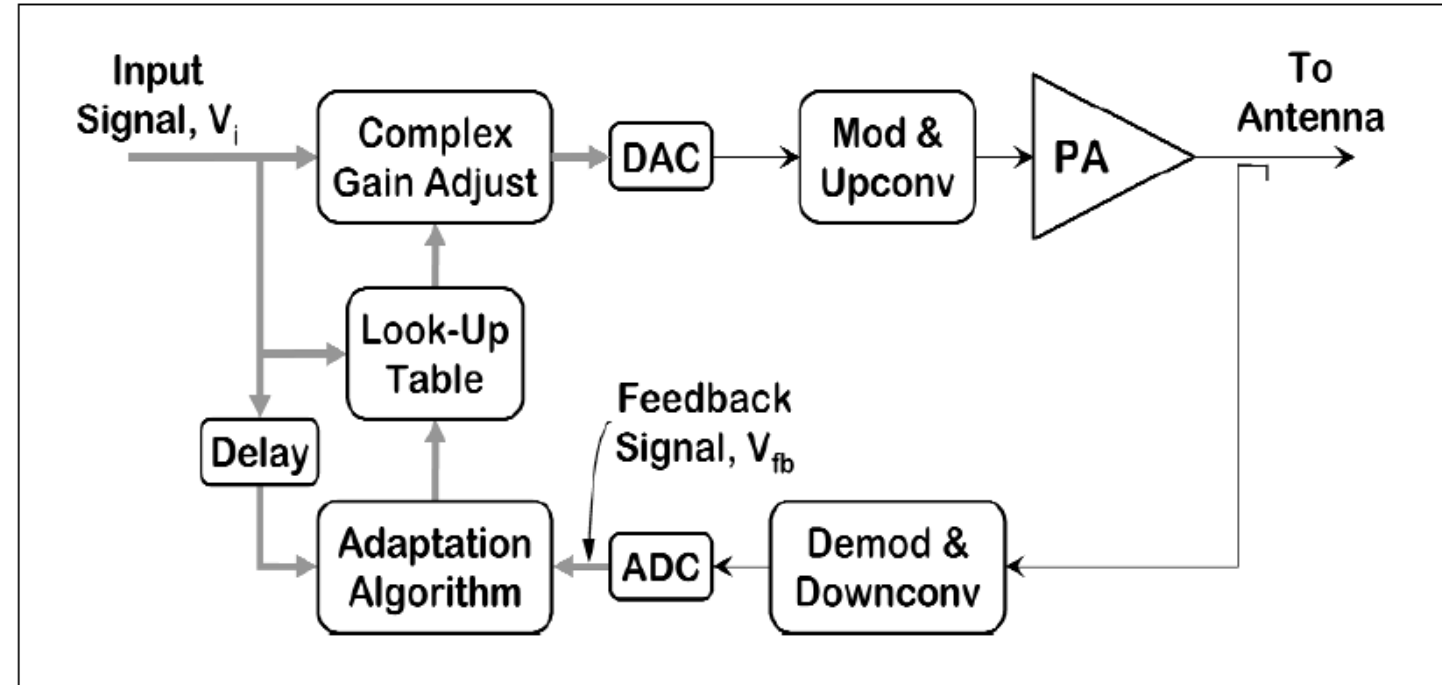
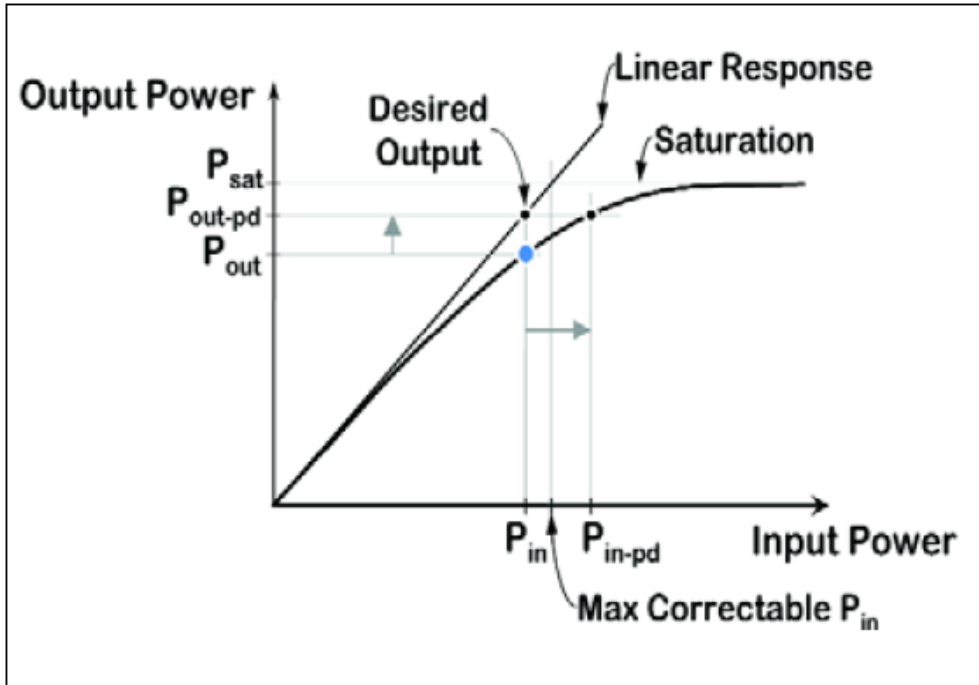
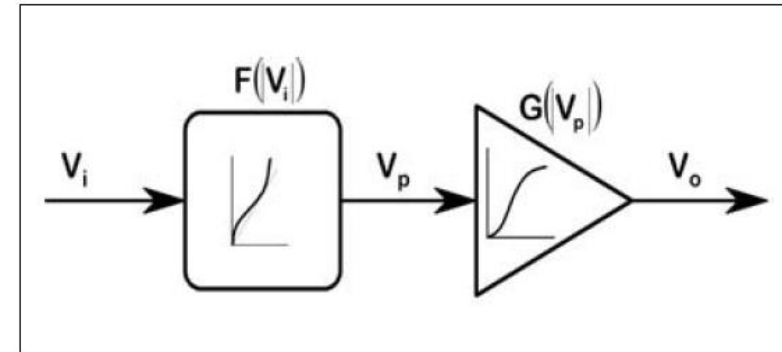


Non-linear region



Dynamic Range – Linearity – Digital Pre-Distortion (DPD)

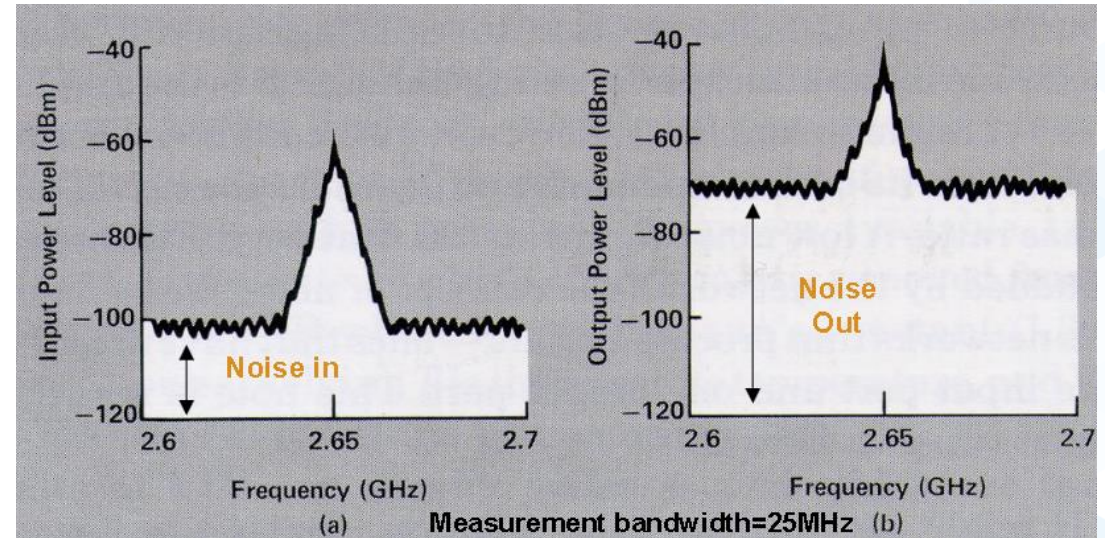
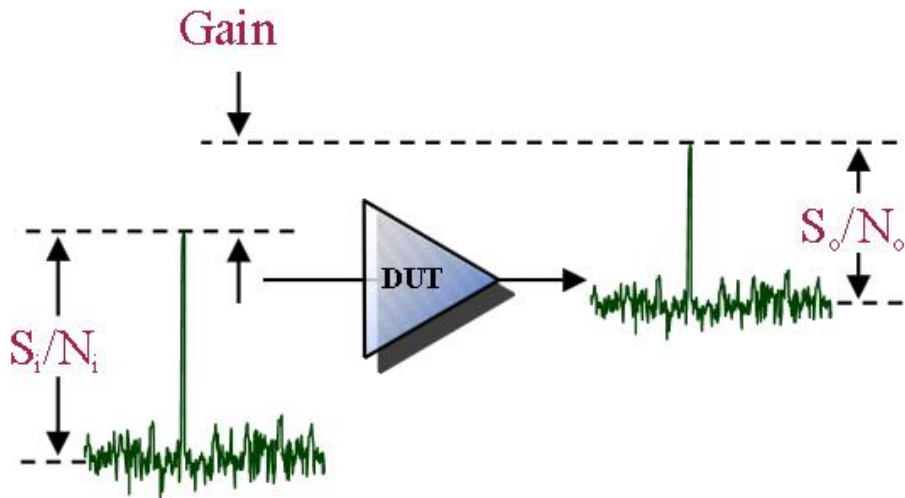
Phase and gain adjustments of the power amplifier's non-linear region are fed back and corrected in the baseband



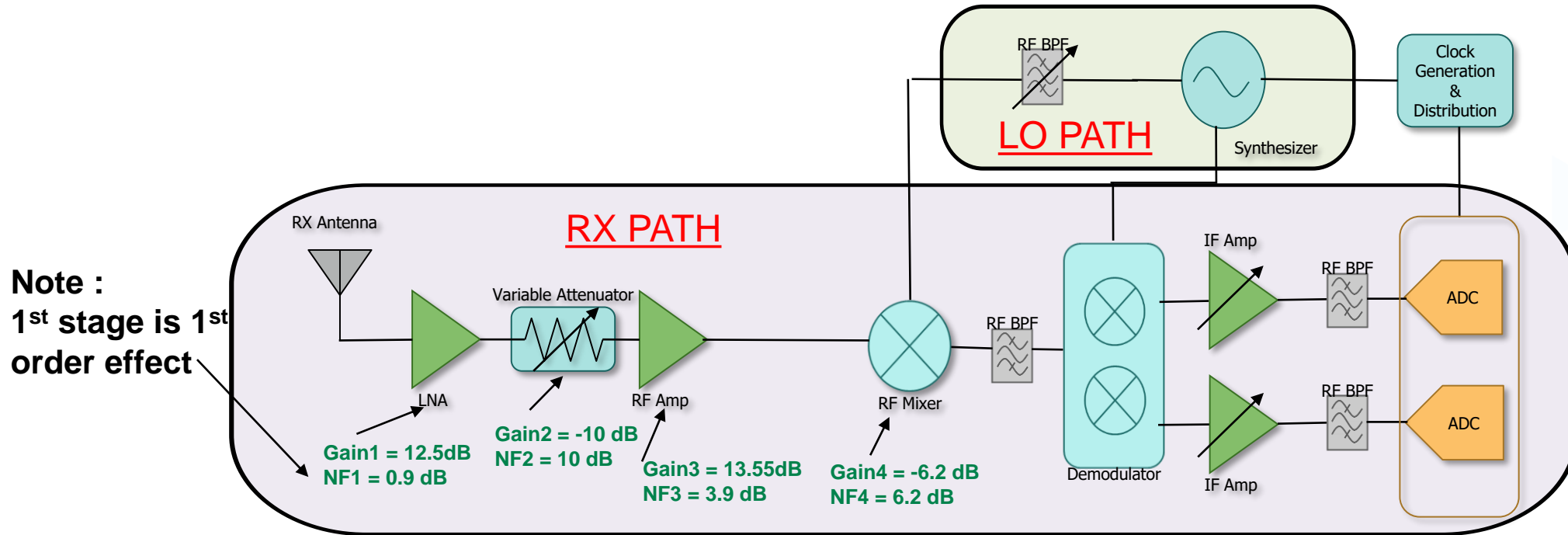
Dynamic Range – Noise

$$\text{Noise Factor} = F = \frac{\left(\frac{S}{N}\right)_{in}}{\left(\frac{S}{N}\right)_{out}}$$

$$\text{Noise Figure} = 10 \log(F)$$



Dynamic Range – Cascaded Noise



$$\text{Total Noise Factor (NF in milliwatts)} = NF1 + (NF2-1)/G1 + (NF3-1)/G1*G2 + (NF4-1)/G1*G2*G3...$$

$$\text{Noise Figure (dB)} = 10 \log (NF)$$

Dynamic Range – Phase Noise

- Phase noise – Generated from a VCO or synthesizer which is close in frequency to the source

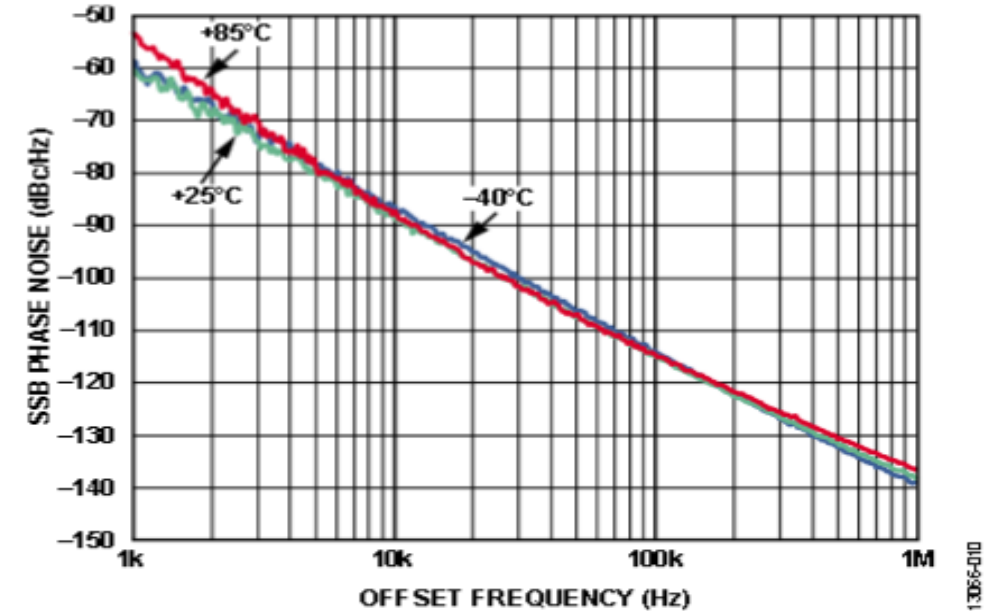
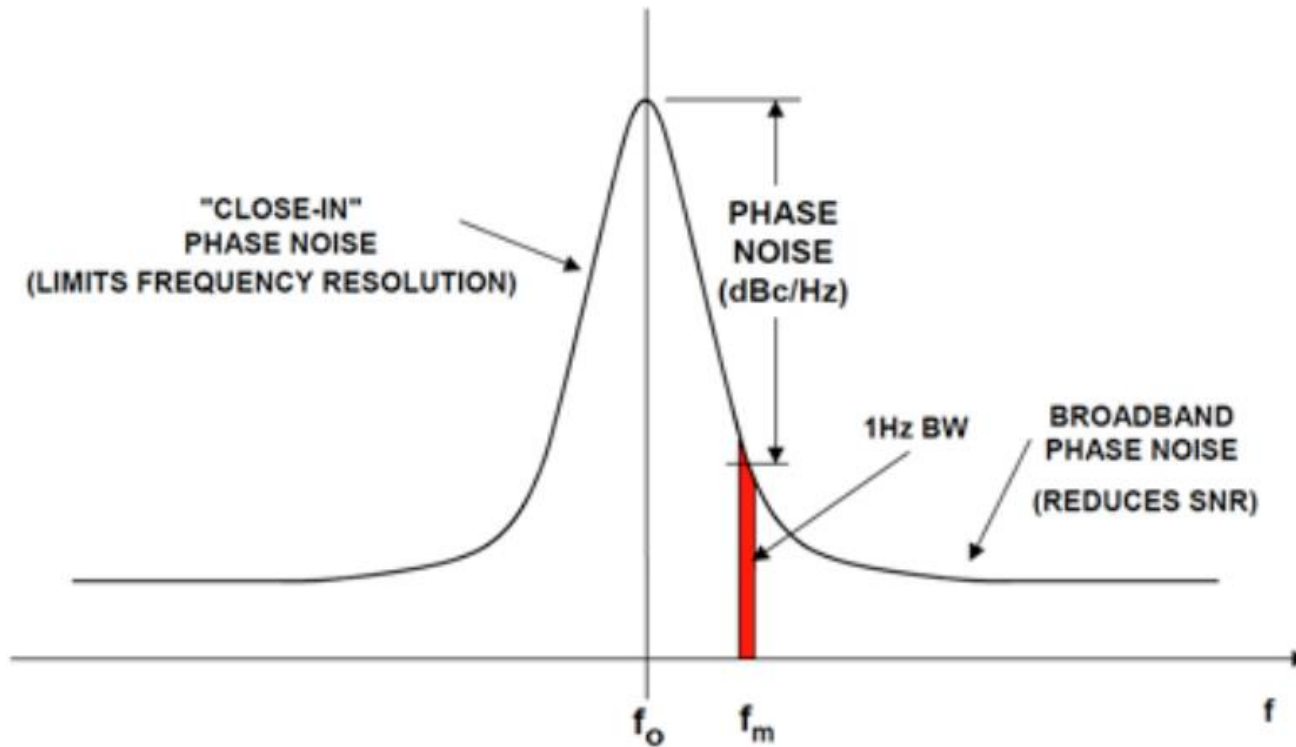
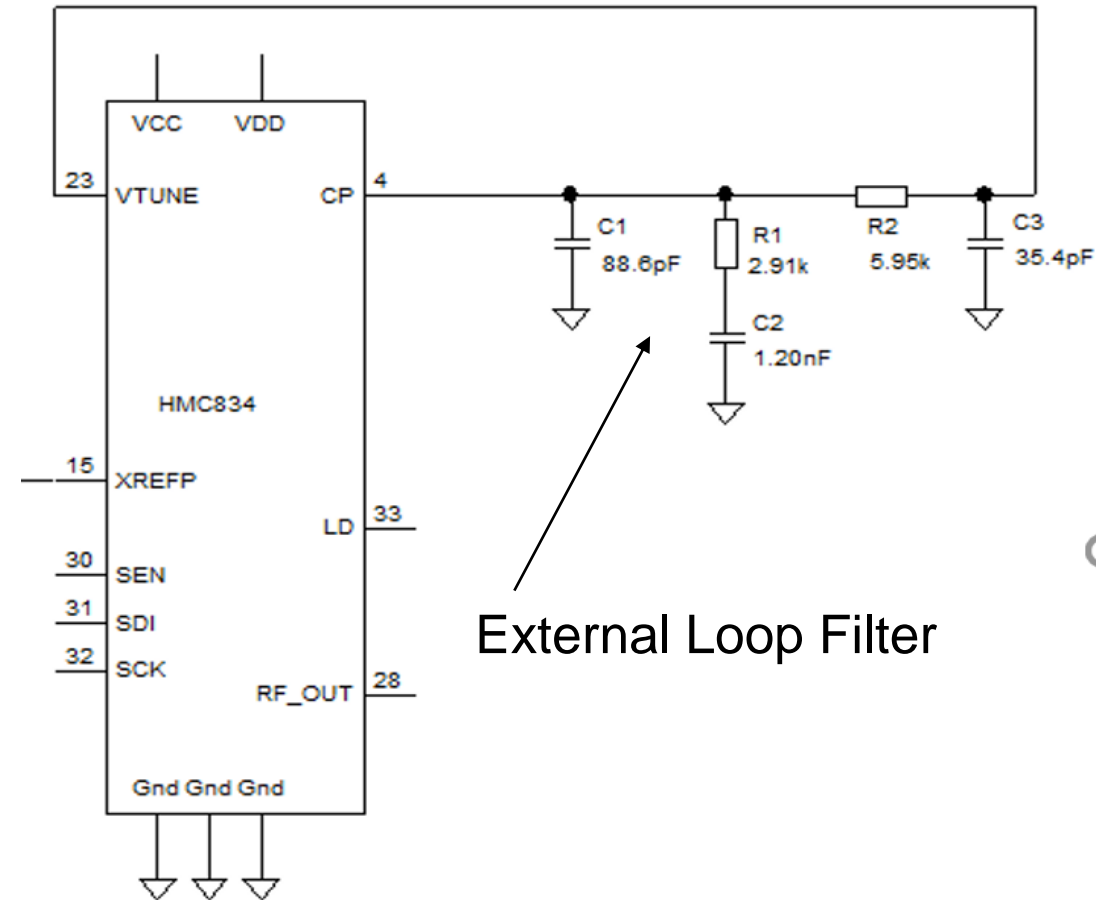
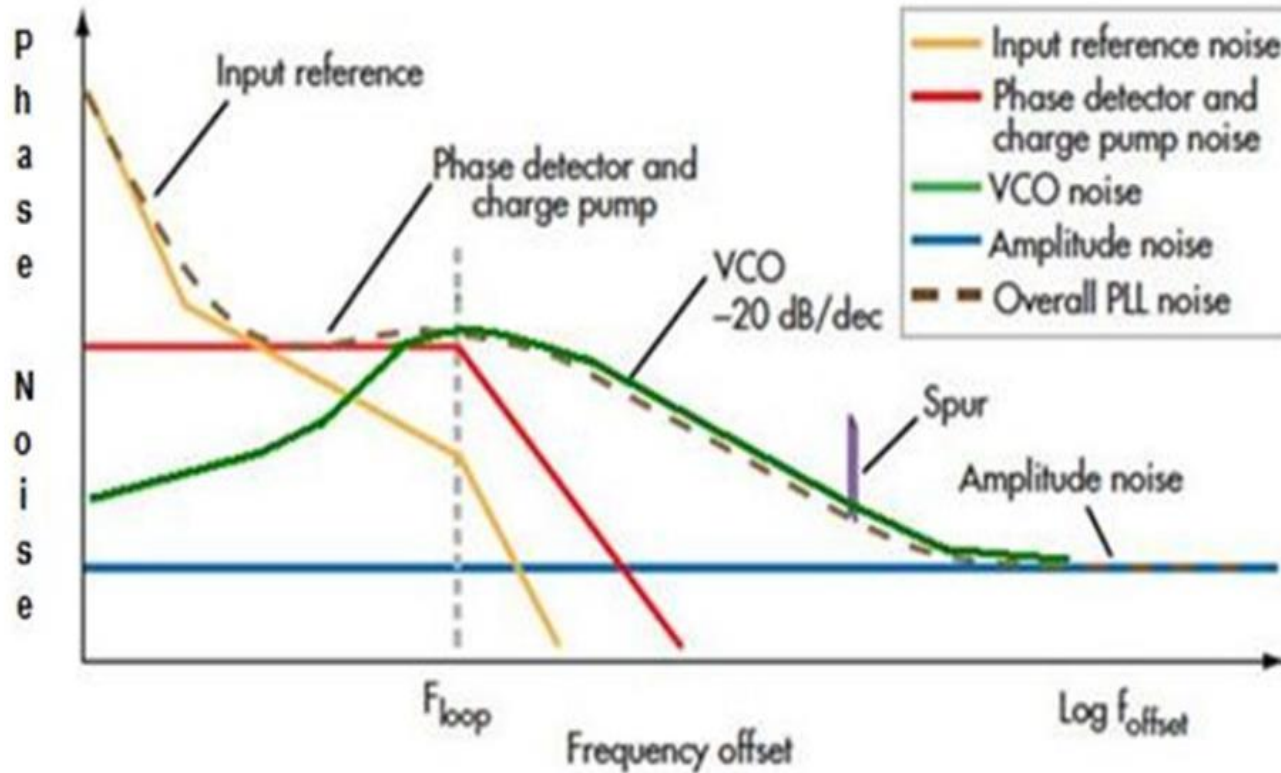


Figure 15. SSB Phase Noise vs. Offset Frequency at VTUNE = 5 V

Dynamic Range – Synthesizer Phase Noise

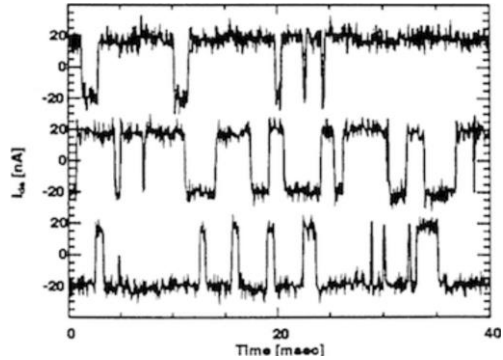
- Synthesizer phase noise is a compilation of several components of the synthesizer such as the input reference, phase detector, charge pump and phase lock loop.



Dynamic Range – Other Noise Types

- Thermal (Johnson-Nyquist) noise – Broadband frequency noise created by all components and varies with temperature

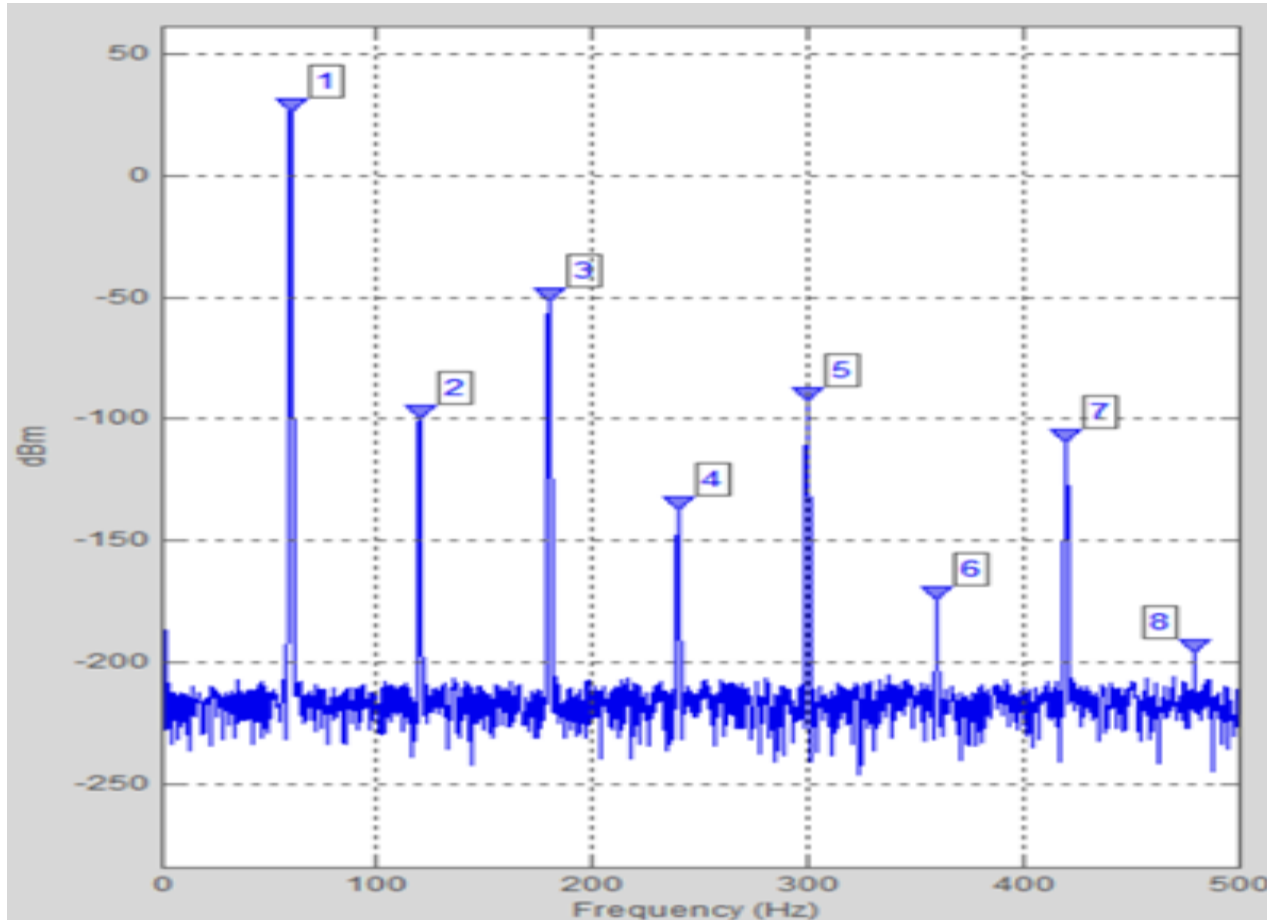
- Popcorn (Burst) noise - Caused by defects in semiconductors with trapping and releasing charges



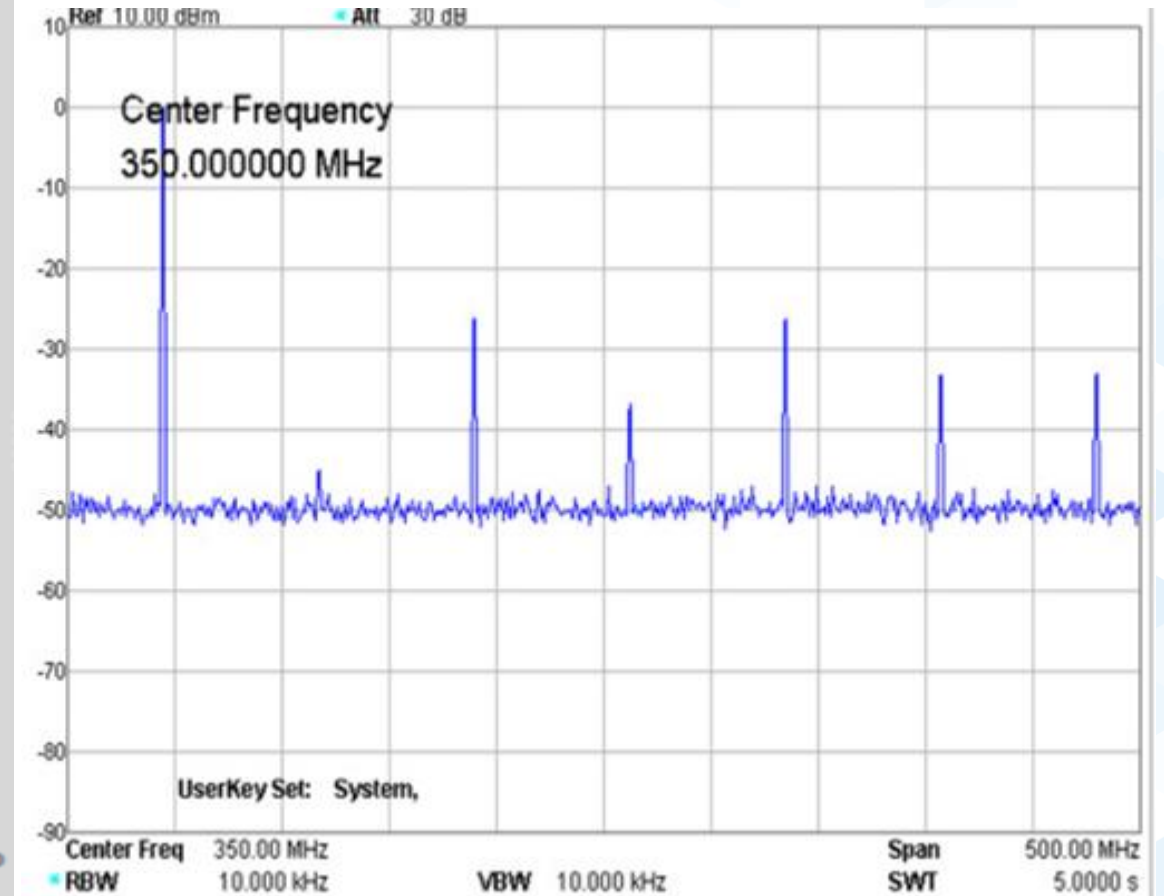
- Shot noise – Broadband frequency noise in all electronic devices and varies with current
- 1/f (Flicker) noise – Very low (Hz or sub Hz) noise and decreases as frequency increases
- Quantization Noise - Leftover energy created by the converters after conversion.

Dynamic Range – Spurious Signals

- Harmonic and non-harmonic spurious signals are found in every signal chain
- Non-harmonic spurious signals can come from within or outside the signal chain.



Harmonics

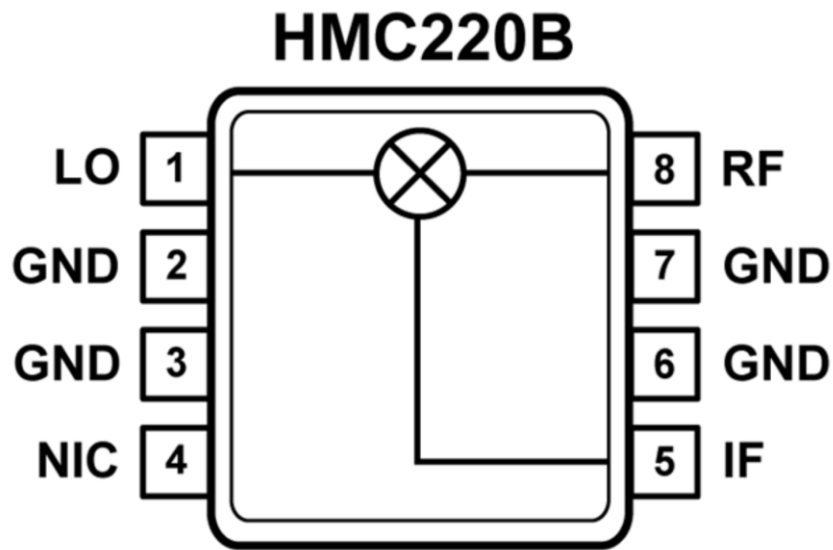


Spurious Signals

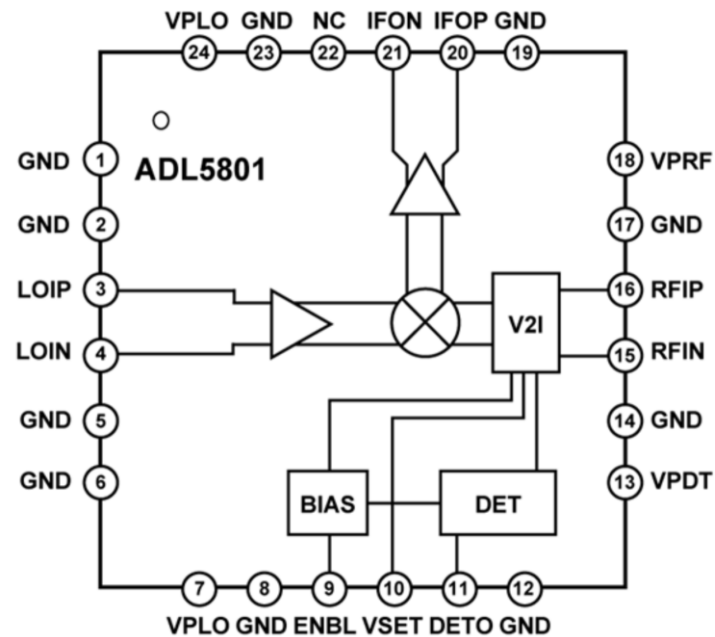
Dynamic Range – Mixers

- Mixers can come in various types, passive, active, IQ and others.

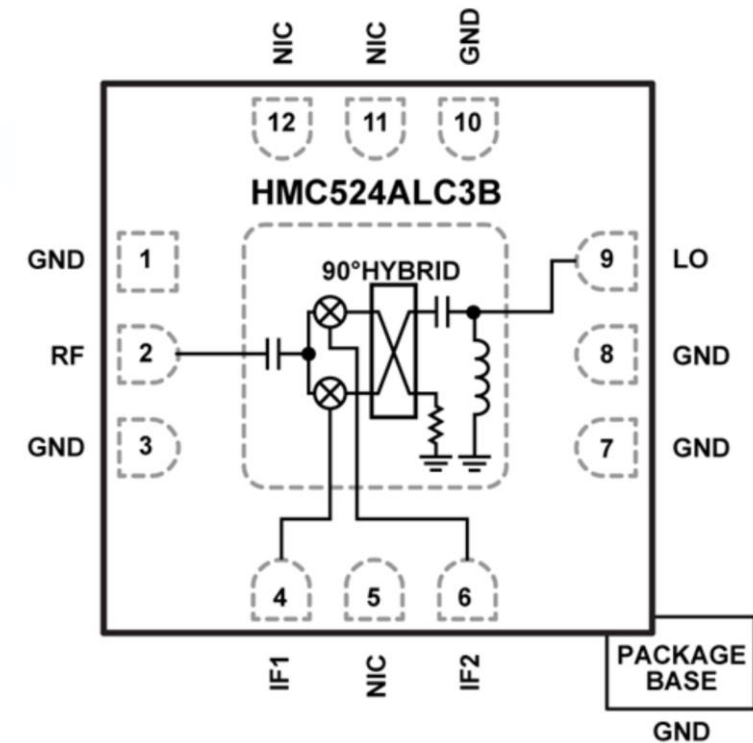
Passive



Active

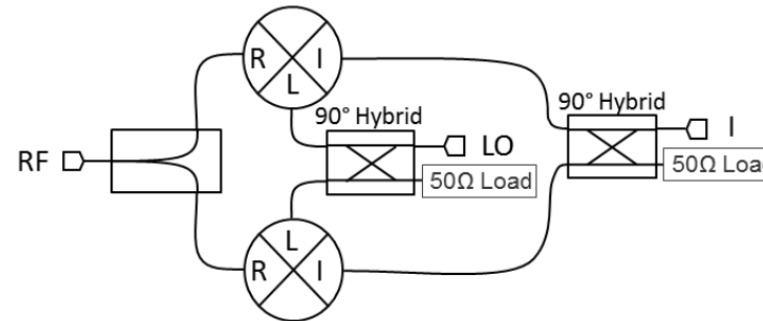


IQ



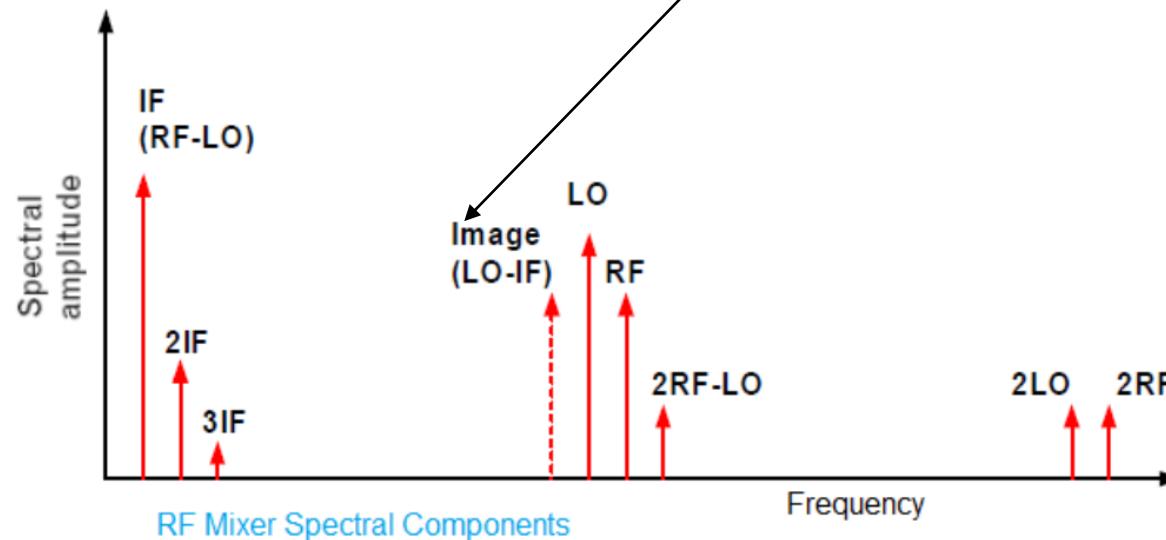
Dynamic Range – IQ Mixers – Image Rejection

- IQ Mixers, also known as image reject or single sideband mixers can help dynamic range by cancelling the image using phase cancellation



IR/SSB Mixer

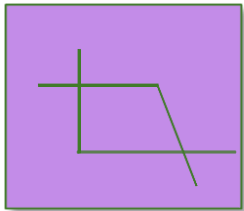
Image reduced or cancelled by phasing



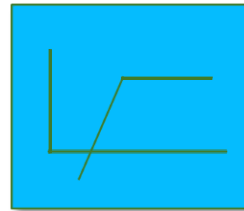
Dynamic Range – Spurious Signals - Filters

- 4 basic types of filters can be used. Some may be tunable
- Often filters cannot help with close-in signals such as IMD tones, images or in-band receiver spurious

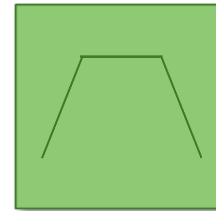
Low Pass Filter



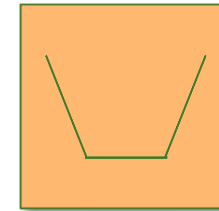
High Pass Filter



Band Pass Filter



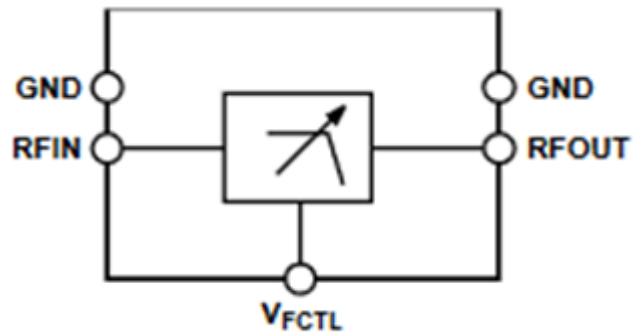
Band Stop Filter



Dynamic Range – Spurious Signals - Filters

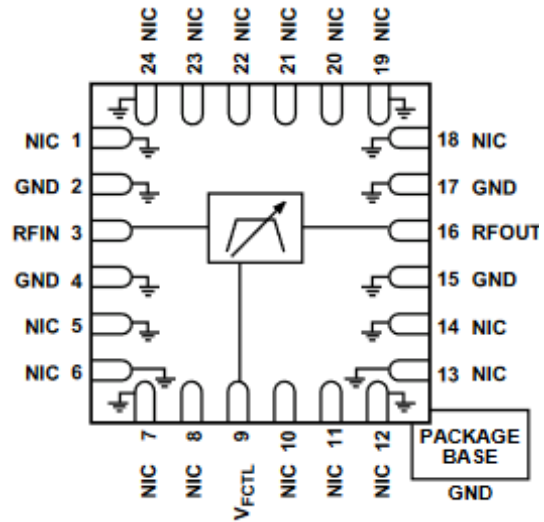
3.95 GHz to 6.9 GHz,
Tunable Low-Pass Filter

HMC882A



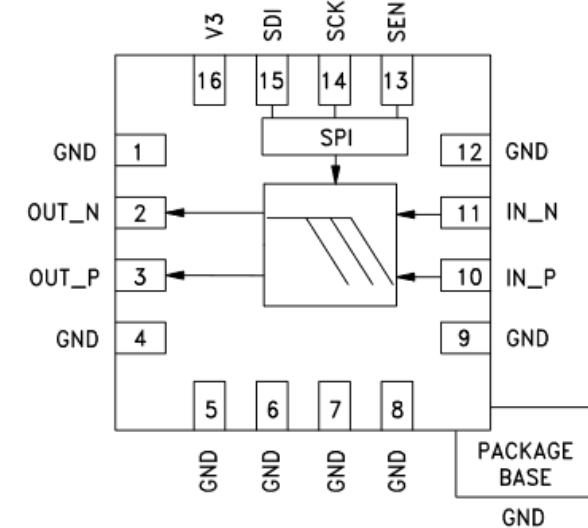
11 GHz to 20 GHz,
Tunable Band-Pass Filter

ADMV8420



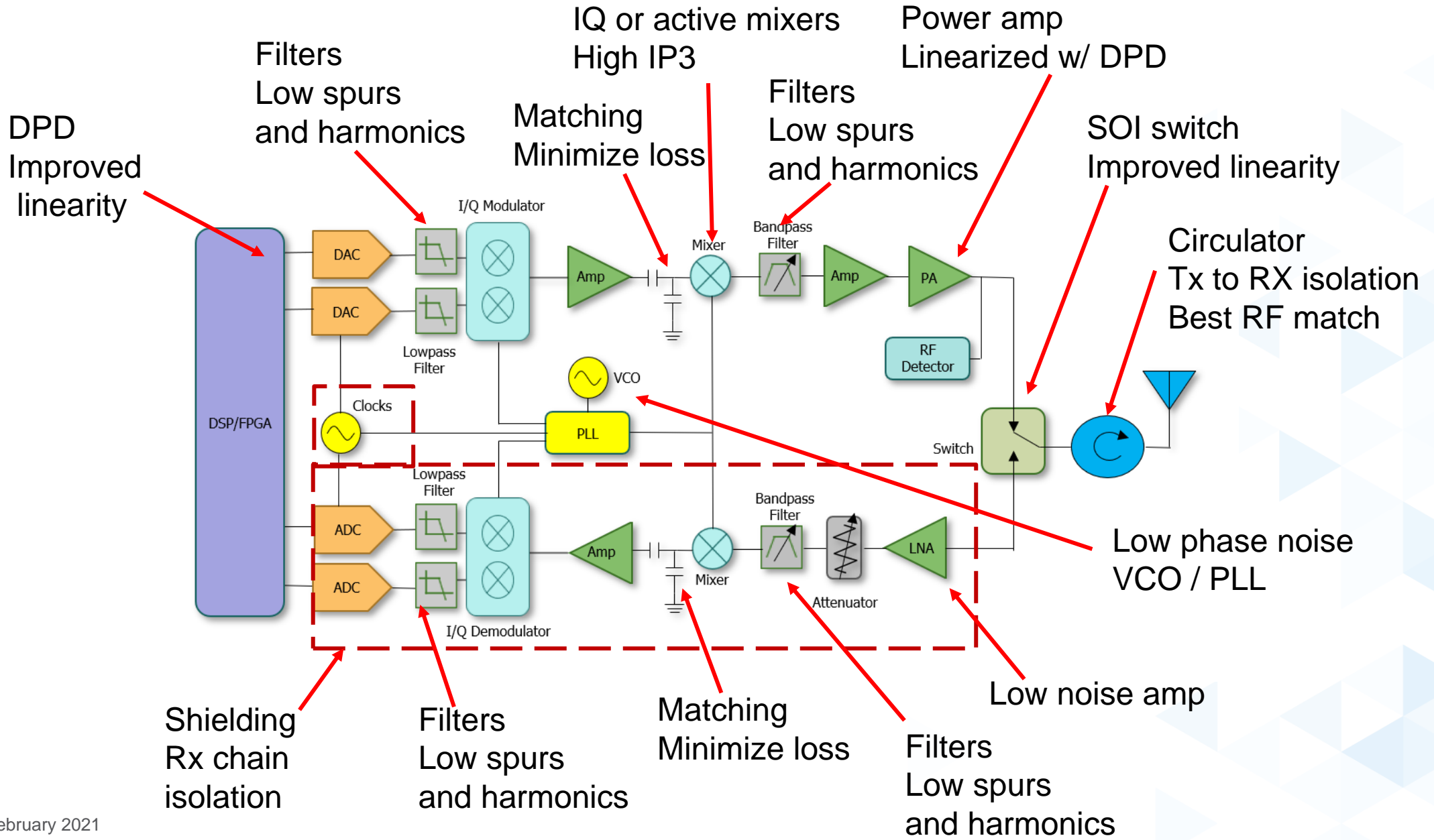
Programmable Harmonic
Low Pass Filter

HMC1044LP3E



Improving the RF Signal Chain

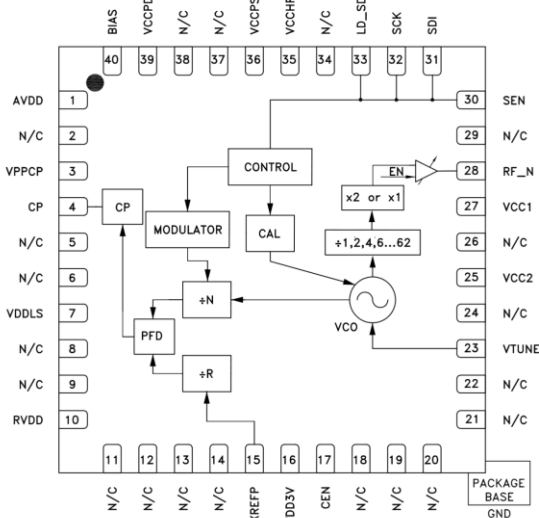
Optimizing the Signal Chain – In Review



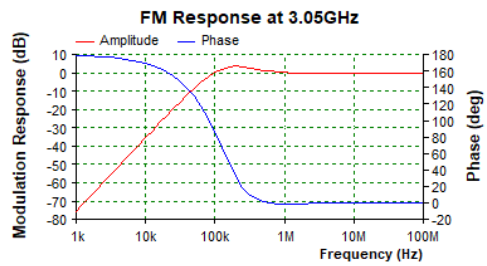
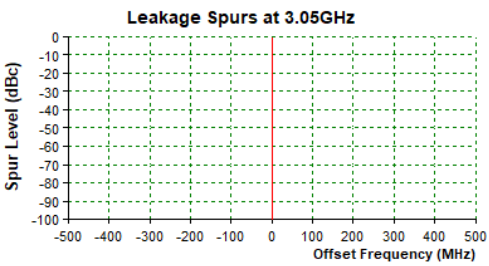
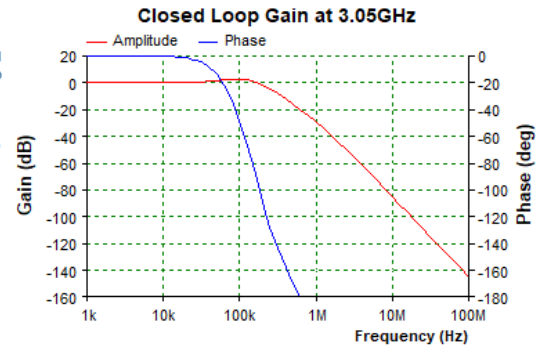
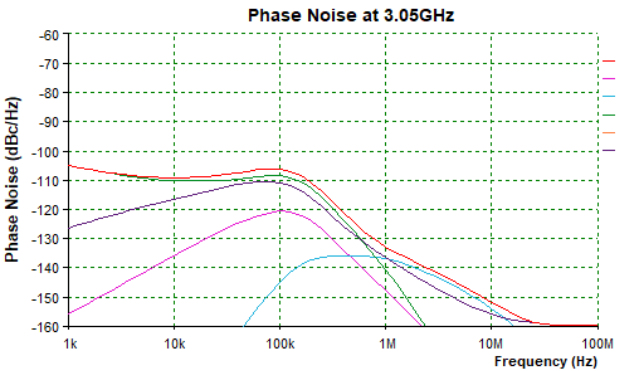
Tools

Tools - ADISimPLL

HMC834

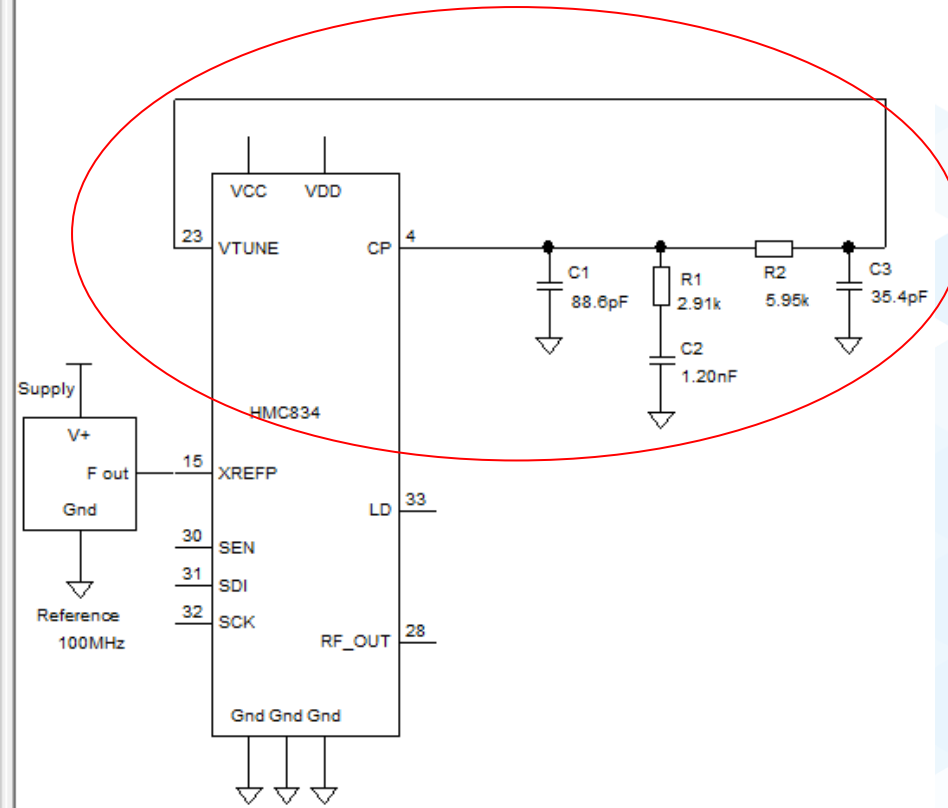


Synthesizer simulated RF performance



System	Min Freq	3.00GHz
	Max Freq	3.10GHz
	Channel Spc.	2.980 Hz
	PD Freq.	50.0MHz
	Modulus	2 ²⁴
	Design Freq	3.04959GHz
Reference	Frequency	custom
	Phase Noise	None
VCO	Frequency	HMC834
	Tuning Law	Multiband
	Input Cap.	5.00pF
	Divider N	1
	Phase Noise	Table
Chip	Mode	HMC834
	Mode	Normal
	Main Divider	
	Ref Divider	
	Phase Detector	Charge Pump
	Lock Detect	None
	Speedup Mode	None
Loop Filter	Specify:	CPP_3C
	Loop Bandwidth	127kHz
	Phase Margin	45.0 deg
	Zero Loc.	45.3kHz
	Pole Loc.	356kHz
	Last Pole	1.27MHz
	C1	88.6pF
	R1	2.91k
	C2	1.20nF
	R2	5.95k
	C3	35.4pF
Lock Detect	Lock Detect	None
FreqDomain	Min Freq	1.00kHz
	Max Freq	100MHz
	Pts per Decade	10

Loop filter design



Notes:
1. Consult datasheet for full pinout detail

Signal Chain Analysis



	Stage 1	Stage 2	Stage 3	Stage 4	Stage 5	Stage 6
	DAC	VGA	Mixer (Tx)	Driver Amp	GaN PA	SPDT T/R
	AD9162V2	ADRF6520VGA1	AD8342	ADL5320-3V	HMC8205BF10	HMC646LP2-Rx
Output Freq (MHz)	500	500	2000	2000	2000	2000
Zin (Ohms)	100	100	50	50	50	50
Zout (Ohms)	100	100	50	50	50	50
Power Gain (dB)	-12.57	-12	4.65799949645996	12.6	25.94	-1.3
Voltage Gain (dB)	-12.6	-12	4.7	12.6	25.9	-1.3
OIP3 (dBm)	17.6	36	20.7	31.4	47.7	32.7
OP1dB (dBm)	25	12.5	10.5	22.8	42.1	17.7
Pout (dBm)	-12.6	-24.6	-20.4	-7.8	18.1	16.8
Pout Backoff (dB)	37.6	37.1	30.9	30.6	24	0.9
Peak Backoff (dB)	37.6	37.1	30.9	30.6	24	0.9
Noise Figure (dB)	23.2	39	13.8	3.6	6	1.3
Voltage (V)	3.3	3.3	5	3.3	50	0
Current (mA)	697	140	98	44	1300	0

Transmit

Toggle Tx/Rx

Output Freq (MHz)

Zin (Ohms)

Zout (Ohms)

Power Gain (dB)

Voltage Gain (dB)

OIP3 (dBm)

OP1dB (dBm)

Pout (dBm)

Pout Backoff (dB)

Peak Backoff (dB)

Noise Figure (dB)

Voltage (V)

Current (mA)

Input

Number of Stages	6	
Input Power	0	dBm
Analysis Bandwidth	1	MHz
PEP-to-RMS Ratio	0	dB
P1dB Backoff Warning	10	dB
Peak Backoff Warning	1	dB

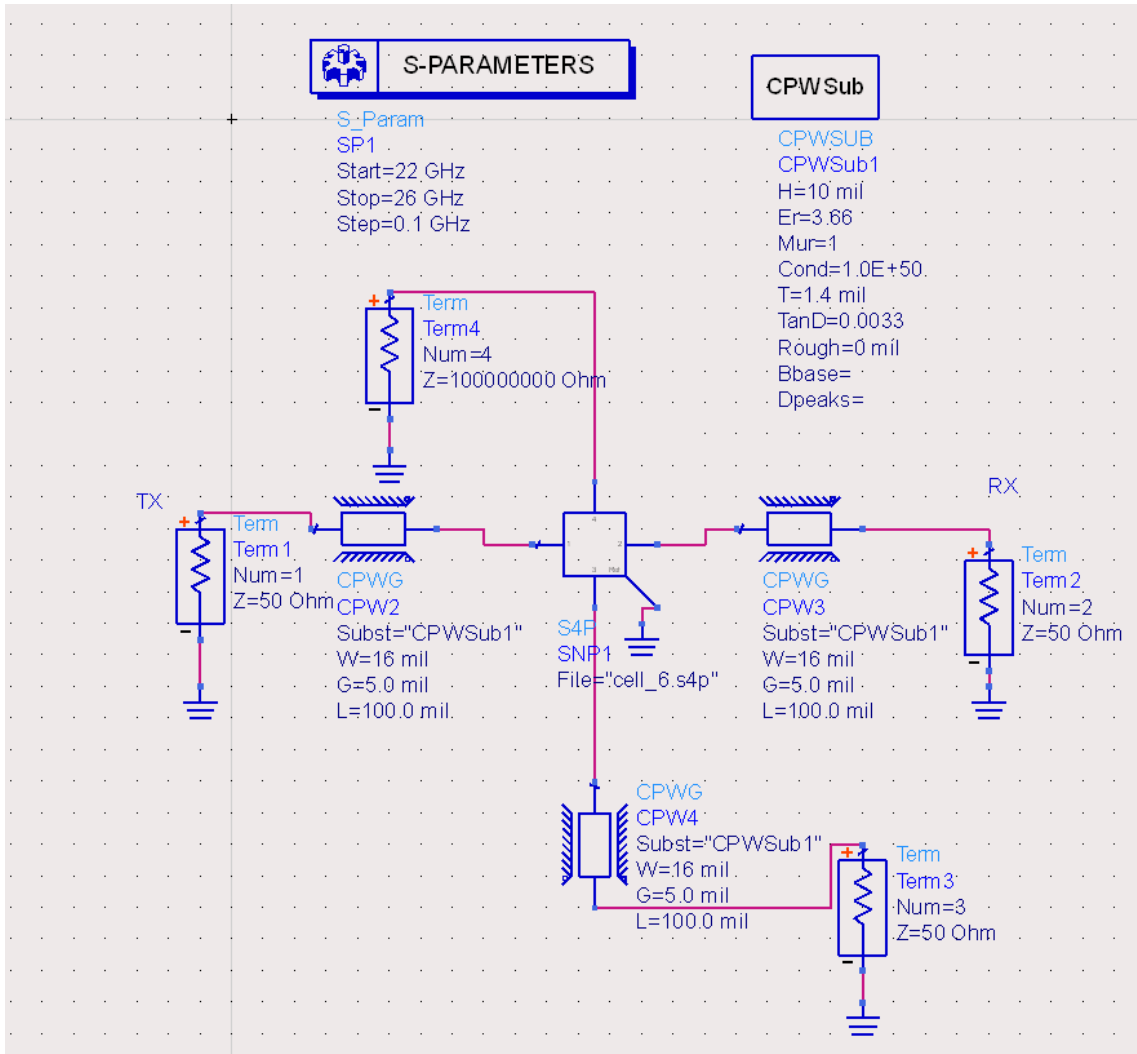
Analysis

Output Power (rms)	16.82	dBm
Output Voltage (rms)	1.55	Vrms
Output Voltage (pp)	4.38	Vpp
OP1dB	17.67	dBm
IP1dB	1.9	dBm
Power Gain	16.82	dB
Voltage Gain	13.81	dB

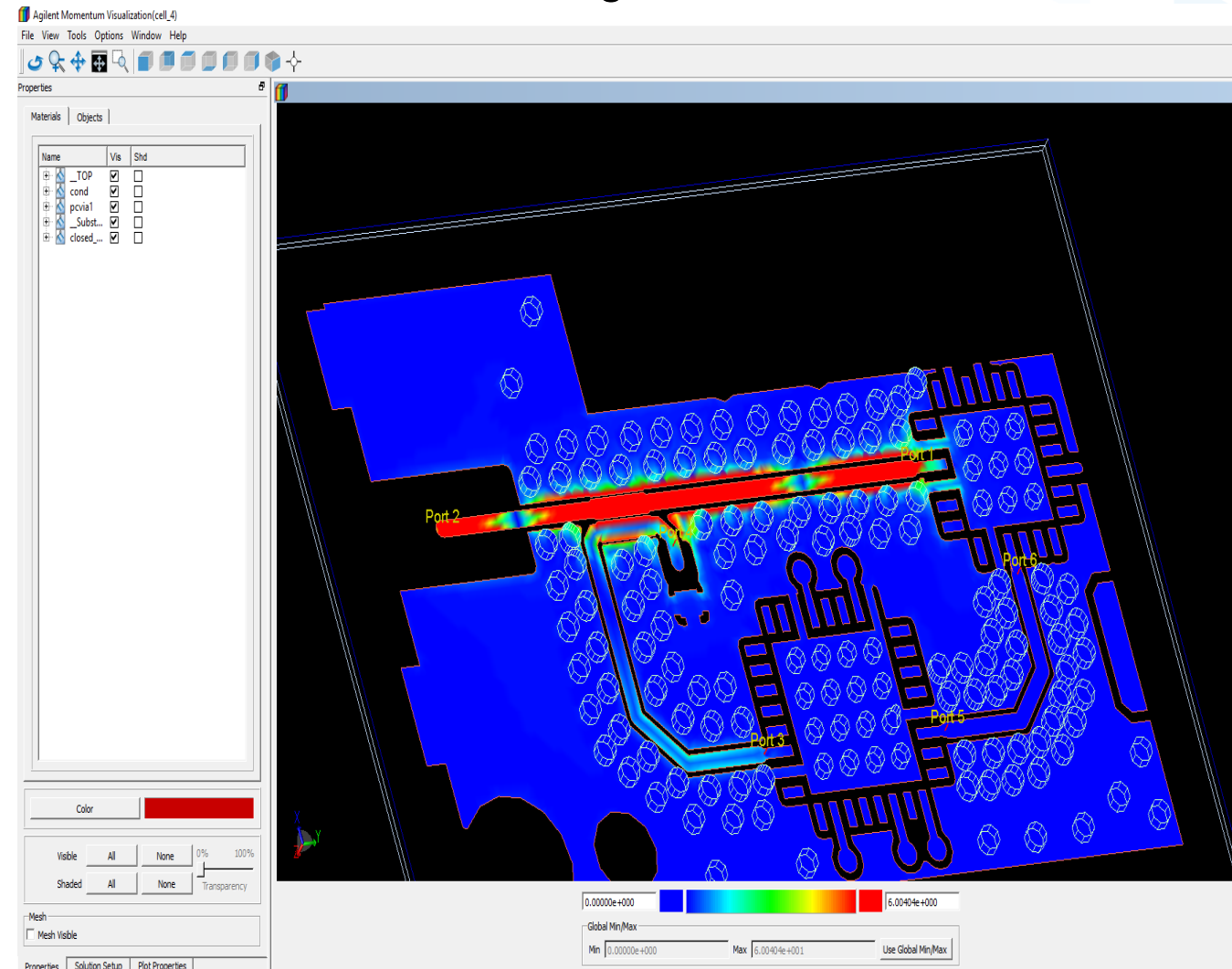
Noise Figure	51.77	dB
Output NSD	-105.4	dBm/Hz
Output NSD	1.2	uV/rtHz
Output Noise Floor	-45.4	dBm
SNR	62.2	dB

OIP3	32.34	dBm
IIP3	15.5	dBm
IMD3 ((Pout-3dB) per tone)	-37	dBc
SFDR	51.7	dB
ACLR (est.)	-51	dB
Pwr Consumption	68.4	W

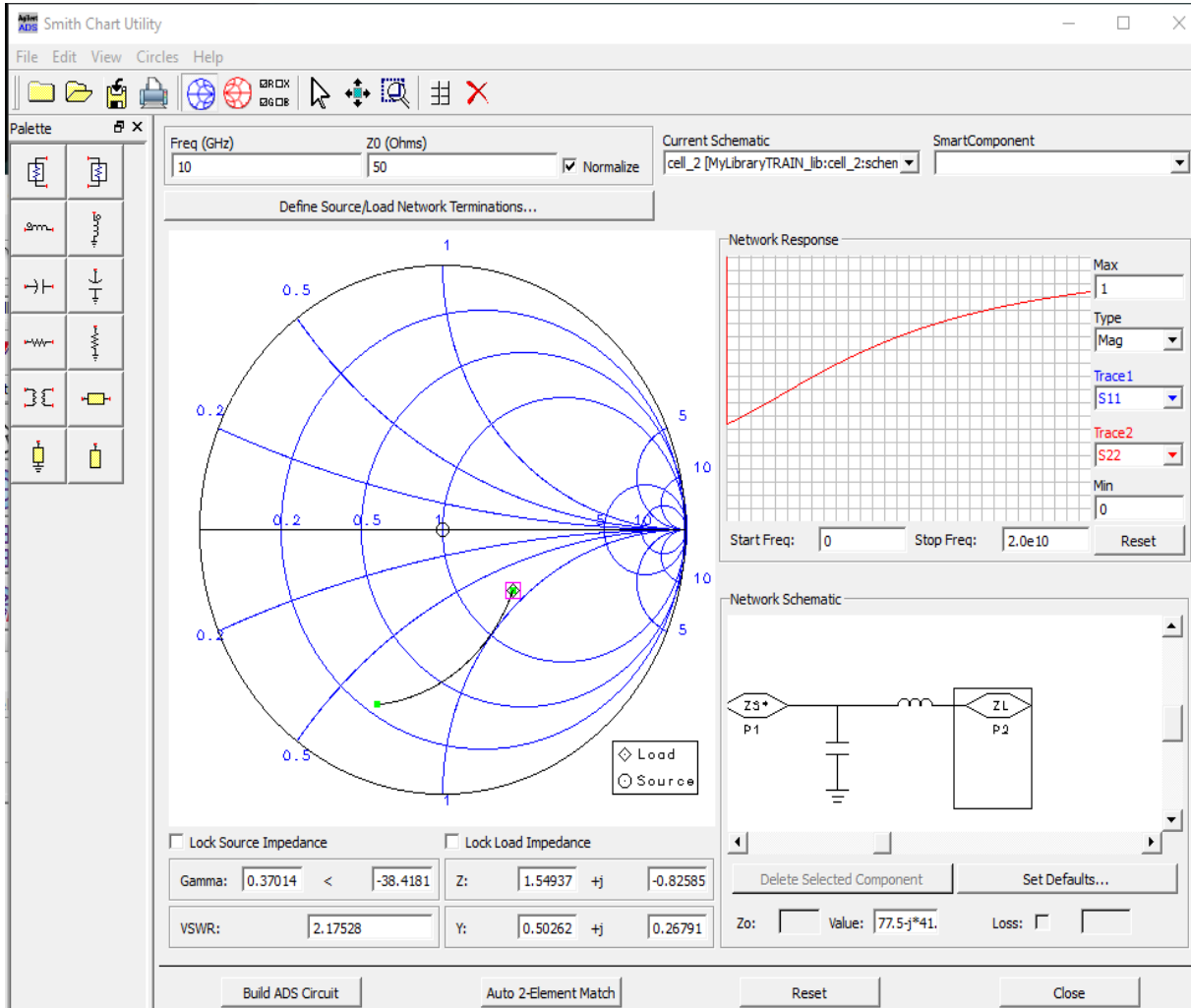
Linear Analysis



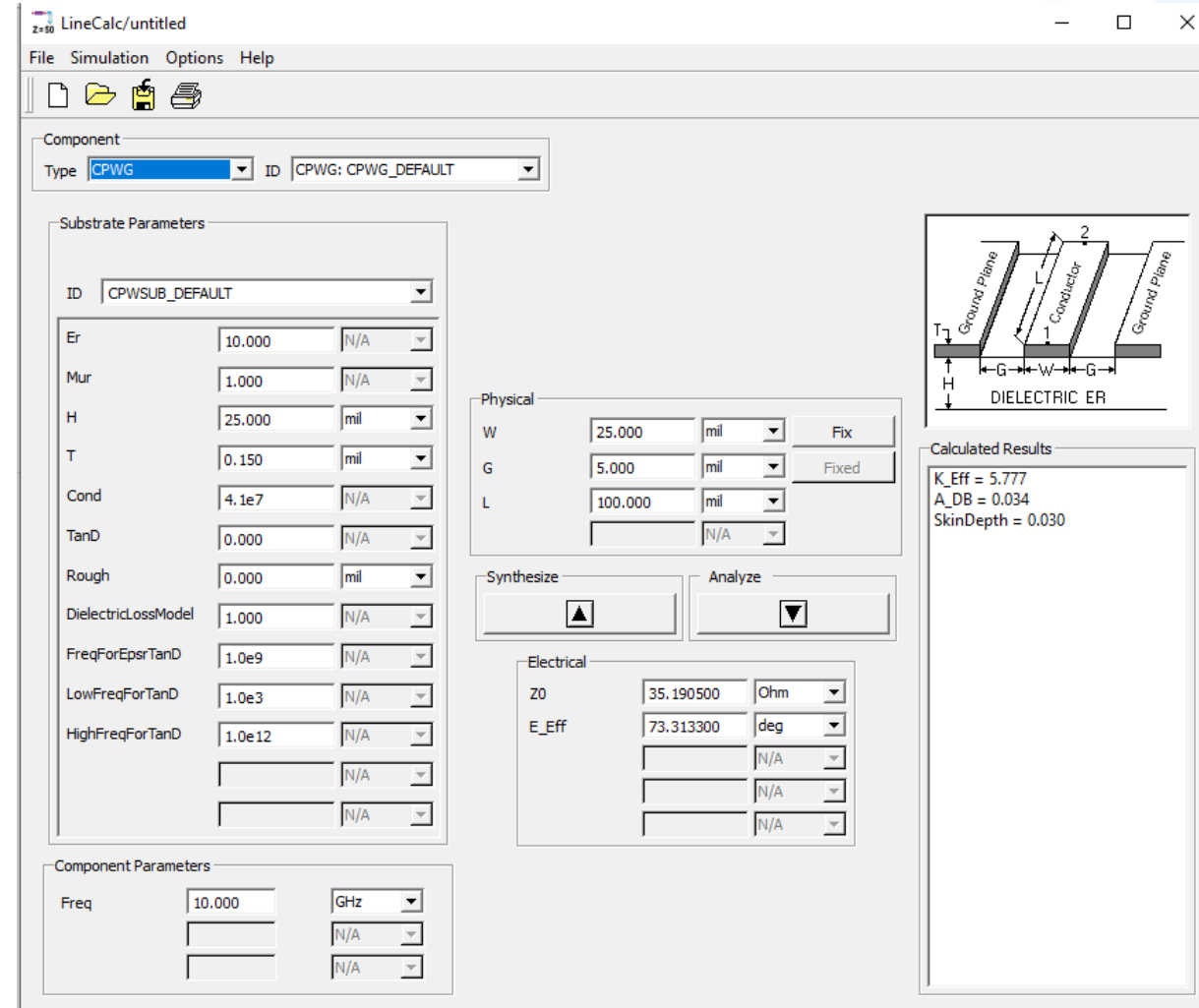
Electromagnetic Simulation



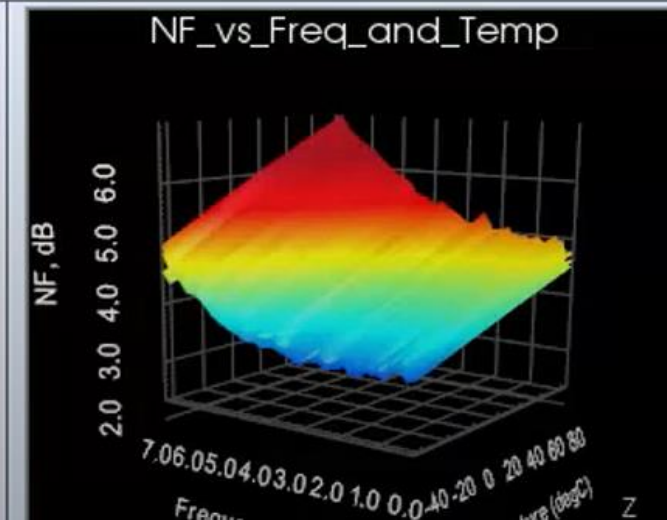
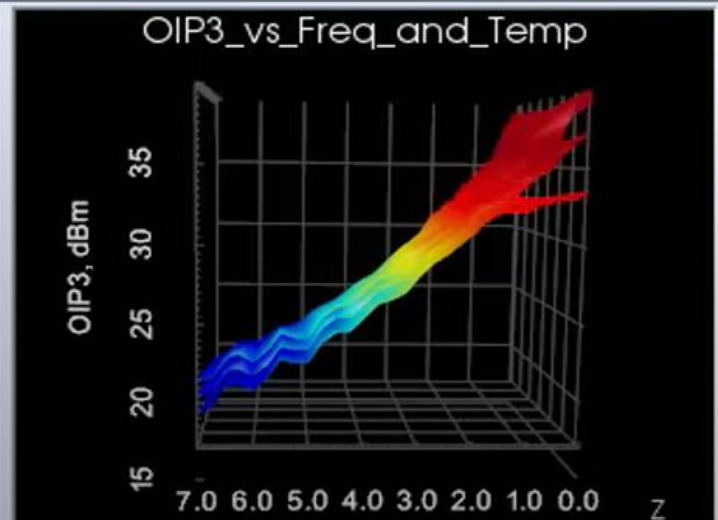
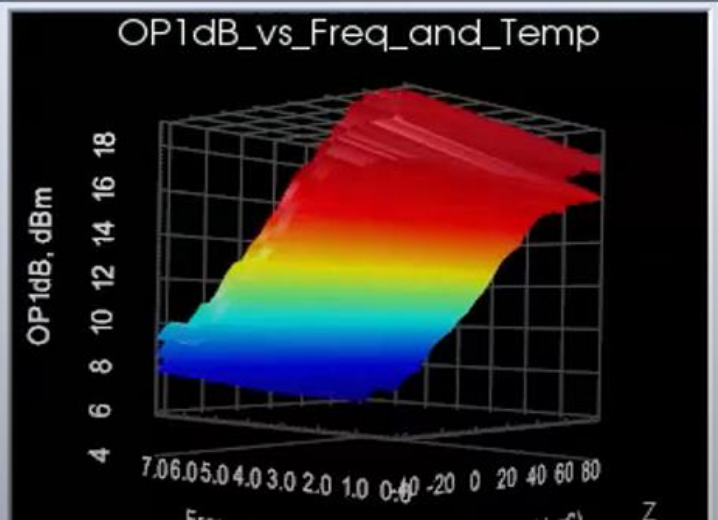
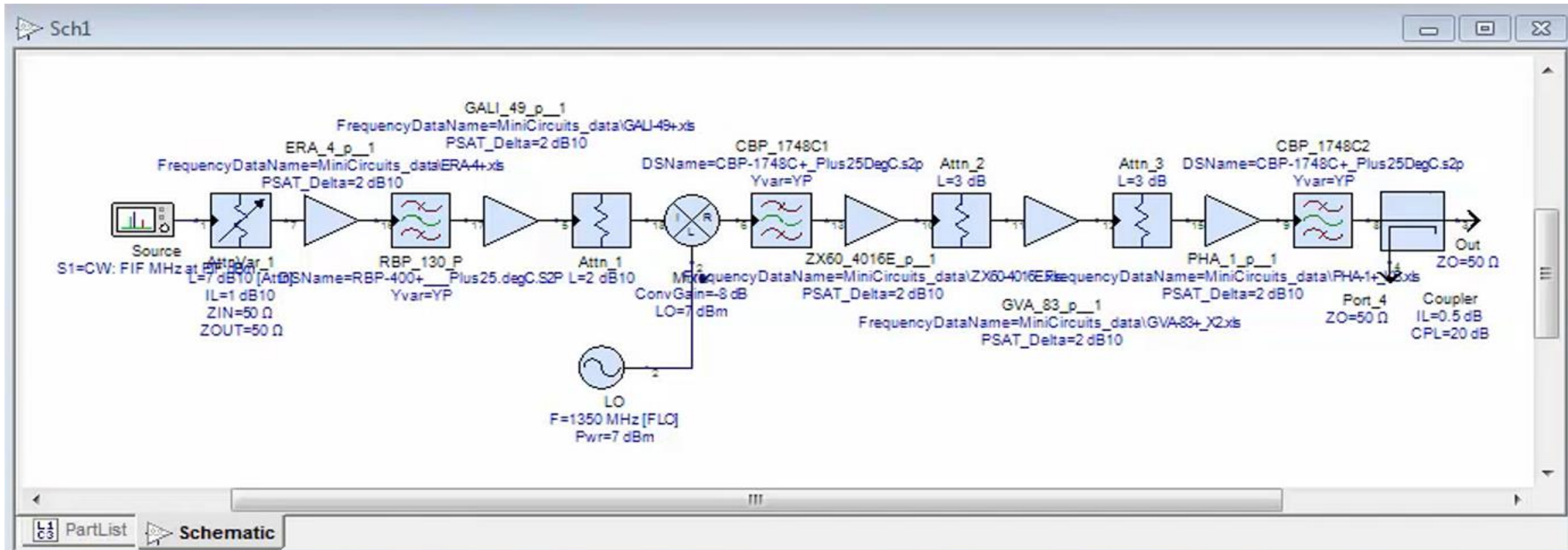
Smith Chart Utility



Line Calc

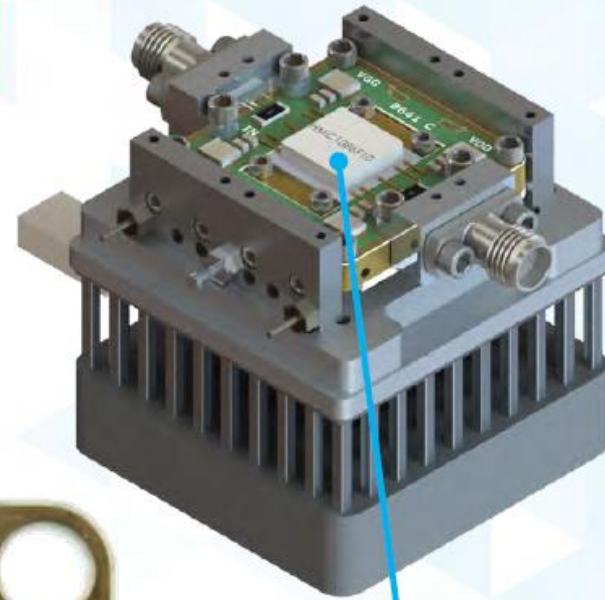
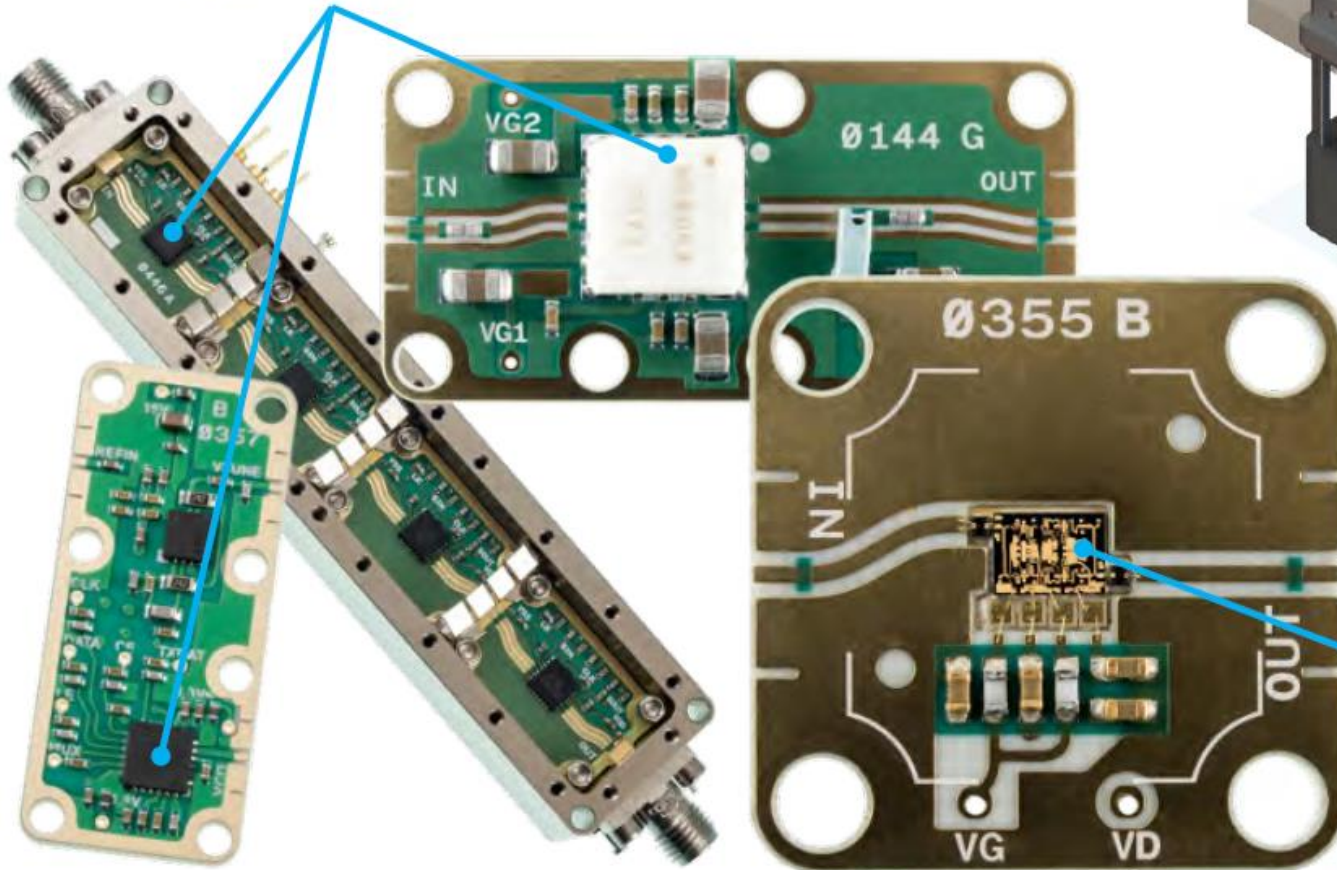


Tools – Keysight Genesys



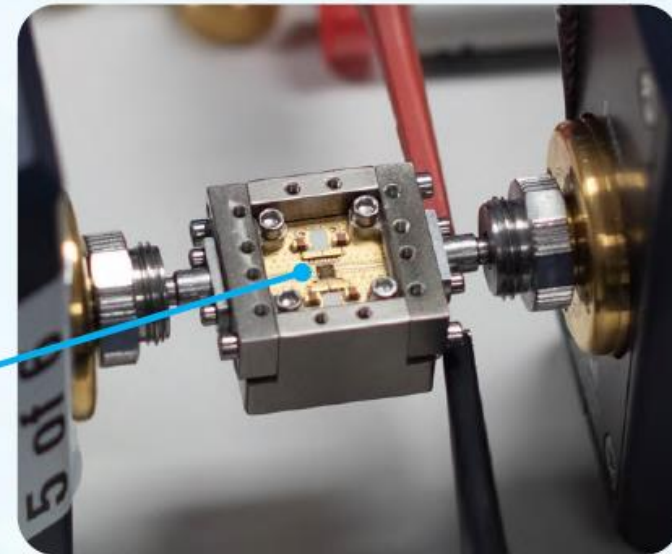
Drop-In RF Blocks (X-MWblocks)

SMT
RF Blocks



Flanged
RF Blocks

DIE
RF Blocks



Questions ?

Thank You !!

ADI Central Applications – 1-800-262-5643

Email – cic.americas@analog.com

References

References

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Jong Heon Kim, Kwangwoon University

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3. SOI process information – WaferPro - <https://waferpro.com/what-are-soi-wafers-or-silicon-on-insulator-wafers/>

4. **“The Effect of Via Spacing on the Signal Integrity Performance of PCB with Slotted Ground”**

By Soonyong Lee, Wonbum Seo, and Jaehoon Choi at Hanyang University

5. **“Applying shielding and ferrite materials”**

By Alex Snijder of Würth Electronics

References (cont.)

Arrow Related Webinars –

Title: Designing Power Solutions for RF Signal Chain Applications

<https://event.on24.com/eventRegistration/EventLobbyServlet?target=reg20.jsp&partnerref=ARROW&eventid=2390134&sessionid=1&key=DC41DD047B402583E3458DCDD1E63AEB®Tag=&sourcepage=register>

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