High-Speed Transceiver Toolkit

Stratix V FPGA Design Seminars 2011

Stratix V FPGA Design Seminars 2011

- Our seminars feature hour-long modules on different Stratix V capabilities and applications to help you understand how you can take advantage of these 28-nm FPGAs in your next-generation designs.

Stratix V FPGA Design Seminar Topics	
1	Designing with Partial Reconfiguration in Stratix V FPGAs
2	10Gbps Backplane Design and Optimization Using Stratix V FPGAs
3	Designing 28Gbps With Confidence
4	Minimizing Circuit Board Design Costs for Stratix V FPGAs
5	High-Speed Transceiver Toolkit
6	Using fPLLs in Stratix V FPGAs for Fractional-N Synthesis
7	Oscillator Replacement for Optical Transport Network (OTN) Applications
8	Using Variable Precision DSP Block in Stratix V FPGAs
9	Implementing Floating-Point DSP Using Stratix V FPGAs
10	Optimizing Power and Performance in Stratix V FPGA Designs
11	Designing High-Performance External Memory Interfaces with Stratix V FPGAs
12	Using Configuration via PCIe in Stratix V FPGAs

Agenda

- Introduction
- Transceiver debug use scenarios
- Getting started
- Demo
- Summary

Stratix V FPGAs – Built for Bandwidth

- Highest bandwidth
  - 66 transceivers capable of 14.1 Gbps and 7 x72 800-MHz DDR3 interfaces
  - Devices with 28-Gbps transceivers
- Unprecedented level of integration
  - Embedded HardCopy Blocks supporting PCI Express Gen3 and 40G/100G Ethernet
  - High-performance, high-precision DSP
  - Enhanced logic fabric with 1,000K LEs, 55 Mb RAM, and 4,096 18x18 multipliers
- Ultimate flexibility
  - Fine-grain and easy-to-use partial reconfiguration
  - Configuration via PCI Express
- 50% higher system performance and 30% lower total power

Introduction

Leading Edge Transceiver Features

Feature	Stratix IV FPGA	Stratix V FPGA
Process Technology	40nm	28nm
Maximum Transceiver Count	48	66
Data rate – Chip to chip	.600 - 11.3 Gbps	.600 – 14.1 Gbps 20-28 Gbps
Data rate – Backplane	Up to 8.5 Gbps	Up to 14.1 Gbps
Ring / LC Oscillator	Yes / Yes	Yes / Yes
Pre-emphasis	4 tap	4 tap
Continuous Time Linear Equalizer - CTLE	4 stage (up to 8.5 Gbps)	4 stage (up to 14.1 Gbps) 3 stage (up to 28 Gbps)
Adaptive Dispersion Compensation Engine - ADCE	Yes	Yes
Decision Feedback Equalizer - DFE	3 tap (up to 8.5Gbps)	5 tap (up to 14.1 Gbps)
EyeQ	Horizontal	Horizontal and vertical with bit comparator
Hard IP	x8 PCIe Gen2	x8 PCIe Gen3 100G PCS Interlaken

Signal Integrity Tool Offerings

I/O Simulation Models (HSPICE, IBIS-AMI, and others)

Pre-Emphasis Equalization Link Estimator (PELE)

High-Speed Toolkit (HST) Estimator and Simulator

Signal Integrity (SI) Kit

Website/Documents

Power Distribution Network (PDN) Tool

Early SSN* Estimator

Quartus II SSN Analyzer

EyeQ

Transceiver Toolkit

*** Simultaneous switching noise**

Transceiver Debug Use Scenarios

High-Level Challenges – Debug Phases

Phase 1:

Check if data is passing through transceiver channel during PCB bring-up

- Test BER by generating and verifying industry-standard PRBS data patterns
- Dynamically reconfigure the pre-emphasis and equalization settings
- Analyze the link by using Stratix V EyeQ feature to find optimal settings

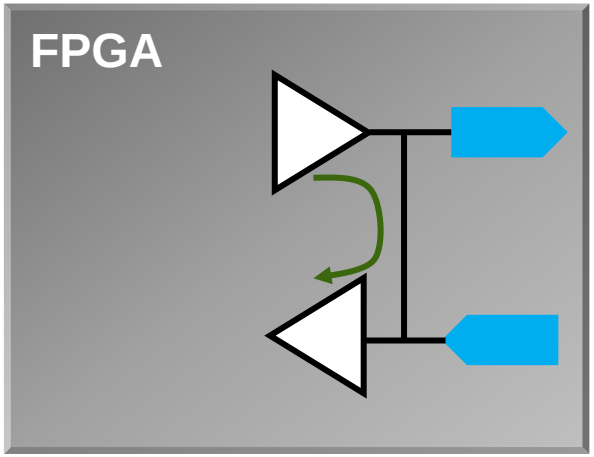
Phase 2:

Perform in-system or mission-mode link analysis with real-time data in an operating hardware system

- Integrate completed user design for full system testing
- Verify BER by using Stratix V bit comparator

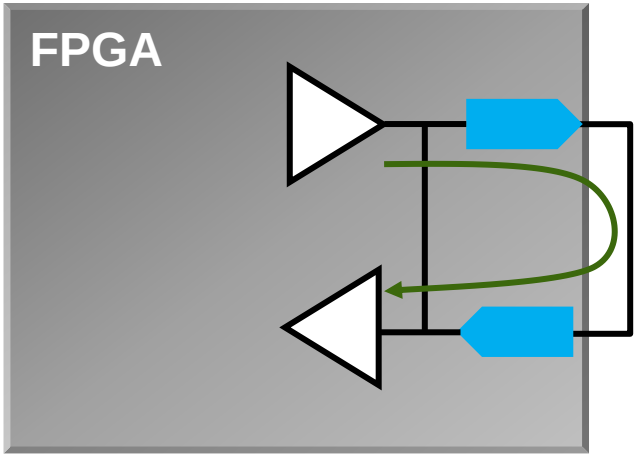
Debug Phase 1 – Q & A (1/3)

- Can I see data in the transceiver channels?
  - Perform internal serial loopback
  - TX and RX loopback directly within the silicon



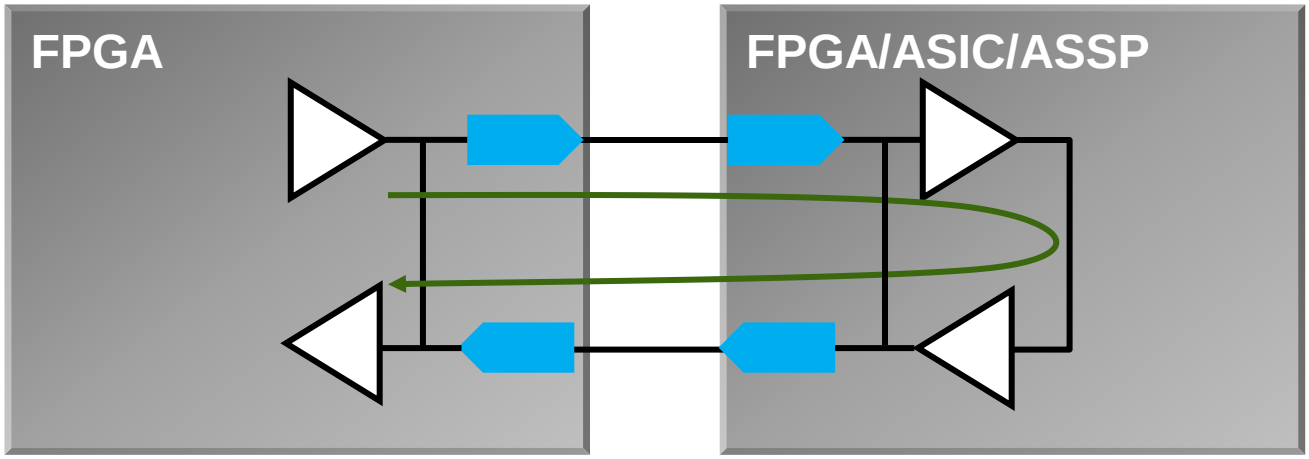
Debug Phase 1 – Q & A (2/3)

- Can I see data drive out of the FPGA TX pin and the same data drive back into the RX pin, and vice versa?
  - Perform external loopback
  - TX and RX drive in and out of the FPGA pins



Debug Phase 1 – Q & A (3/3)

- Can I see data drive out of the FPGA TX pin and the same data received in another device or external test equipment, and vice versa?
  - Perform reverse serial loopback
  - TX from device 1 drives RX in device 2 and vice versa
  - External test equipment drives RX in device 1 and vice versa



Debug Phase 2 – Q & A

- Can I see data running in the completed hardware system?
  - Run final test by using the fully integrated user design

Transceiver Toolkit Overview

What is the Transceiver Toolkit?

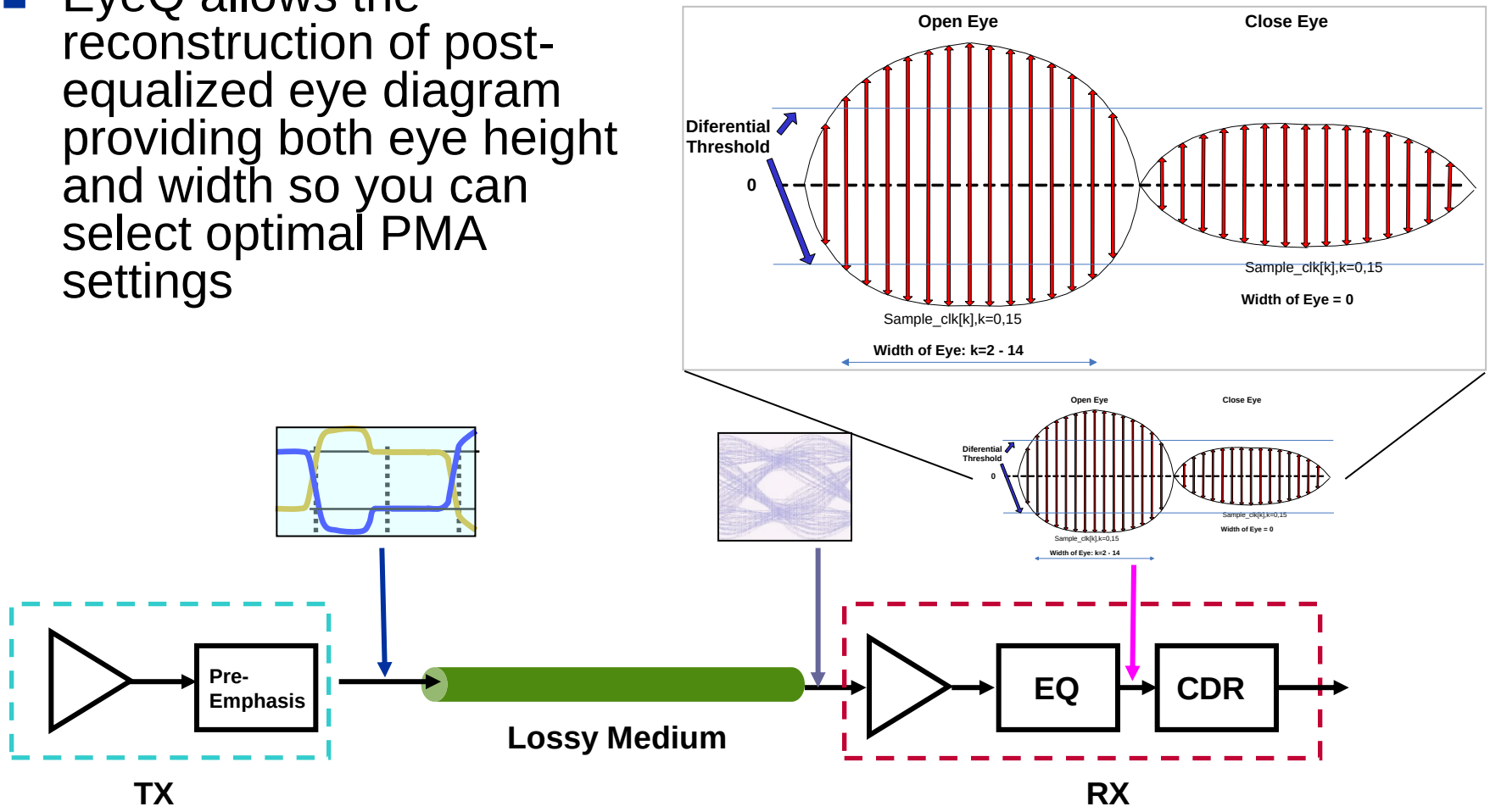
- The Transceiver Toolkit helps users generate designs to control and test transceivers during PCB bring up or in-system signal integrity analysis
- Users can easily control PMA settings, generate and check PRBS patterns to ensure optimal link operation
- Both command line and graphical user interfaces are available

Transceiver Toolkit Features Overview

Features	Description
Transceiver channels	• Consist of full-duplex transmitter (TX) and receiver (RX) channels • Enable and disable each transceiver channel
Dynamic reconfiguration	• Change configuration (e.g. data rate, differential output voltage (V_{OD}), pre- emphasis, decision feedback equalizer (DFE), continuous-time linear equalizer (CTLE), and EyeQ) at run time
EyeQ	• Draw BER bathtub curve and eye contour
DFE	• Enable decision feedback equalization (DFE)
Data pattern generator and checker	• Change test patterns (e.g. pseudo-random binary sequence (PRBS) 7, 15, 23, and 31) at run time
Auto sweep	• Run sweep tests to converge optimal pre-emphasis and EyeQ settings • Provide target BER for error check
Error insertion	• Insert error on serial data in transceiver channel
Status	• Indicate link lock, # of errors, # of transmitted data, and BER
Reporting	• Report settings converged for different BER, equalization, and pre-emphasis
Diagnostics	• Perform serial loopback and reverse serial loopback tests

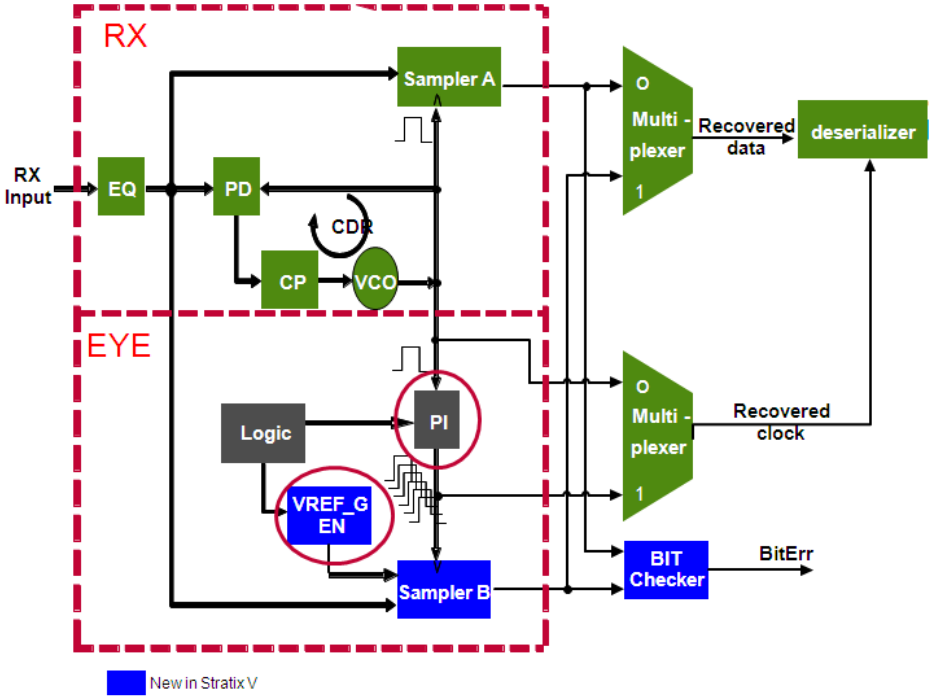
New Transceiver Toolkit Features for Stratix V FPGAs (1/2)

- EyeQ allows the reconstruction of post-equalized eye diagram providing both eye height and width so you can select optimal PMA settings

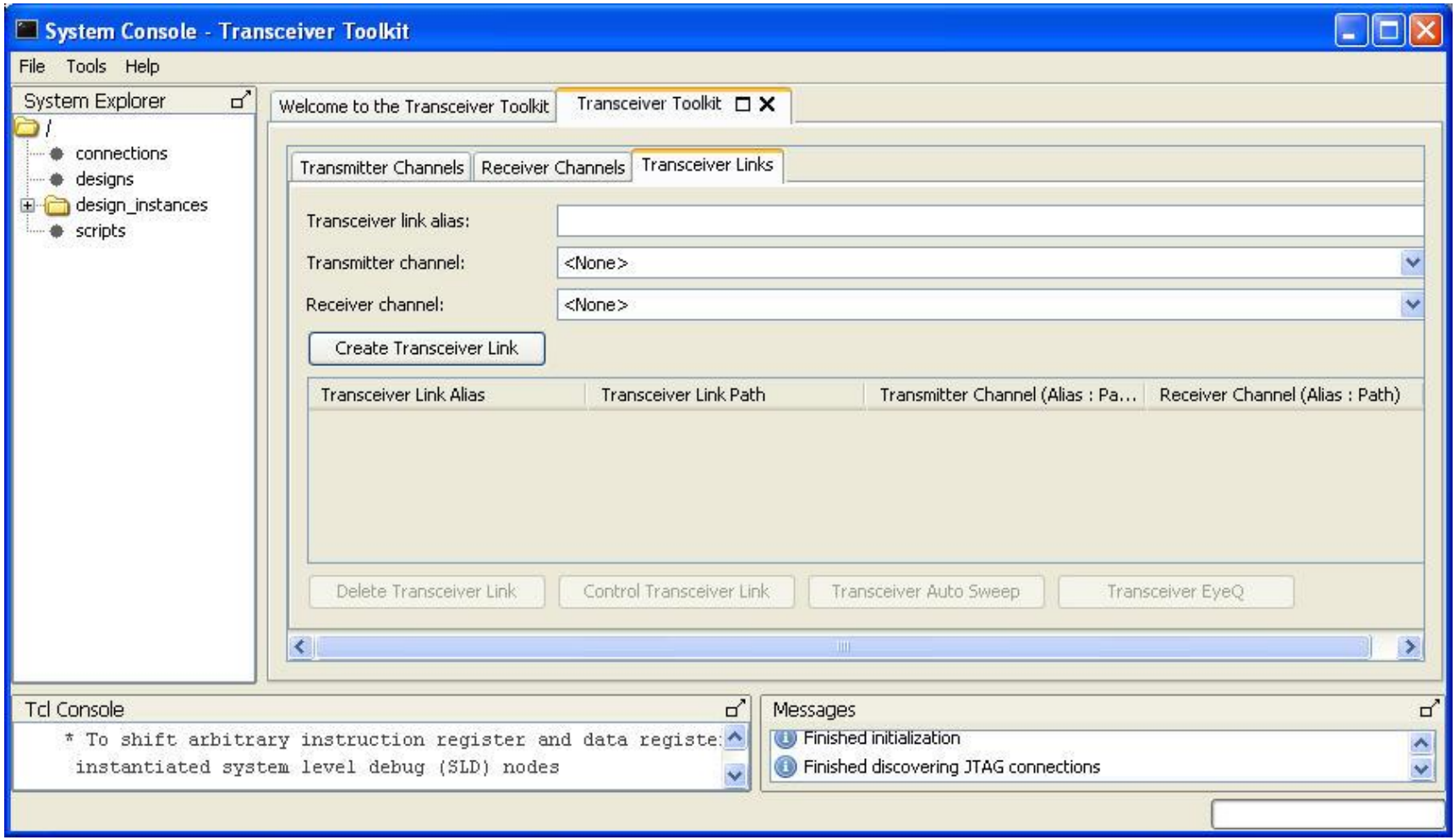


New Transceiver Toolkit Features for Stratix V FPGAs (2/2)

- Stratix V serial bit comparator allows fine tuning of PMA settings with real-time data traffic

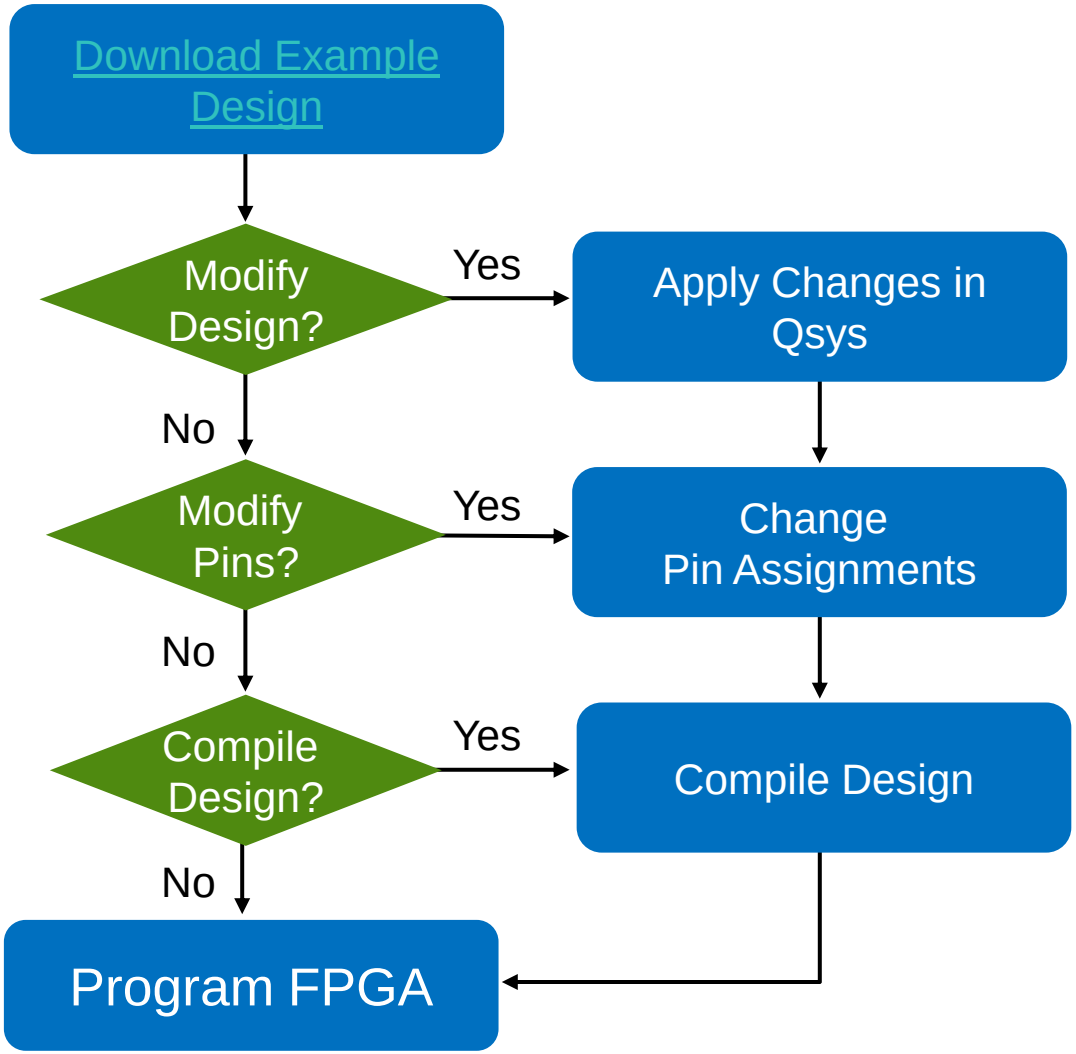


Transceiver Toolkit GUI Overview

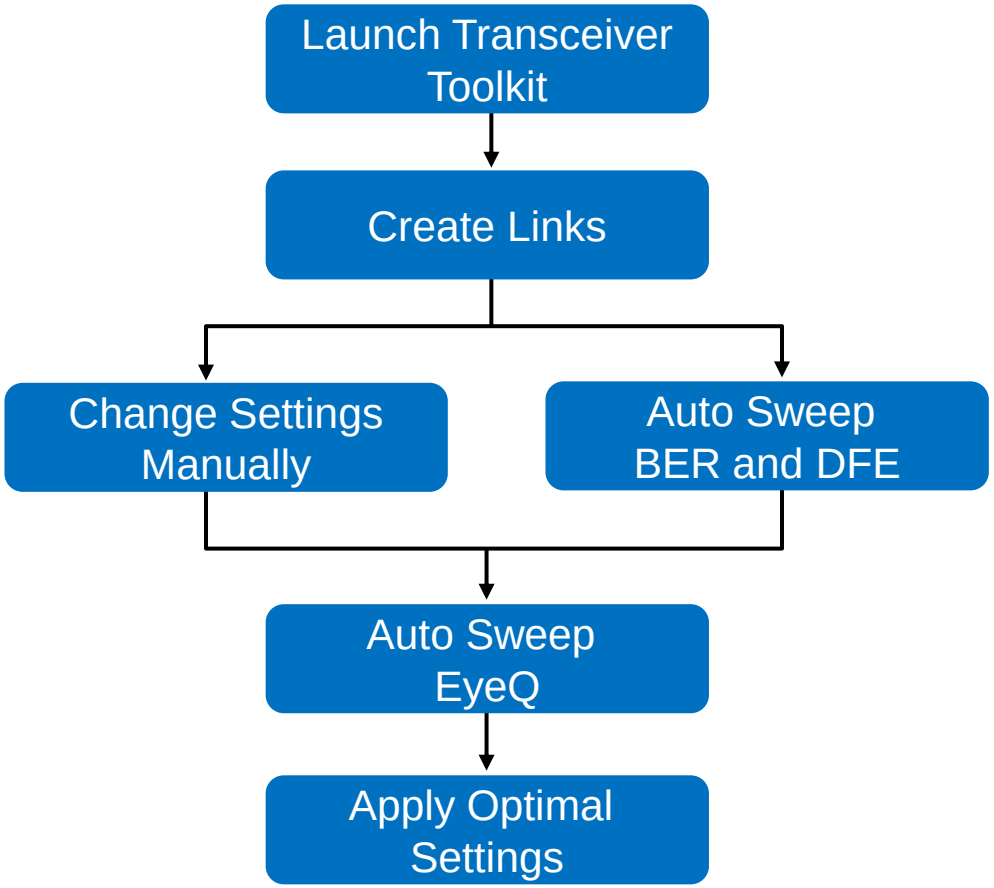


Getting Started

Recommended User Flow (1/2)

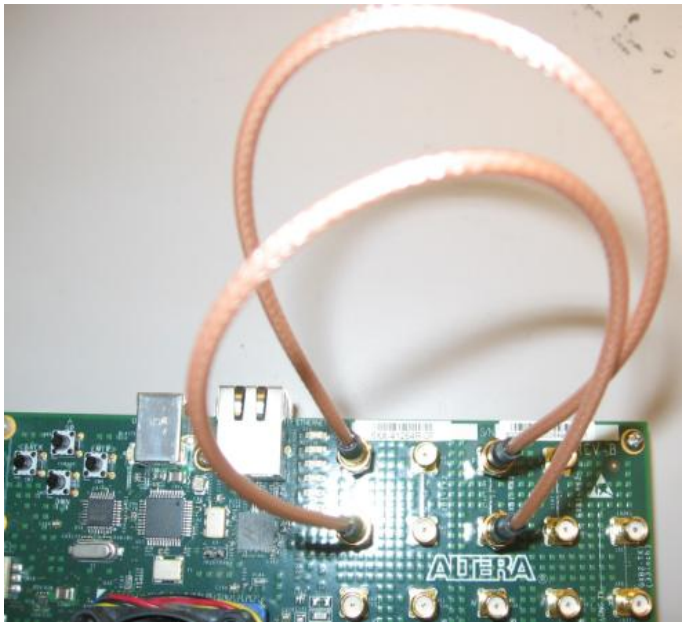


Recommended User Flow (2/2)

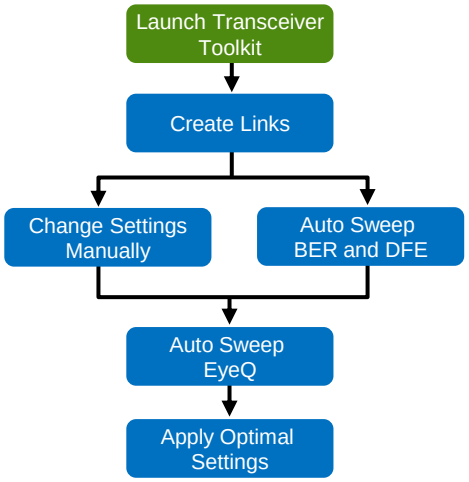


PCB Set-Up

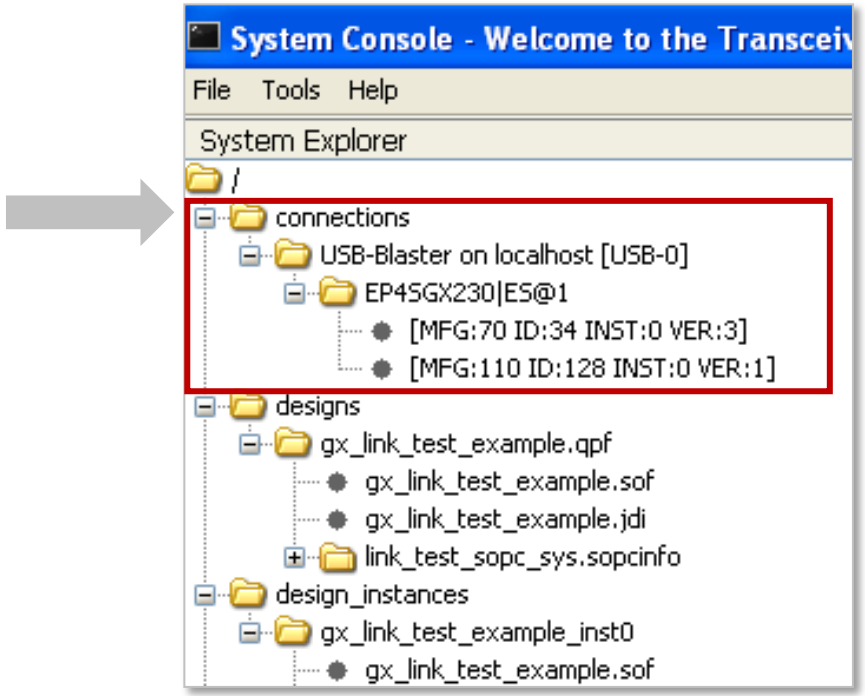
- Power up PCB
- Check if FPGA was configured successfully
- Make sure the links you want to test are connected correctly (e.g. connect cables for external loopback shown below)



Launch Transceiver Toolkit

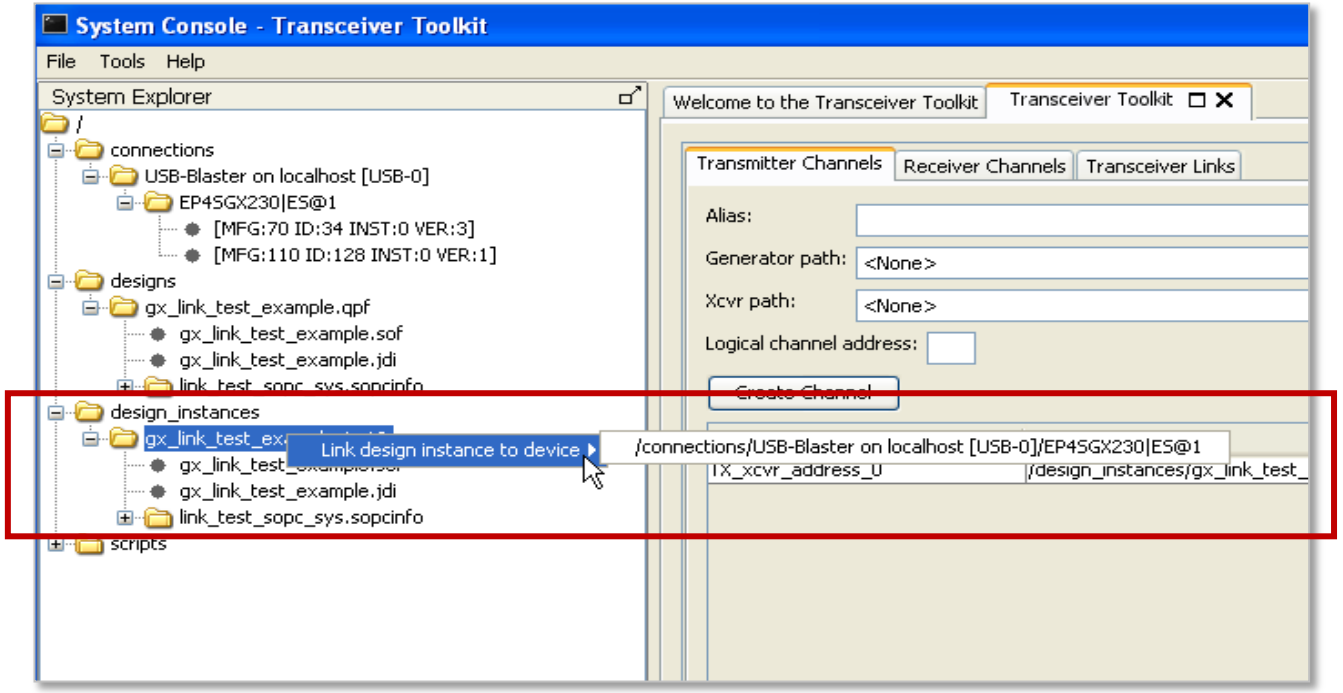


- Click **Transceiver Toolkit** from **Tools** menu in Quartus II software
- From System Explorer window, under "**connections**", check list for your JTAG device
  - If device name does not appear, make sure the device is powered on and connected to the machine
- Load Quartus II project containing transceiver design
  - File → Load Project
- Open Transceiver Toolkit tab
  - Tools → Transceiver Toolkit

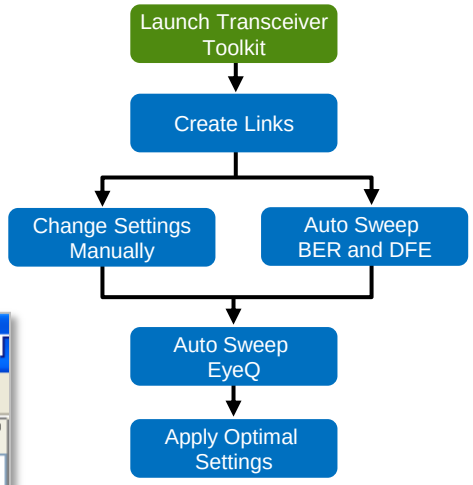


Connect to Targeted Device

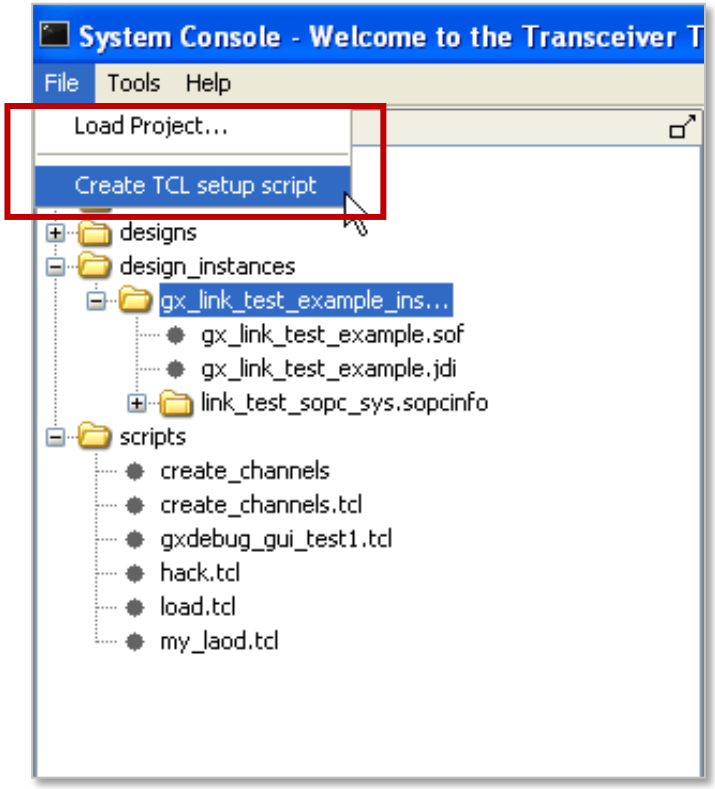
- Linking design instance to device:
  - From System Explorer window, navigate to “**design_instances**”
  - Right click on targeted instance
  - Select your connected device



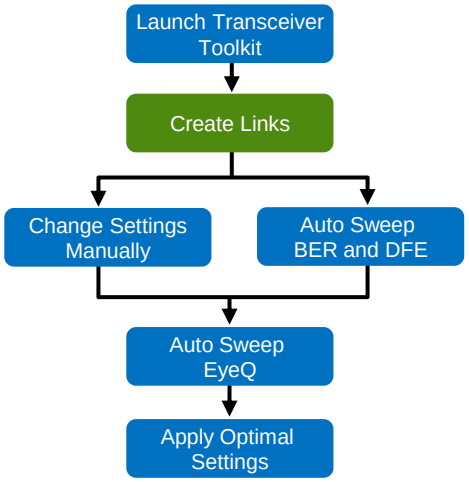
Create Tcl Set-Up Script



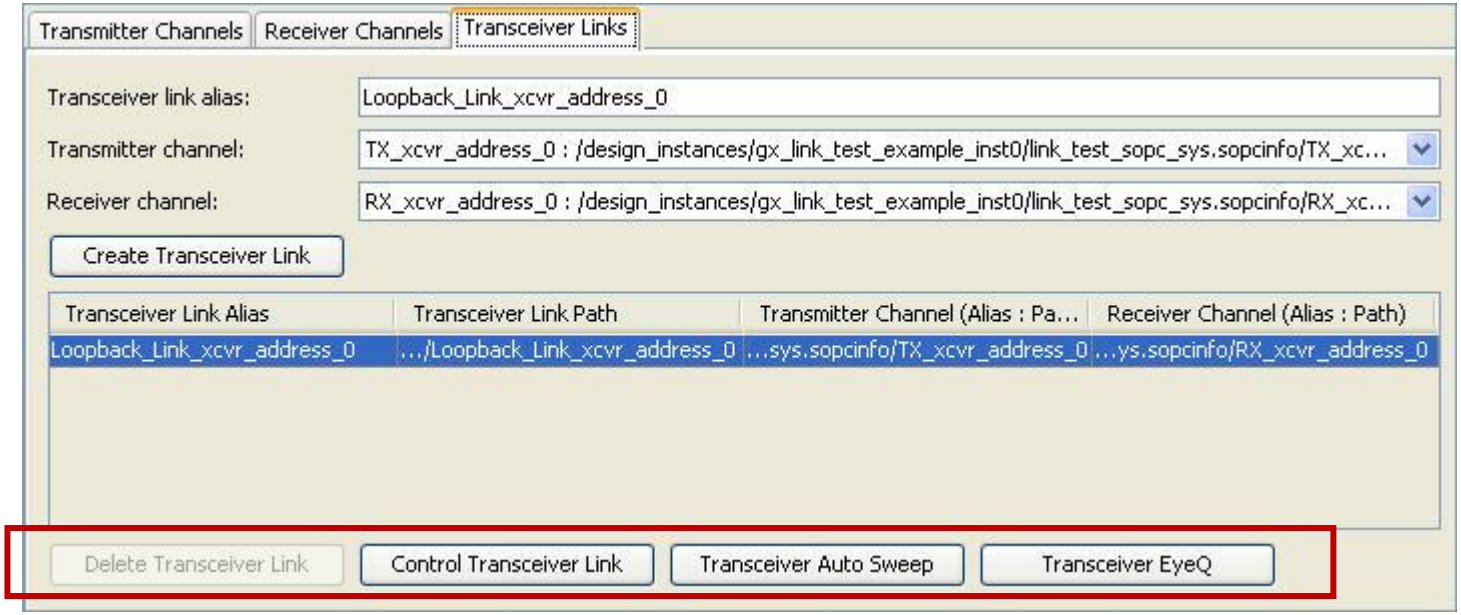
- Automate set-up using Tcl script
  - Click **Save As…** from **File** menu
  - All saved scripts are shown under "**scripts**"
  - Click on a script



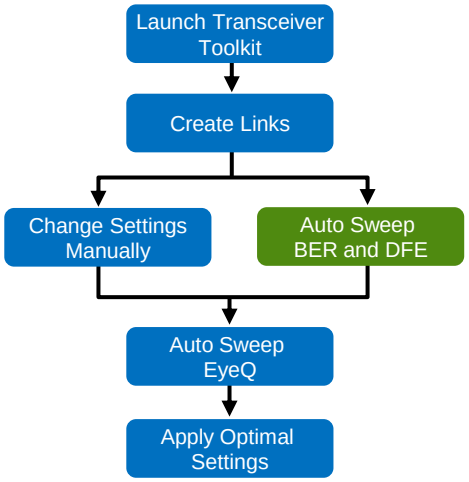
Create Links



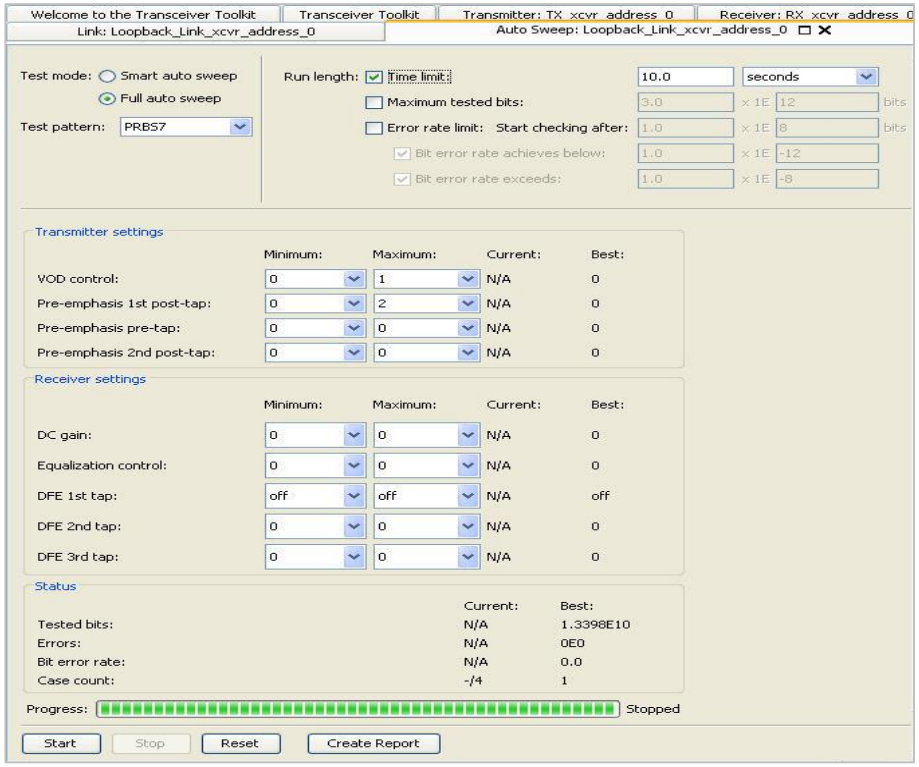
- Transceiver Links tab
  - The channels in your design are auto-populated in the **Transmitter Channels** and **Receiver Channels** tabs
  - By default, a link will be created between the transmitter and receiver of the same channel and shown in **Transceiver Links**



Auto-Sweep BER Tests



- Click **Transceiver Auto Sweep**
  - Choose the Minimum and Maximum values for each setting (e.g. VOD, pre-emphasis, DC gain, equalization, etc.)
  - Case count = number of different permutations will be performed
  - Run length = conditions for stopping the auto-sweep (e.g. time limit per permutation, error rate, etc.)



Auto-Sweep BER Report

- Create reports by clicking **Create Report** in the middle of the test or when the test completes
- Different columns show various transceiver settings
  - All columns can be sorted
- The report is exportable in a .csv format
  - Right click on report, Select "**Export…**"

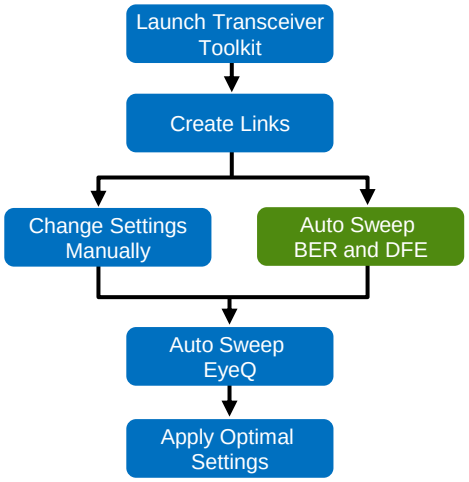
Welcome to the Transceiver Toolkit | Transceiver Toolkit | Transmitter: TX_xcvr_address_0

Receiver: RX_xcvr_address_0 | Link: Loopback_Link_xcvr_address_0 | Auto Sweep: Loopback_Link_xcvr_address_0 | Report: 2010-12-15 14:55:14

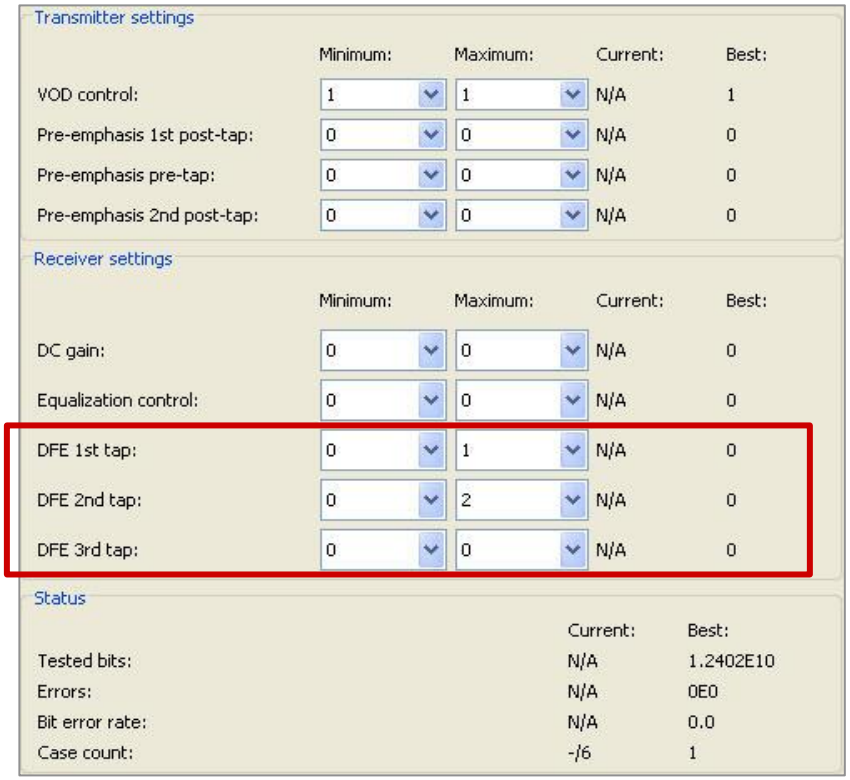
Report: 2010-12-15 14:55:14

	Data Pattern	VOD Control	Pre-emph…	Pre-emph…	Pre-emph…	DC Gain	Equalizati…	DFE 1st Tap	DFE 2nd Tap	DFE 3rd Tap	Phase Step	Tested Bits	Error Bits	BER
1	PRBS7	0	0	0	0	0	0	off	N/A	N/A	off	13398497728	0	0.0
2	PRBS7	1	0	0	0	0	0	off	N/A	N/A	off	13419074304	0	0.0
3	PRBS7	1	1	0	0	0	0	off	N/A	N/A	off	12206997440	0	0.0
4	PRBS7	1	2	0	0	0	0	off	N/A	N/A	off	13398426976	0	0.0

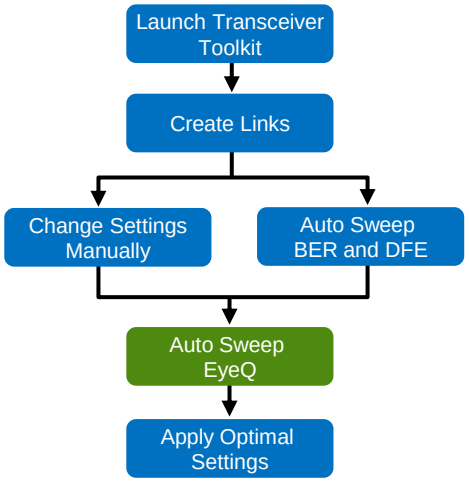
Auto-Sweep DFE Tests



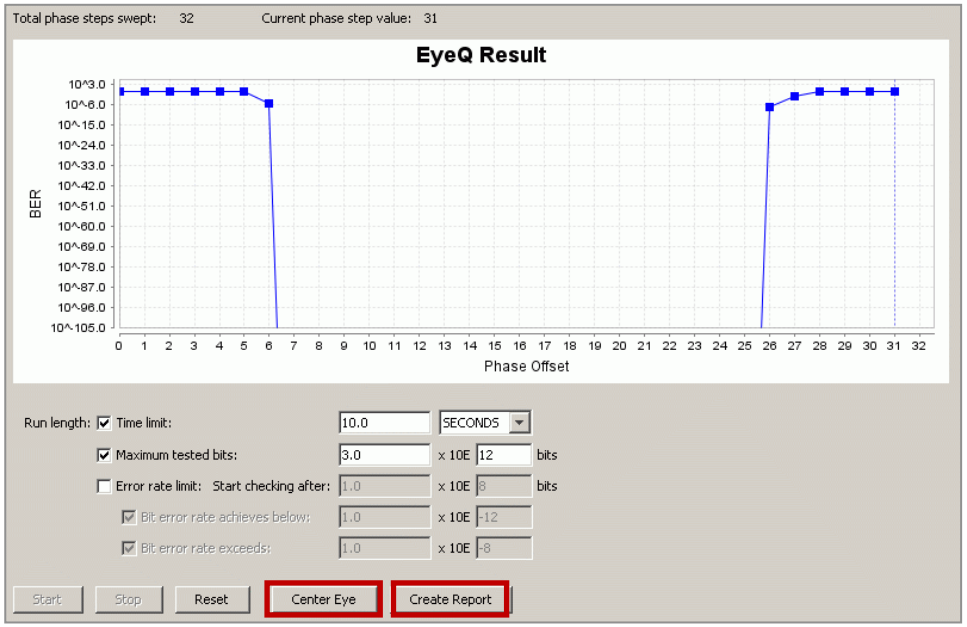
1. Auto sweep with DFE off
2. With best BER results, lock down settings (VOD, pre-emphasis, DC gain, equalization)
3. Then sweep with DFE settings to find best BER



Auto-Sweep EyeQ Tests

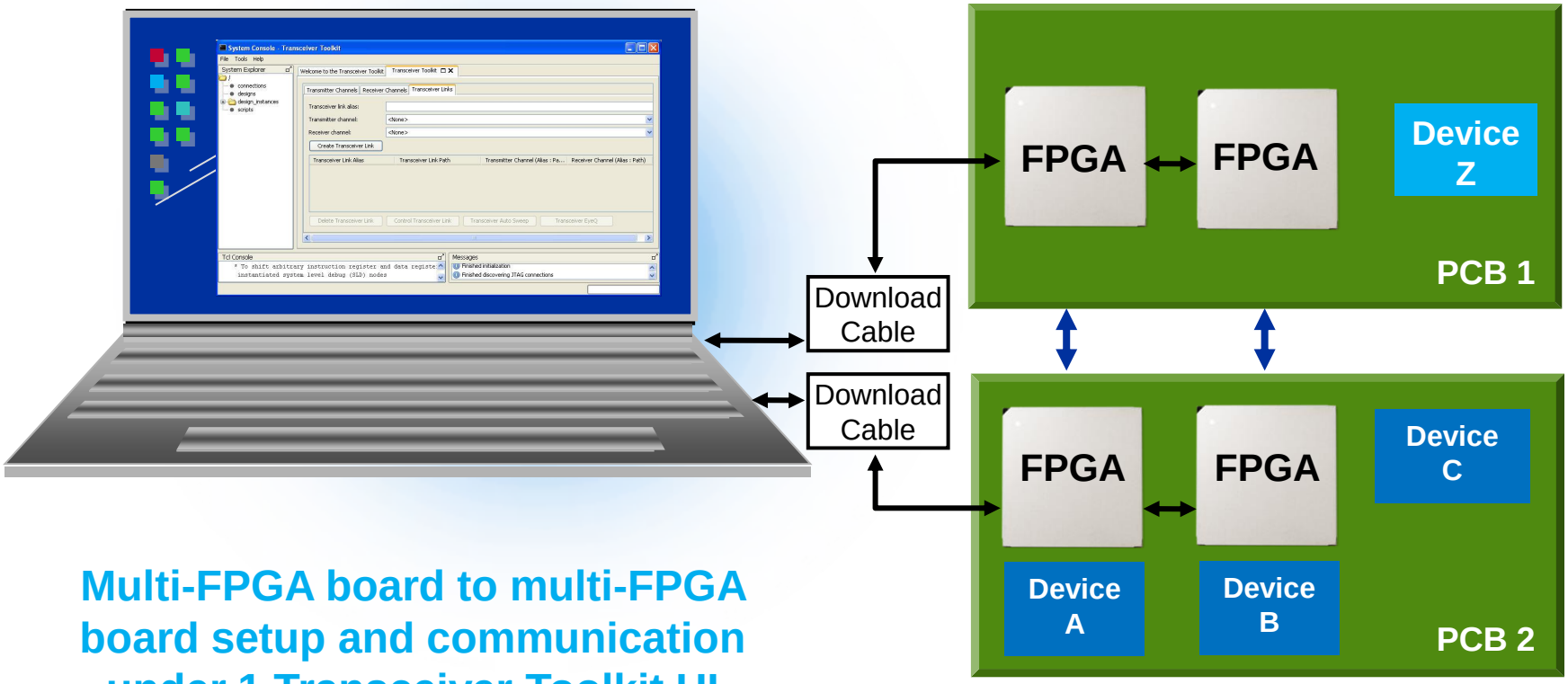


- Click **Transceiver EyeQ** button on **Transceiver Links** tab to launch the EyeQ window
- Bathtub curve automatically generated when sweep completes
  - If you don't see a bathtub curve at the end of the run, click **Center Eye**
- Click **Create Report** to generate EyeQ reports
  - If you sort by BER column, the number of rows with BER = 0 will be considered as the unit width of the eye from the specified physical media attachment (PMA) settings



Board to Board

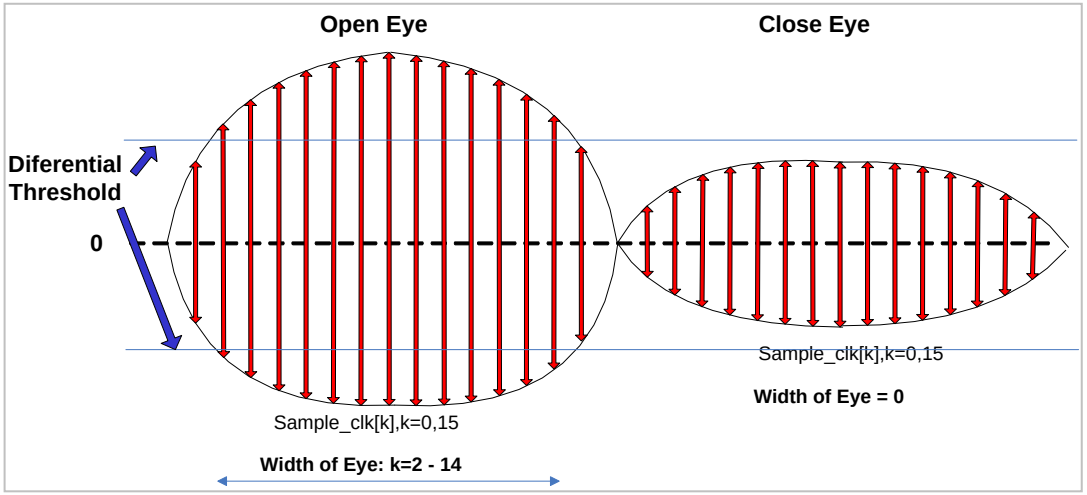
Transceiver Toolkit



Multi-FPGA board to multi-FPGA board setup and communication under 1 Transceiver Toolkit UI

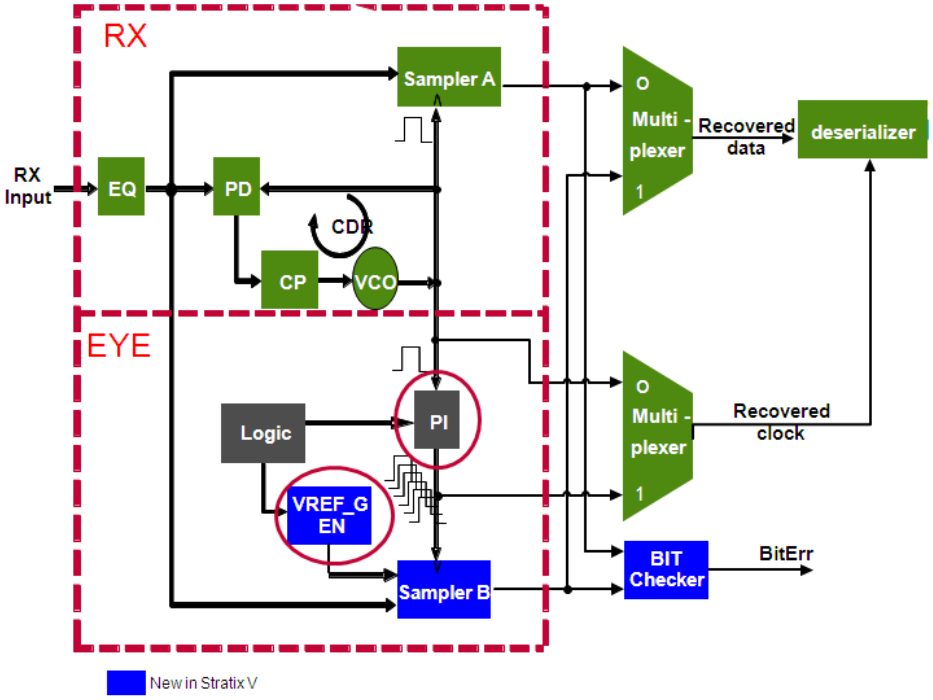
Stratix V EyeQ Test

- Run Stratix V EyeQ to generate the eye contour
  - Use it with DFE



Stratix V Bit Comparator Test

- Run final test by using the fully integrated user design



Demo: 10 minute demo

Demo Steps

- Download example designs
  http://www.altera.com/literature/hb/qts/transceivertoolkit_examples_10_1.zip
- Connect cables correctly on Stratix IV SI board
- Follow steps in **Getting Started** section

Transceiver Toolkit Features Summary

Features	Description	Scope
Transceiver channels	• Consist of full-duplex transmitter (TX) and receiver (RX) channels • Enable and disable each transceiver channel	Block
Dynamic reconfiguration	• Change configuration (e.g. data rate, differential output voltage (V_{OD}), pre- emphasis, decision feedback equalizer (DFE), continuous-time linear equalizer (CTLE), and EyeQ) at run time	Channel
EyeQ	• Draw BER bathtub curve and eye contour	Receiver
DFE	• Enable DFE	Receiver
Data pattern generator and checker	• Change test patterns (e.g. pseudo-random binary sequence (PRBS) 7, 15, 23, and 31) at run time	Channel
Auto sweep	• Run sweep tests to converge optimal pre-emphasis and EyeQ settings • Provide target BER for error check	Channel
Error insertion	• Insert error on serial data in transceiver channel	Channel
Status	• Indicate link lock, # of errors, # of transmitted data, and BER	Channel
Reporting	• Report settings converged for different BER, equalization, and pre-emphasis	Channel
Diagnostics	• Perform serial loopback and reverse serial loopback tests	Channel

Summary

- The Altera Transceiver Toolkit provides a very effective way to plan and bring-up your transceiver links

- Altera Stratix V FPGAs provide a series of features that make high-speed transceiver design easier and get you to market sooner.

Further Reading

- Altera literature
  - Transceiver toolkit handbook
  - Transceiver toolkit on-line demo
  - Download this presentation and collateral from: ftp.altera.com/outgoing/2011_design_seminars/
- Training courses
  - Altera on-line transceiver training (free)
  - Transceiver toolkit training (free)
  - Dr Bogatin Signal Integrity Courses
- Stratix V web pages
  - Stratix V FPGAs
  - Altera transceiver portfolio

Stratix V FPGA Design Seminars 2011

- Are you interested in learning more?

	Stratix V FPGA Design Seminar Topics
1	Designing with Partial Reconfiguration in Stratix V FPGAs
2	10Gbps Backplane Design and Optimization Using Stratix V FPGAs
3	Designing 28Gbps With Confidence
4	Minimizing Circuit Board Design Costs for Stratix V FPGAs
5	High-Speed Transceiver Toolkit
6	Using fPLLs in Stratix V FPGAs for Fractional-N Synthesis
7	Oscillator Replacement for Optical Transport Network (OTN) Applications
8	Using Variable Precision DSP Block in Stratix V FPGAs
9	Implementing Floating Point DSP Using Stratix V FPGAs
10	Optimizing Power and Performance in Stratix V FPGA Designs
11	Designing High-Performance External Memory Interfaces with Stratix V FPGAs
12	Using Configuration via PCIe in Stratix V FPGAs

Thank You

High-Speed Transceiver Toolkit

Stratix V FPGA Design Seminars 2011