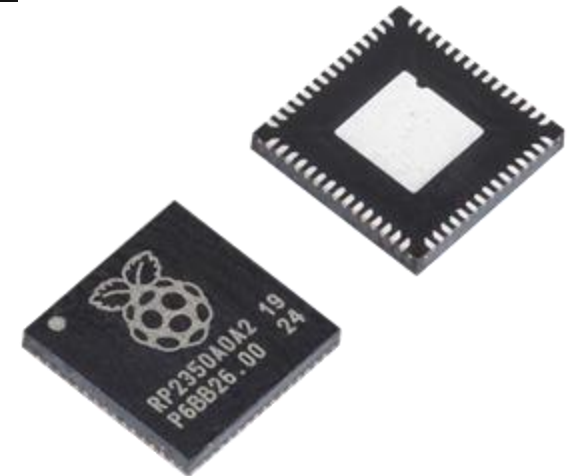
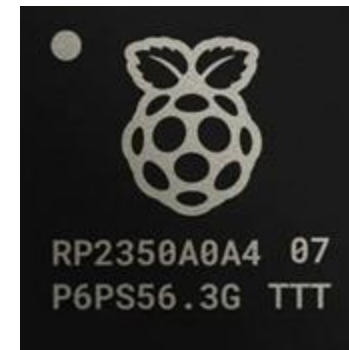


Raspberry Pi - RP235x Microcontroller

INSEM (www.insem.co.kr)

The RP235x is a new family of microcontrollers from Raspberry Pi, offering significant enhancements over the RP2040.

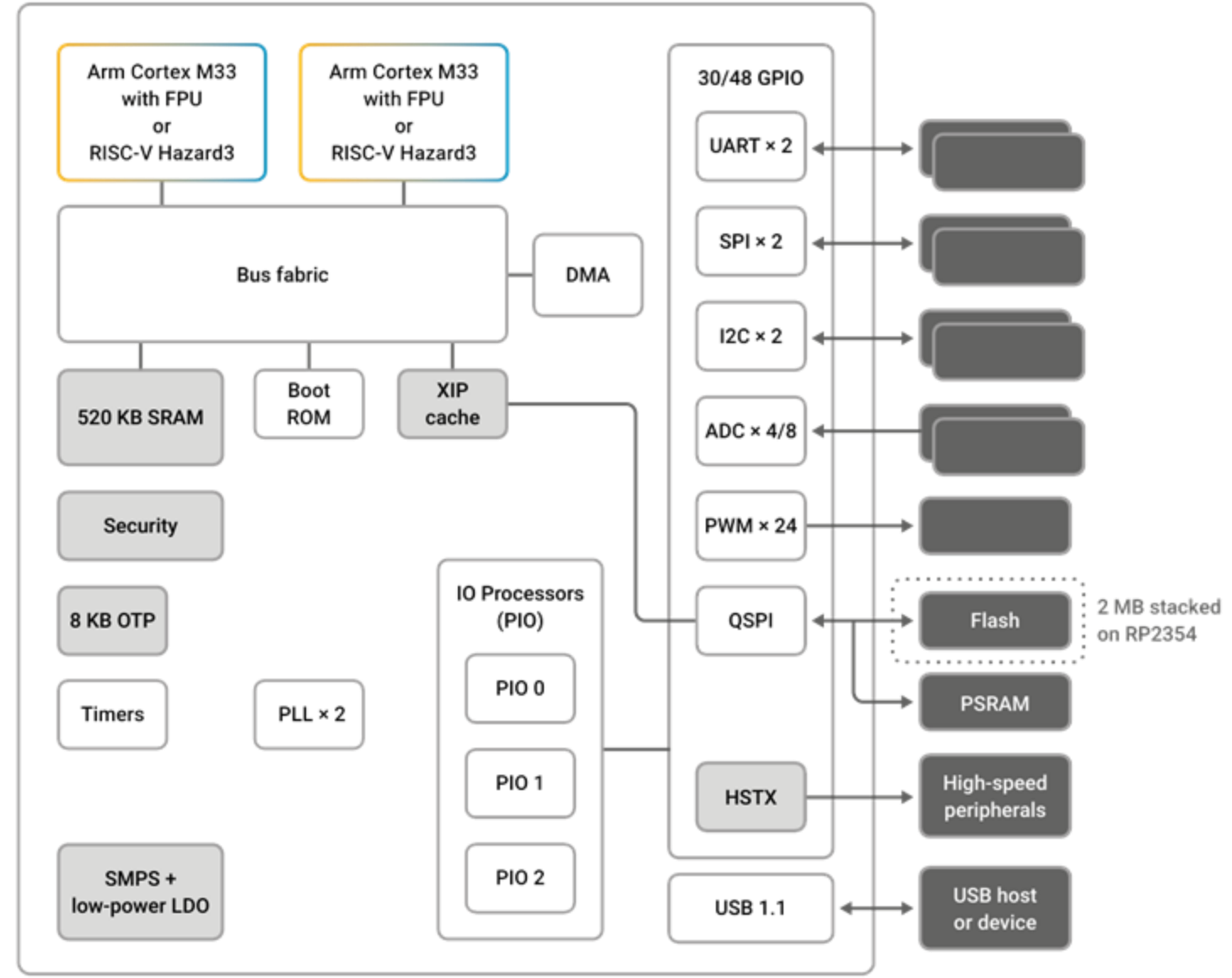
- Dual Cortex-M33 or Hazard3 processors at 150 MHz
- ARM TrustZone for Cortex-M
- 520 kB on-chip SRAM, in 10 independent banks
- 8 kB of one-time-programmable storage (OTP)
- Up to 16 MB of external QSPI flash/PSRAM via dedicated QSPI bus
- 2× on-chip PLLs for internal or external clock generation
- Hardware SHA-256 accelerator and TRNG
- 2× UARTs Controllers.
- 2× SPI controllers
- 2× I2C controllers
- 24× PWM channels
- 12× PIO state machines
- 1× HSTX peripheral



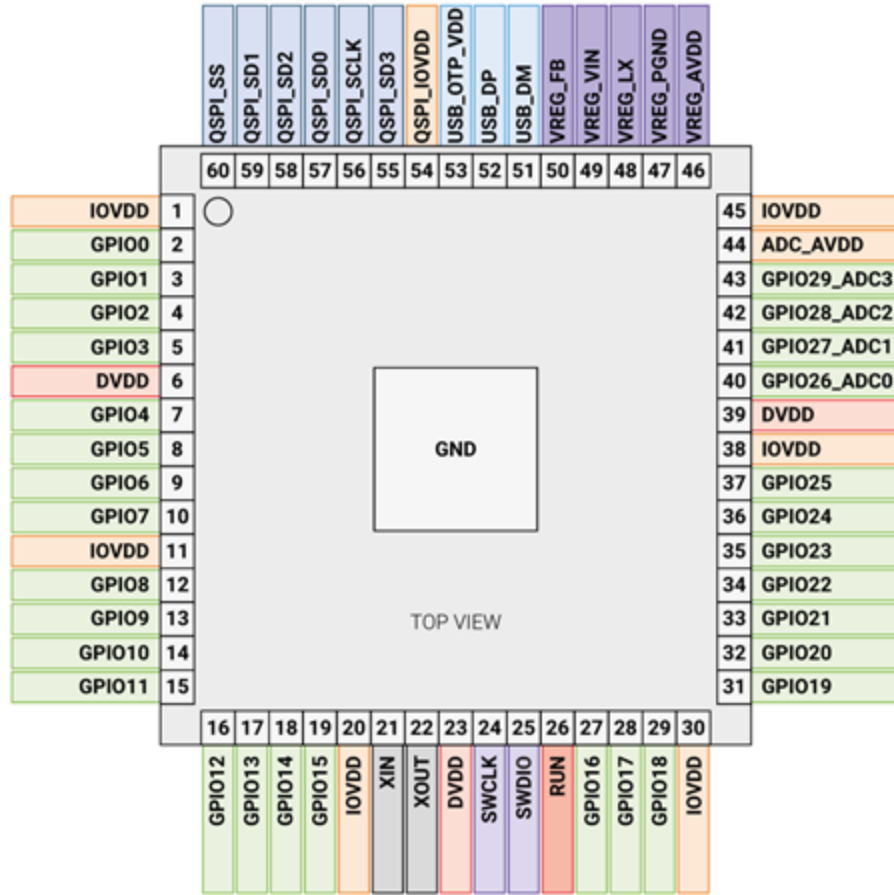
RP235x Device Family

Product	Package	Core	Speed (MHz)	Ext. Flash	Int. Flash	RAM	USB	PIO	SPI	ADC (12bit)	UART	I2C	PWM	I/Os	Voltage (V)	Temperature (°C)
RP2350A	QFN-60	Dual (M33, RISC-V)	150	16MB	x	520KB	1.1 (Host,Device)	3	2	4	2	2	24	30	1.8~3.6	-40 ~ 85
RP2350B	QFN-80	Dual (M33, RISC-V)	150	16MB	x	520KB	1.1 (Host,Device)	3	2	8	2	2	24	48	1.8~3.6	-40 ~ 85
RP2354A	QFN-60	Dual (M33, RISC-V)	150	16MB	2MB	520KB	1.1 (Host,Device)	3	2	4	2	2	24	30	1.8~3.6	-40 ~ 85
RP2354B	QFN-80	Dual (M33, RISC-V)	150	16MB	2MB	520KB	1.1 (Host,Device)	3	2	8	2	2	24	48	1.8~3.6	-40 ~ 85

- RP2350A and RP2354A are pin-to-pin compatible.
- USB 2.0 High Speed (480 Mb/s) is not supported.
- RP2354A and RP2354B have built-in flash memory (2 MB)



RP2350A (QFN-60 / 7*7mm)



- GPIOx**
- GPIOx/ADCy**
- QSPIx**
- USB_DM and USB_DP**
- XIN and XOUT**
- RUN**
- SWCLK and SWDIO**
- GND**
- QSPI_IOVDD**
- IOVDD**
- USB_OTP_VDD**
- ADC_AVDD**
- VREG_VIN**
- VREG_FB**
- VREG_LX**
- VREG_PGND**
- VREG_AVDD**
- DVDD**

General-purpose digital input and output

General-purpose digital input and output, with analogue-to-digital converter function

Interface to an SPI, Dual-SPI or Quad-SPI flash device, with execute-in-place support

USB controller, supporting full-speed device and full-/low-speed host

Connect a crystal to RP2350's crystal oscillator

Global asynchronous reset pin; reset when driven low, run when driven high

Access to the internal Serial Wire Debug multi-drop bus; provides debug access to both processors

Single external ground connection, bonded to a number of internal ground pads on the RP2350 die

Provides the IO supply for the chip's QSPI interface

Power supply for digital GPIOs, nominal voltage 1.8 V to 3.3 V

Power supply for internal USB full-speed PHY and OTP, nominal voltage 3.3 V

Power supply for analogue-to-digital converter, nominal voltage 3.3 V

Power input for the internal core voltage regulator, nominal voltage 2.7 V to 5.5 V

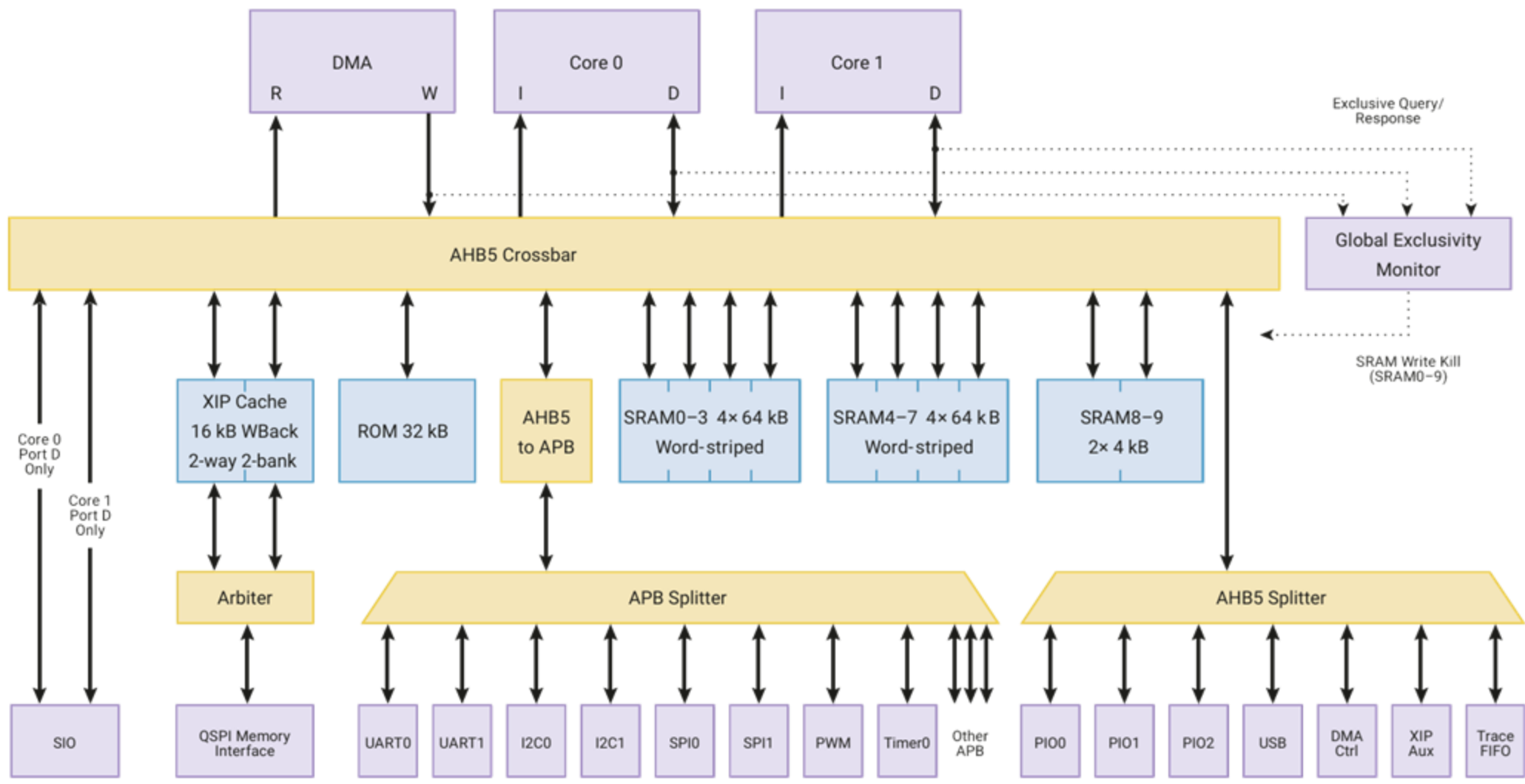
Internal core voltage regulator: See datasheet

Internal core voltage regulator: See datasheet

Internal core voltage regulator: See datasheet

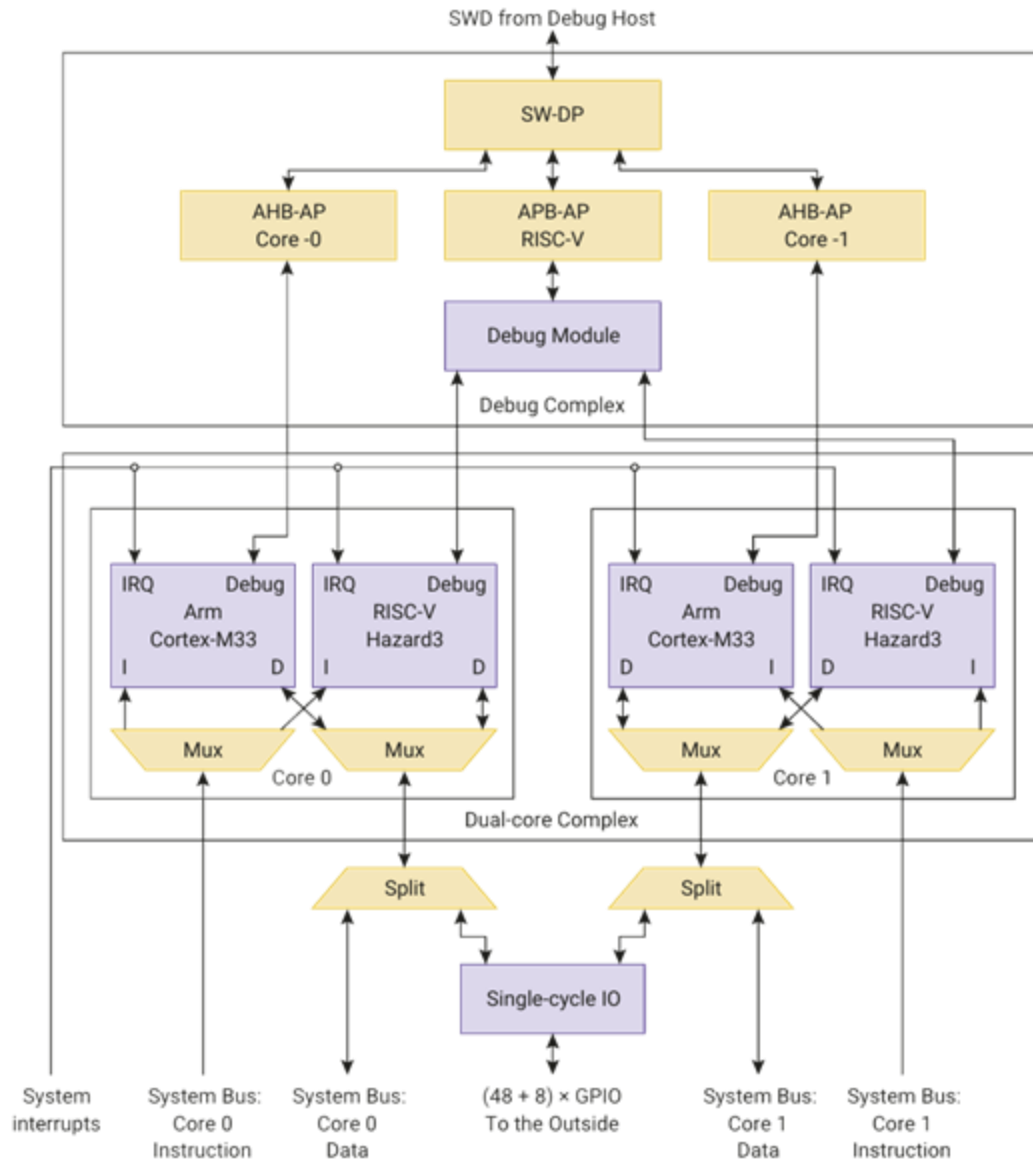
Internal core voltage regulator: See datasheet

Digital core power supply, nominal voltage 1.1 V



RP235x Address Map

Bus Segment	Base Address	Detail
ROM	0x00000000	Boot code execution address after reset and Reset vector address
XIP	0x10000000	64MB Space(The lower 32 MB is assigned to QSPI, and the upper 32 MB is reserved.)
SRAM	0x20000000	SRAM Start Address(Max: 520KByte)
APB Peripherals	0x40000000	ex) SPI, Uart, ADC
AHB Peripherals	0x50000000	ex) DMA, PIOx, HSTX
SIO	0xD0000000	Access is always zero-wait-state
Cortex-M33 Private registers	0xE0000000	Systick Timer



- **Symmetric dual-core system**
 - Cortex-M33 + RISC-V Hazard3.
 - The instruction bus and data bus are physically separated.

- **Each Core can be selected at boot time**
 - Cortex-M33 is the default option.

- **Each core has a pair of 32-bit AHB5 links to the system bus**

- **ROM (32KByte, Read Only)**

- Core 0 Boot code : The first code executed when the chip is powered on, initializing the system.
- USB bootloader : Mass storage interface for drag and drop of UF2 flash and SRAM binaries.

- **SRAM(520KByte, SRAM0~9)**

- SRAM can be allocated and managed linearly.
- SRAM0~3(4*64KB), SRAM4~7(4*64KB), SRAM8~9(2*4KB)

- **XIP(16KByte Cache)**

- External flash and PSRAM are accessible through the Execute-in-Place (XIP) subsystem.

- **OTP(8KByte, one-time-programmable)**

- Manufacturing information such as unique device ID.
- Boot configuration(Cortex-M33 or RISC-V) and Secure Boot.(Public key fingerprint)

- **Partition Tables (Max 16 Regions)**

- Save multiple execution images: A/B boot versions, different architectures (Arm/RISC-V)

- **Flash Permissions (Secure, Non-secure, bootloader)**

- Define read (R) and write (W) permissions for the flash area.

- **Image Definitions**

- Determines whether the image is normal and executable.: Entry-Point, Architecture(Arm/RISC-V), load Address

- **Flash Image Boot(Default Boot)**

- Search the first 4kB area of the external flash memory, and if *IMAGE_DEF* is valid, proceed with booting.

- **Flash Partition Boot (Advance Boot)**

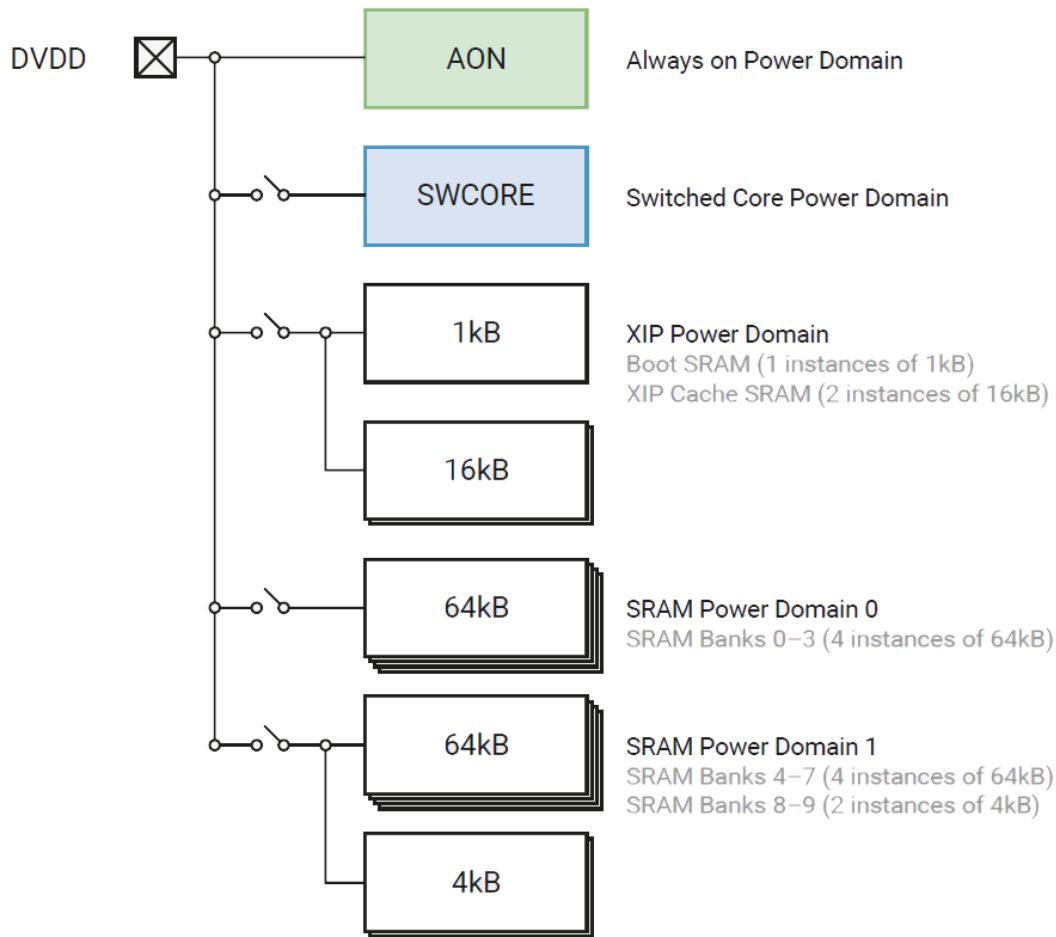
- If A/B Versions, it searches for two partitions and boots with the latest version.

- **USB Boot (UF2 Download)**

- UF2 files are a file format created to allow firmware updates.
- The UF2 file contains 32-bit family ID information.(eg. rp2350-arm-ns, rp2350-risc v)

Sequence	Description
Entry	Bootrom Process Start
Core 1 Wait	Active (Core 0) , Sleep (Core 1)
Boot Path Start	Find a valid boot image
Await Rescue	Recovery request by debugger(RESCUE_FLAG)
Generate Boot Random	Secure boot and random number generation
Check POWMAN Vector	POWMAN Check(Core, SRAM)
Check Watchdog Vector	Watchdog Check(ex:SCRATCH4 – USB bootloader address)
Prepare for Image Boot	Clock Configure, QSPI Initial
Try RAM Image Boot	Execute the boot image located in RAM
Check BOOTSEL	QSPI CSn is low (BOOTSEL button) or watchdog type is BOOTSEL
Try OTP Boot	Execute the boot image stored in OTP (One-Time Programmable) memory
Try Flash Boot	Execute the boot image stored in flash (XIP) memory

RP235x Core Power Domain



- **AON(Always On)**
 - Small amount of logic that is always powered on when chip's core supply (DVDD) is available.
- **SWCORE(Switched Core)**
 - the remaining core logic functions, including processors, bus fabric, peripherals, etc.
- **XIP**
 - XIP cache SRAM and Boot RAM
- **SRAM0(SRAM Power Domain 0)**
 - the lower half of the large SRAM banks.
- **SRAM1(SRAM Power Domain 1)**
 - the upper half of the large SRAM banks, and the scratch SRAMs.

RP235x Power Supply Spec

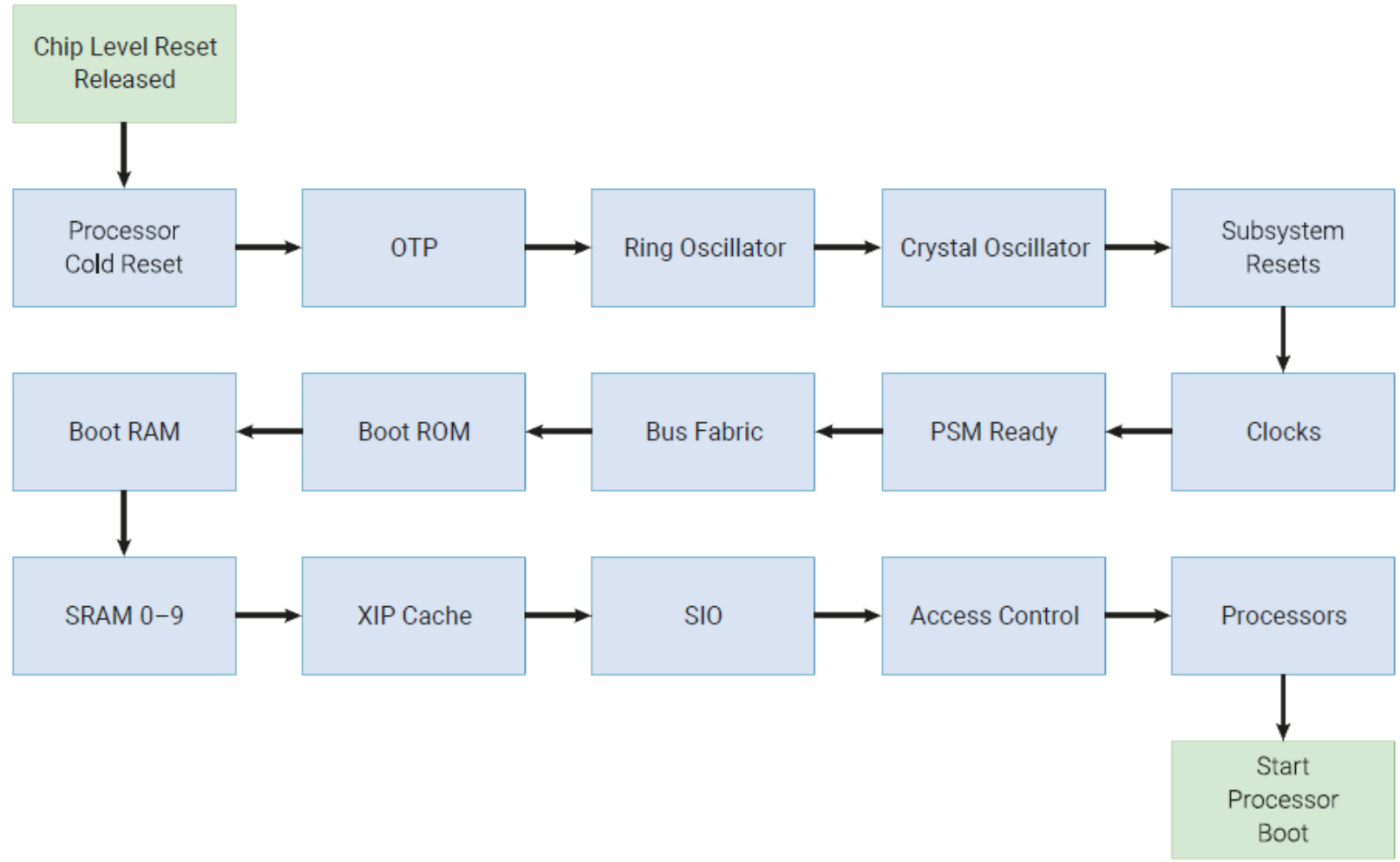
Power Supply	Supplies	Min	Typ	Max	Units
IOVDD	Digital IO	1.62	1.8 / 3.3	3.63	V
QSPI_IOVDD (RP2350)	Digital IO	1.62	1.8 / 3.3	3.63	V
QSPI_IOVDD (RP2354)	Digital IO	2.97	3.3	3.63	V
DVDD	Digital core	1.05	1.1	1.16	V
VREG_VIN	Voltage regulator	2.7	3.3	5.5	V
VREG_AVDD	Voltage regulator	3.135	3.3	3.63	V
USB_OTP_VDD	USB PHY & OTP	3.135	3.3	3.63	V
ADC_AVDD	ADC	1.62	3.3	3.63	V

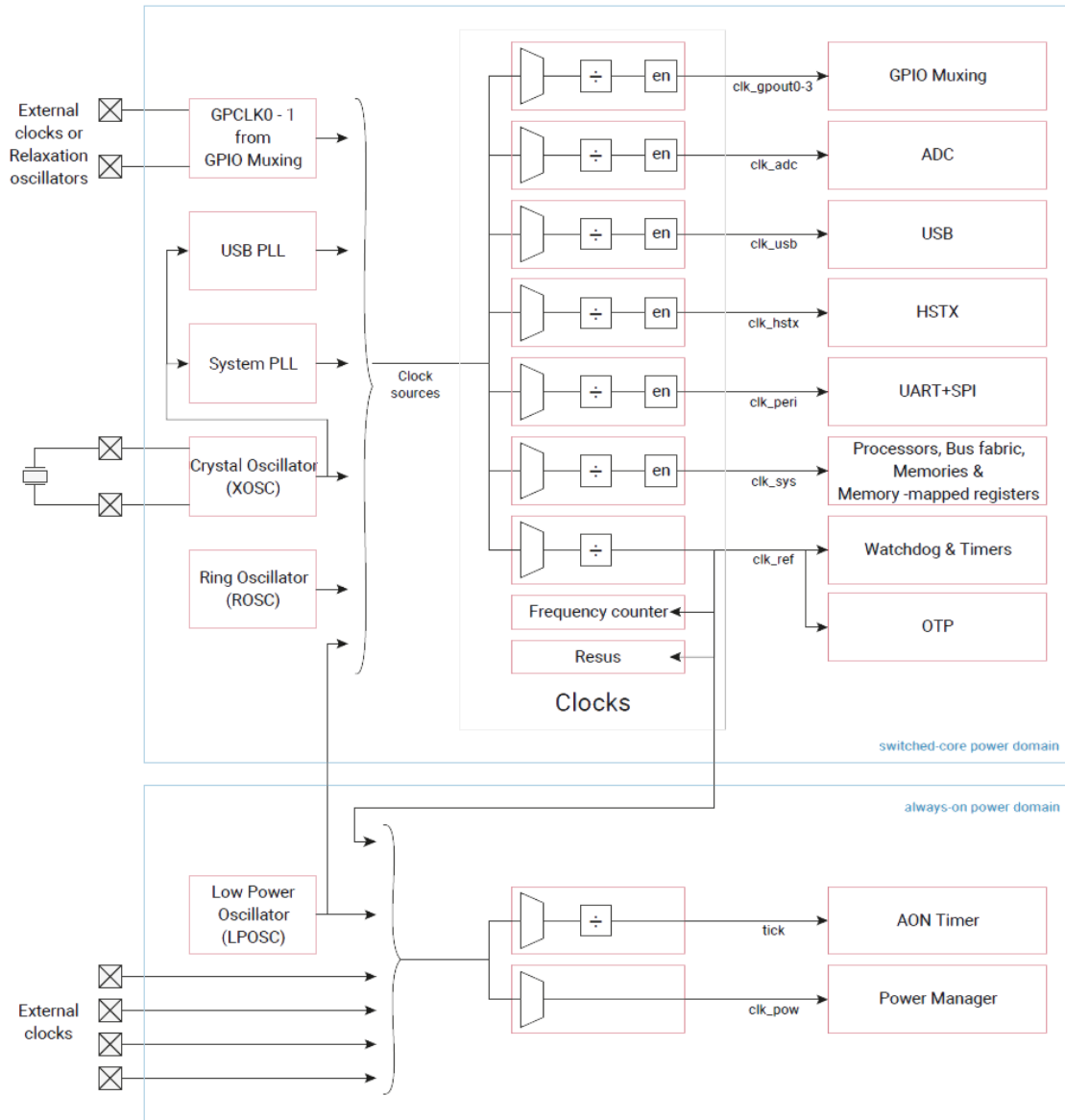
RP235x Reset Type

Reset Type	Scope	Reset source	Description
Chip-level Reset	Entire chip	Hardware events(POR,Glitch), Watchdog, Debugger	Puts the chip into a default state
System Reset	Core system components (CPU, Bus, OTP, etc.)	Power-on State Machine (PSM)	Chip-level Reset --- > System Reset
Subsystem Reset	Peripherals (USB,PIO,PLL,ADC, etc)	Software, Watchdog, Debugger	Peripherals can be selectively reset

- RP235x Reset Sequence : Chip-level Reset -- > System Reset -- > Subsystem Reset

RP235x PSM (Power-On State Machine Sequence)





• Clocks Sources

- XOSC, ROSC, LPOSC, External Clocks

• PLL

- USB PLL, SystemPLL

• Always On Domain

- LPOSC, AON Timer, Power Manager

• Clock Generator

Clock	Description	Nominal Frequency
CLK_REF	ROSC or XOSC	6 ~ 12MHz
CLK_SYS	System Clock	150MHz
CLK_PERI	UART, SPI, I2C....	12 ~ 150MHz
CLK_USB	USB	48MHz
CLK_ADC	ADC	48MHz
CLK_HSTX	HSTX	150MHz

- **XOSC (Crystal Oscillator)**

- Supports 1 MHz to 50 MHz crystal.
- Recommend Clock is 12MHz crystal.

- **ROSC(Ring Oscillator)**

- ROSC is On-Chip Oscillator. (Internal RC)
- Nominal Clock is 11MHz. (After stabilization of ROSC, trade-offs to XOSC.)

- **LPOSC(Low Power Oscillator)**

- Clock supply to the AON Timer in low power mode.
- Nominal Clock is 32.768KHz.

• GPIOs

18

- QFN-60 package(RP2350A) : Provides 30 user GPIOs.
- QFN-80 package(RP2350B) : Provides 48 user GPIOs.

• External Interrupt and WakeUp

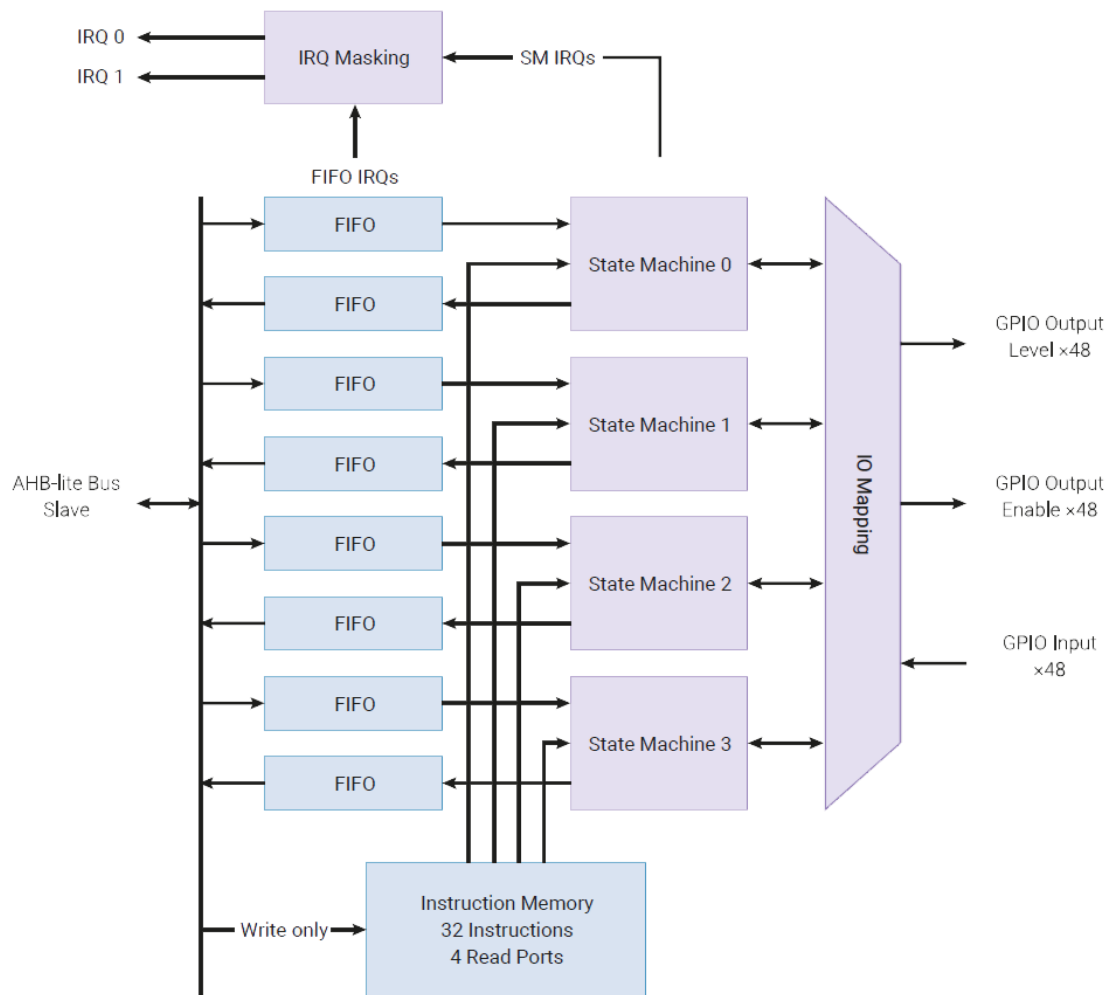
- Level High, Level Low, Edge High, Edge Low
- Can be used to wake up from low-power mode (up to 12 sources).

• Functional Select

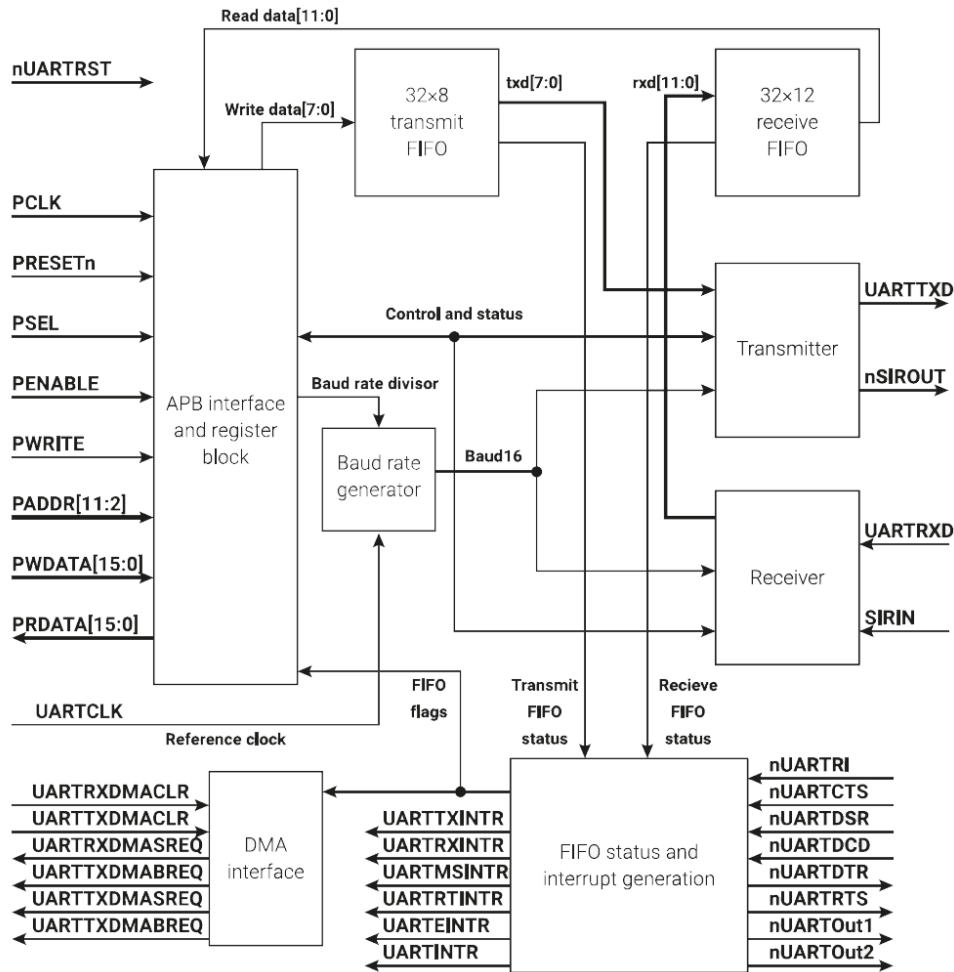
- Each GPIO pin can be connected to one of several peripherals(UARTx,I2Cx....) or functions.
- Controlled by the FUNCSEL bit of the GPIO0_CTRL register. (ex : 0x02 → UART0_TX, 0x03 → I2C0_SDA)

• Bus Keeper Mode and Pad Isolation Latches

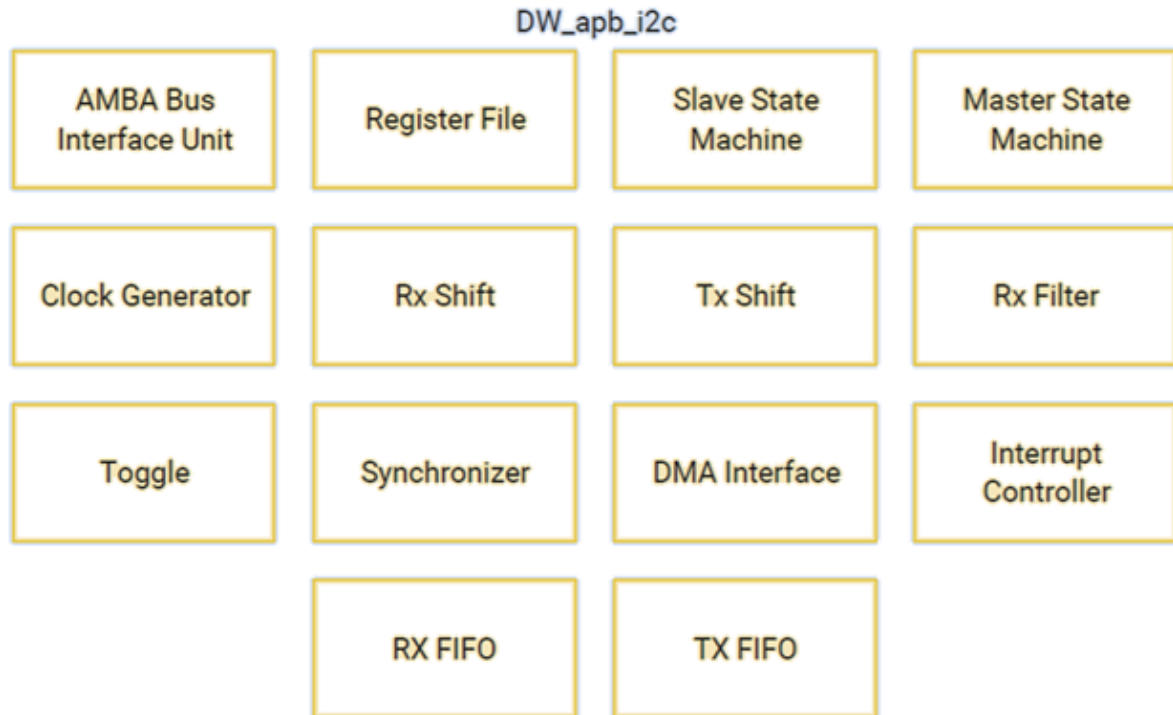
- The purpose is to ensure the stability of GPIO pins and reduce current consumption.
- Pad Isolation Latches are used in low power mode.



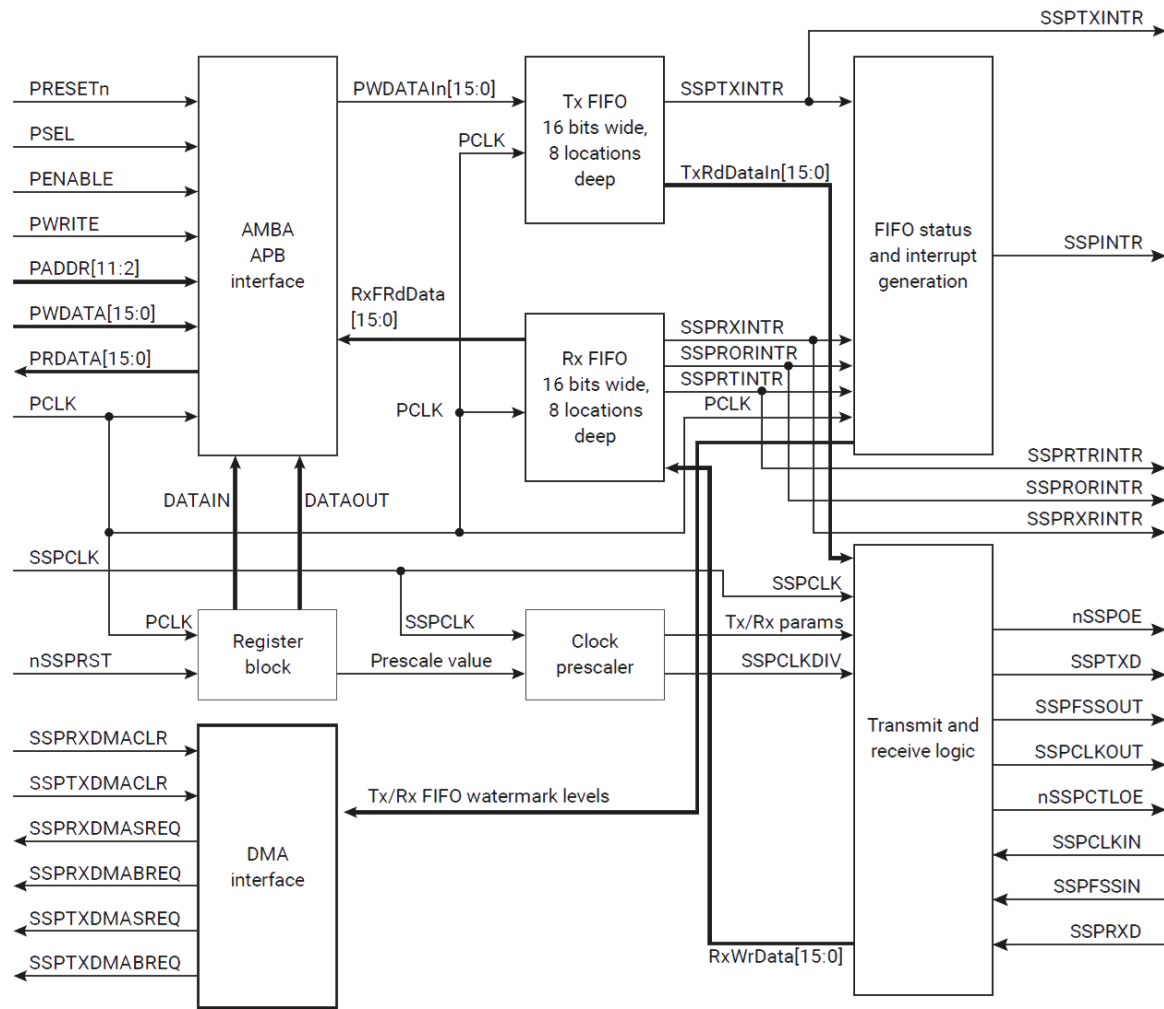
- The PIO (Programmable Input/Output) block is a versatile hardware interface.
- PIO functionality reduces CPU load.
- PIO Channel and State Machines
 - 3 x PIO Channel(PIO0~PIO2)
 - 12 x State Machines (4 per PIO channel)
- Supported I/O Standards
 - 8080 and 6800 parallel bus, I2C, SDIO, QSPI, UART ...
- Supported I/O Non-Standards
 - Custom LED Control, Special Sensor Protocol



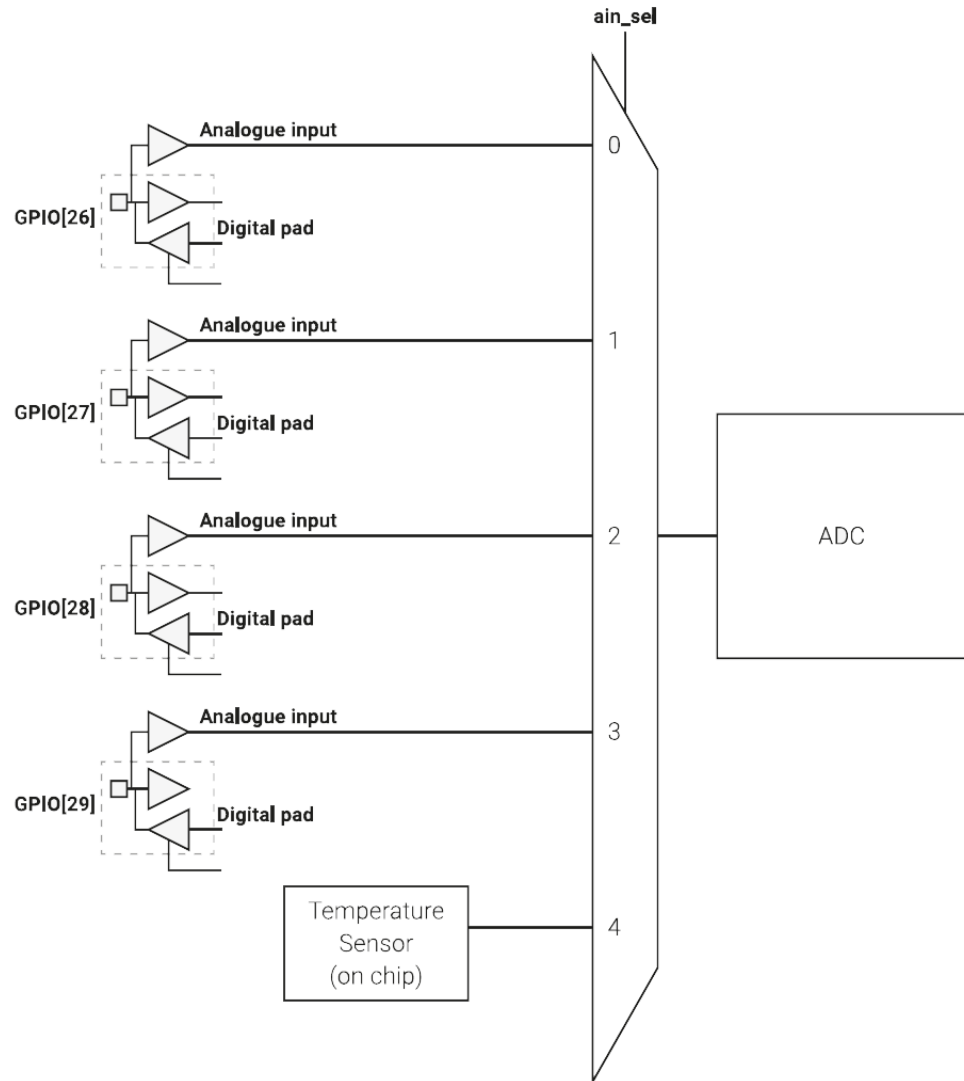
- 2x UART Controllers
- Separate 32x8 TX and 32x12 RX FIFOs
- Programmable baud rate generator, clocked by `clk_peri`
- Line break detection
- Programmable serial interface (5, 6, 7, or 8 bits) / 1 or 2 Stop bits
- Programmable hardware flow control
- Supports a maximum baud rate defined by `UARTCLK` (7.8 Mbaud at 125 MHz).
- DMA Support



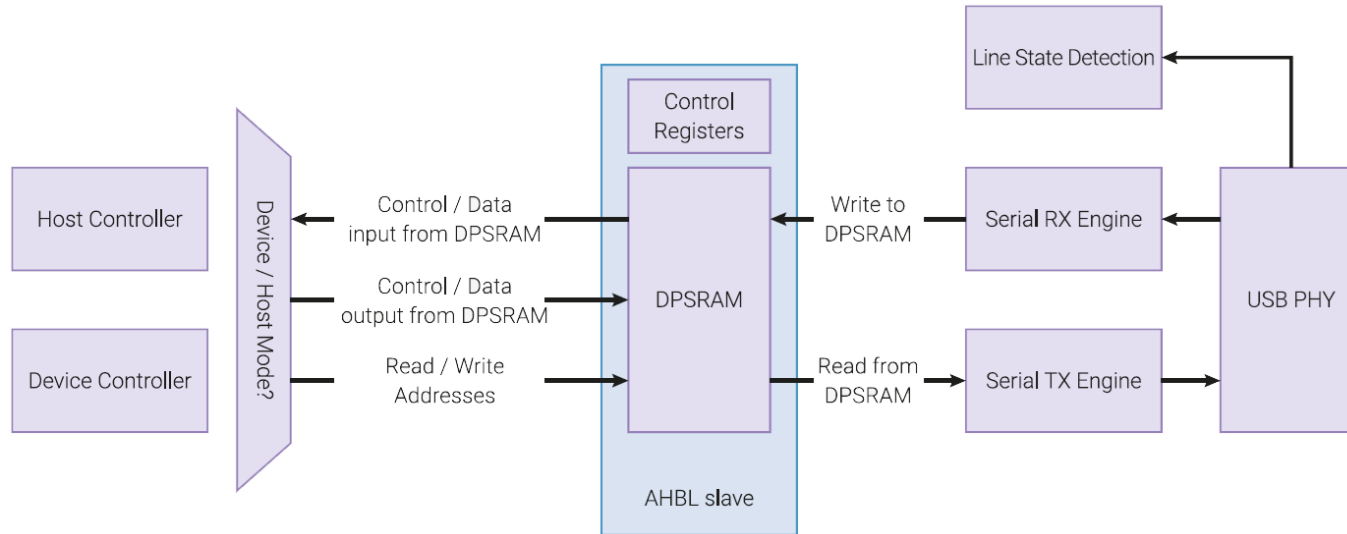
- Master or Slave (Default to Master mode)
- Standard mode, Fast mode or Fast mode plus
- Default slave address 0x55
- Supports 10-bit addressing in Master mode
- 16-element transmit buffer
- 16-element receive buffer
- DMA Support
- Interrupts Support



- Master or Slave modes
- Motorola SPI-compatible interface
- 8-location(16bit) TX and RX FIFOs
- Interrupt generation to service FIFOs
- DMA Support
- Programmable clock rate(SPI Clock)
- Programmable data size 4-16 bits



- SAR ADC
- Conversion is 500ks/s(using an independent 48 MHz clock)
- 12-bit with 9.2 ENOB
- Four or eight input mux (Built in Temperature sensor)
- One input dedicated to the internal temperature sensor
- 8 element receive sample FIFO
- Interrupt generation
- DMA Support



• When not used for USB function, DP and DM ports can be used as general GPIO ports.

- OTG Support (Device and Host Mode)
- Integrated PHY(USB 1.1-compliant PHY built in.)
- Dedicated memory(4KB Dual-Port SRAM)
- Device Mode
 - USB 2.0 - Full Speed(12Mb/s)
 - Supports up to 32 endpoints
- Host Mode
 - USB 2.0 - Full Speed (12Mb/s)
 - Low Speed (1.5Mb/s)



- **Provides a microsecond-resolution timebase for the system and can generate interrupts.**
- **Two independent timers**
 - TIMER 0 (Non-Secure world)
 - TIMER 1 (Secure world)
- **64-bit Counter**
 - Increments once per microsecond (1 MHz tick)
- **Alarms**
 - Four independent alarms per timer.
 - Generates an interrupt (IRQ) on a match.
- **Timebase Source (reference clock.)**

- **Watchdog Counter**

- The watchdog counter is loaded by the LOAD register (Down Counter)

- **Control Watchdog Reset Levels (POWMAN –WDSEL registers)**

- POWMAN_WATCHDOG(Chip-level Reset)
- PSM_WDSEL(System Reset)
- RESETS_WDSEL(Subsystem Reset)

- **Scratch Registers**

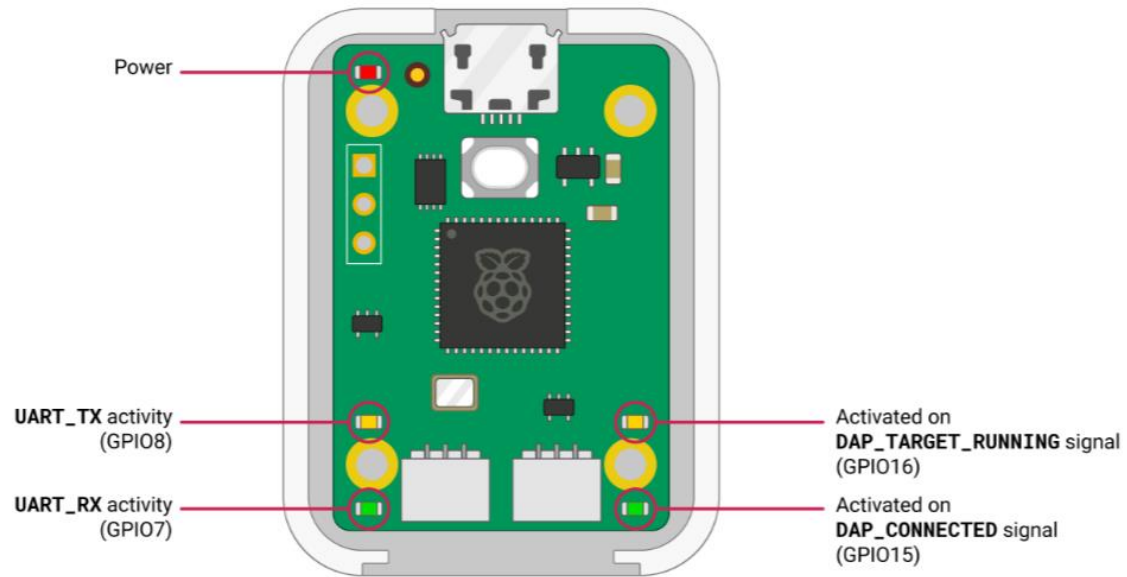
- SCRATCH0 ~ SCRATCH7 (32bit Registers)
- The values are not cleared even if a reset occurs due to the watchdog.
- Useful for storing system status information and analyzing causes.

- **HSTX is a peripheral that supports high-speed serial data transmission (High-Speed Serial Transmit).**
- **Data FIFO**
 - 8-entry, 32-bit-wide FIFO
- **HSTX Port (GPIO12 ~ GPIO19)**
 - 4 lanes(Clock and Data) Support
- **DMA Support (Minimizing CPU Load)**
 - HSTX works with Direct Memory Access (DMA), transferring data directly from memory without CPU intervention.
- **Application**
 - High-speed serial display interface(MIPI DSI, LVDS)

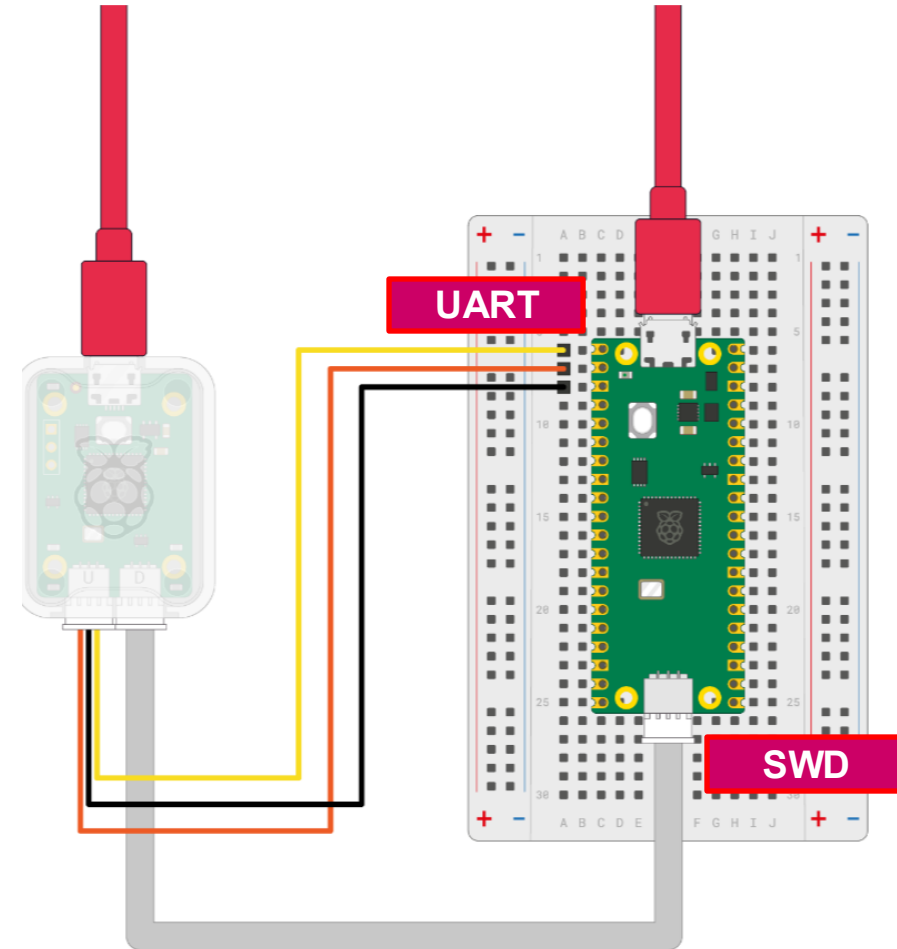
- **QSPI Memory interface, used for execute-in-place from external QSPI flash or PSRAM memory devices.**
- **External QSPI Device Support**
 - Up to two QSPI devices
 - Each device has separate chip selects, shared clock and data pins
- **Memory-Mapped Access**
 - Supports memory-mapped reads and writes
- **Transfer Format and Clock**
 - Supports Serial / Dual / Quad SPI
 - Maximum Clock speed(150MHz) up to clk_sys

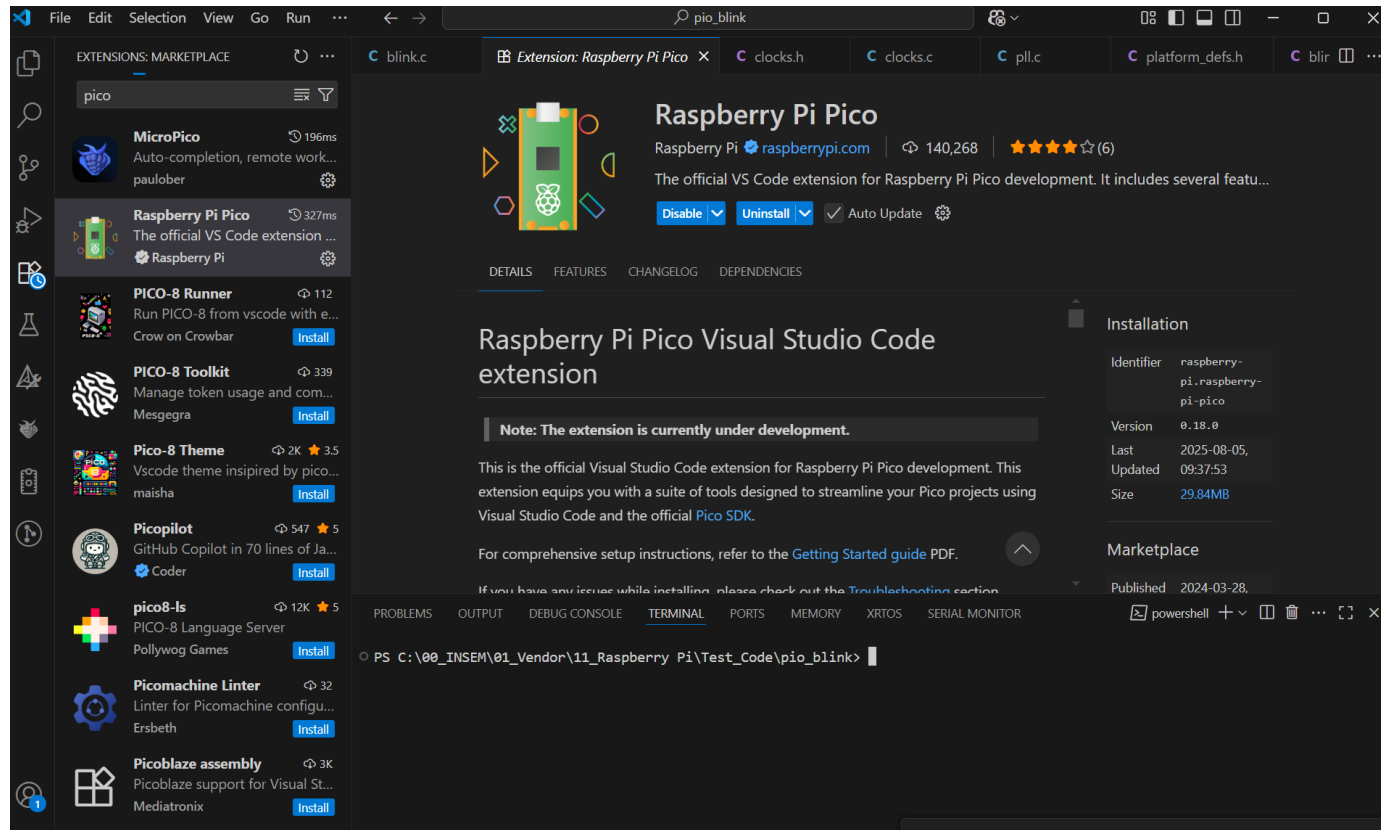
<p>OTP MEMORY</p> <p>8 kB</p> <p>4096 rows × 24 bits</p> <ul style="list-style-type: none"> • Preprogrammed data • Bootable software images
<p>ECC Mode: 16bit + 6bit Hamming ECC + 2bit bit reversal</p>

Item	Description
Size	8 kB (4096 × 24bit)
ECC	ECC mode : 16bit + 6bit Hamming ECC + 2bit bit reversal
Data	Device ID, Oscillator Trim Vaule, Secure Boot , Public Key, Flash Key, USB bootloader Config, Boot Image
Access	Boot ROM API, USB bootloader(PICOBOOT)
ETC	One Time Programming, OTP Access Key



Raspberry Pi Debug Probe





- Visual Studio Code
- Raspberry Pi Pico Extension
- MicroPico Visual Studio Code Extension(Pico-W-Go)
- C/C++ SDK and MicroPython support.
- PICOTOOL Support (CLI Base and Flash Download)
- Various example codes Support
- Middleware (RTOS) : FreeRTOS, Zephyr
- Middleware (USB) : TinyUSB (HID, CDC, MSC..)

INSEM's

Goal

Good Idea
Good Company

Basis

Gratitude
Enthusiasm
Detail

Motto

Ask, and it shall be given
Fulfill your duty
Do it now



Contact to : sales@insem.co.kr