EV 전력 변환 제어기의 신호레벨 HIL 솔루션, NI ITS

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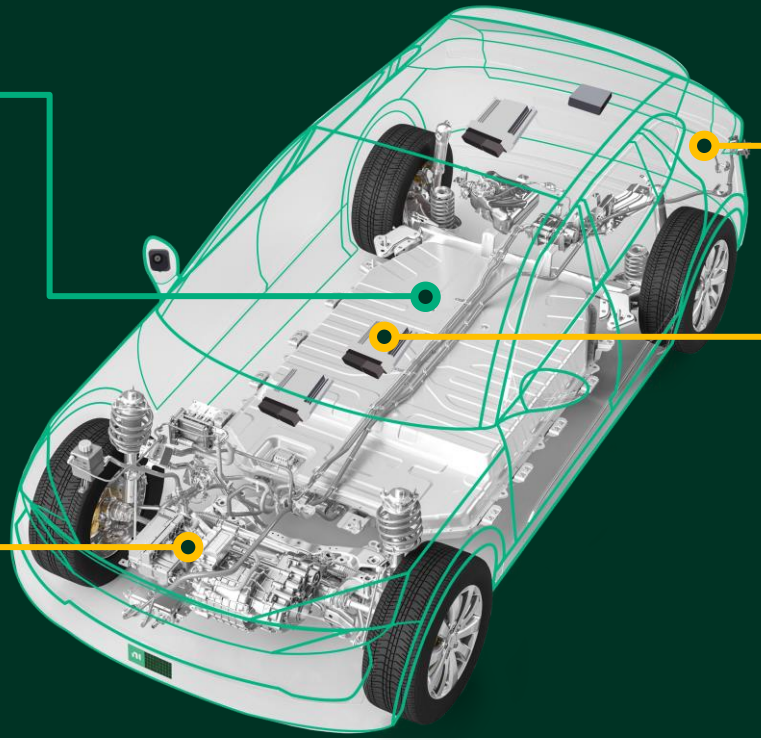
電子

Electronification
전장화
Electronic Circuit
전자회로
Signal
신호
Control
제어

電力

Electrification
전동화
Power Circuit
전력회로
Electromagnetic Force
전자기력
Motion
운동

EV Power Conversion is EVERYTHING but Battery

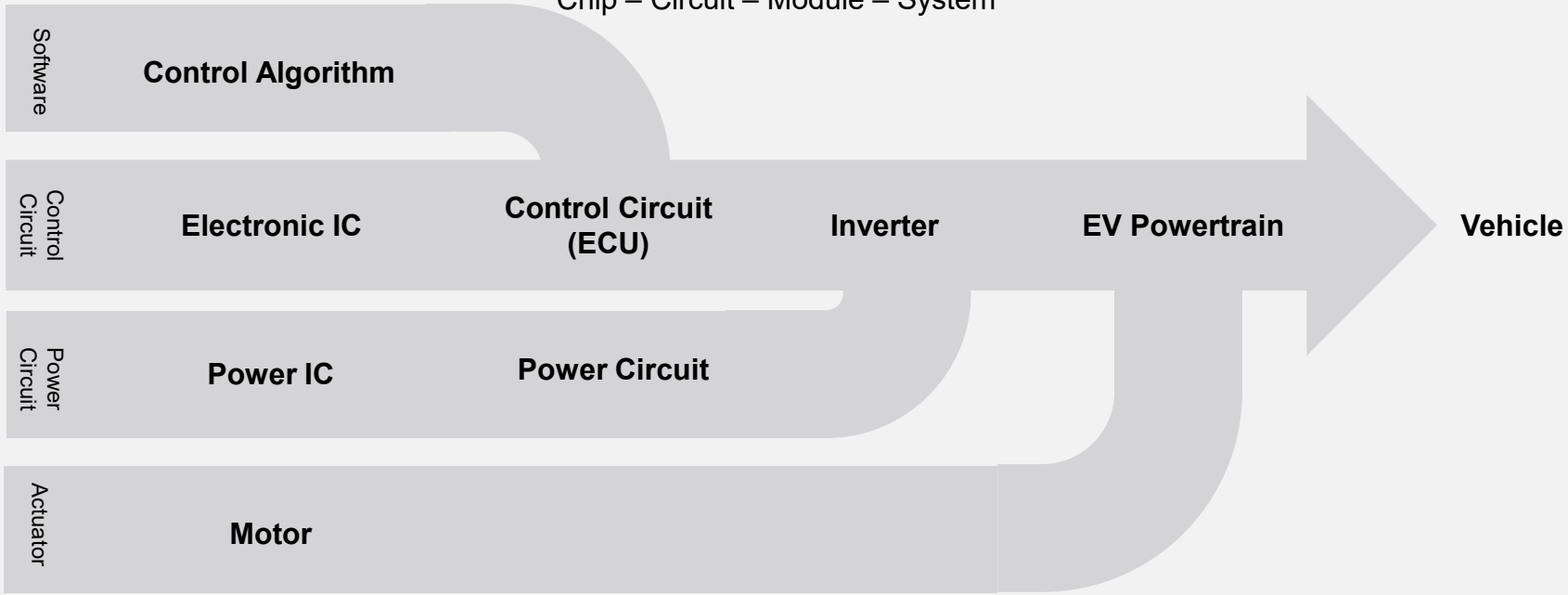


- EV Energy Storage
- EV Power Conversion

EMERSON

Example of EV Power Conversion Development Stage:

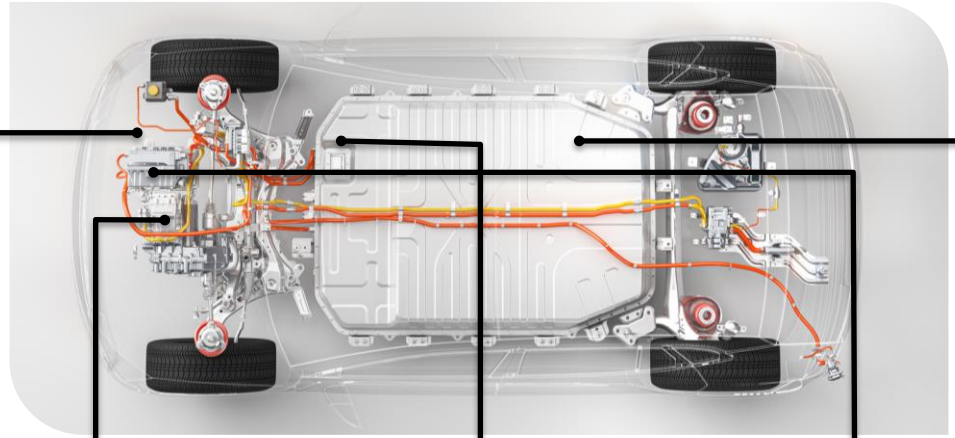
Chip – Circuit – Module – System



Software Test	Electronical / ECU Test	Electrical Power Test	Mechanical / Physical Test	Vehicle Test

NI Platform

What are the EV Power Conversion Components?



OBC

What it is?
Convert the AC from charging station to a DC signal.

Trend
Higher power
Faster Switching freq
Integration with inverter

Why
Faster charging
Lower cost design

Motor

What is it?
A machine that supplies motive power for the vehicle

Trend
Different designs (materials, geometries, # phases)

Why
Cost and performance
Material availability (rare earths)
Efficiency, 'limp home' features

BMS

What is it?
Monitors the battery and makes sure it is safe

Trend
Smaller, Wireless, adapt to new battery chemistries

Why
Cost, efficiency, eliminate cables and noise

Inverter

What is it?
Converts the DC from the battery to AC to spin the motor

Trend
SiC, higher power/switching freq, Varied control algos

Why
Efficiency, smaller/lighter
Regen braking (single petal driving), extend range and life

Battery

What is it?
Where the energy of the vehicle is stored

Trend
lower $/kwh
Higher voltages

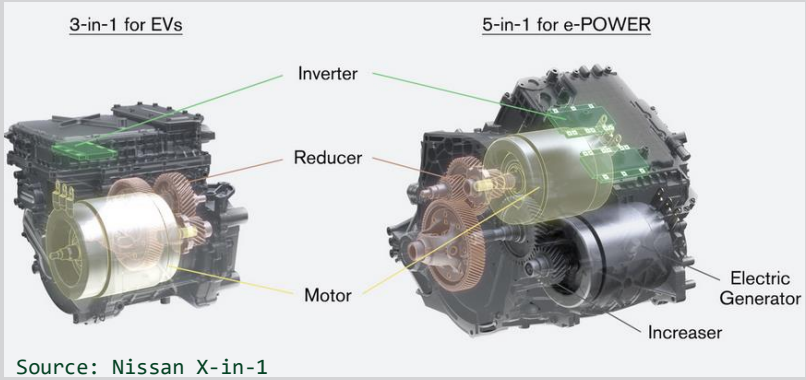
Why
Achieve EV market cost targets
Efficiency, decrease charge times, increase performance

Market Trend and Challenges

- Market Trend
  - X-in-1
  - Multi-motor
  - Dual Inverter with Open Winding Motor
  - Resonant Converter
- Accordance challenges on ECU

Further commonize and modularize core EV powertrain components

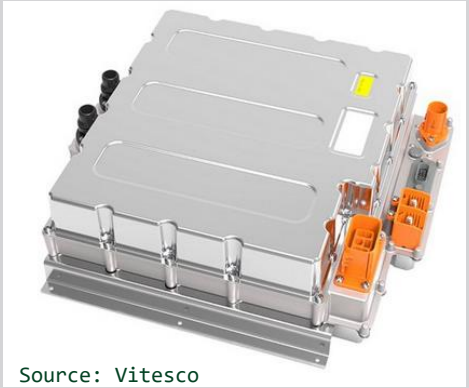
Nissan X-in-1



Source: Nissan X-in-1

The modularization of the X-in-1 will result in improved performance, smaller size, and better vibration control through integration

Vitesco Onebox

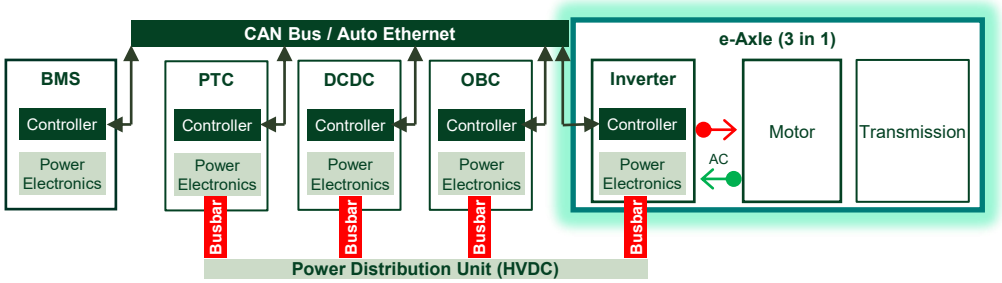


Source: Vitesco

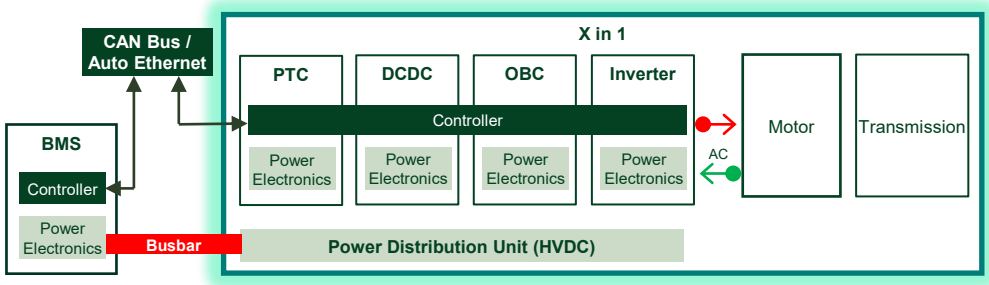
Renault and Vitesco announced the joint development of One Box – integrated DCDC, OBC, and Inverter

- Some Inverter HIL test rings require emulations for other power electronics and controllers tied to OBC and DCDC due to the integration of those components into one unit
- Some OEMs are also driving modular and integrated X-in-1 architectures that require flexibility to adopt additional plant models for Inverter validation test rigs.

X-in-1 – Next-Generation xEV Powertrain



Distributed 3-in-1 plus Controllers with PEs
To
Integrated X-in-1



Market Requirements

Smaller Size
Light Weight
Lower Cost
Higher Efficiency

X-in-1 Benefits

Integration of power electronics and ECUs
Reduction of HV harnesses and connectors
Reduction of components and VCOM
Integrated WBG PE for higher performance

Test Implications

PE emulation for an integrated system
More IO channels for an integrated system
Increased Test Coverage for SW integration
High-frequency emulation for SiC and GaN

Benefits of NI

Scale and Leverage PE emulation options
Select and Update IO from Unrivaled Portfolio
Automate Tests with Ready-to-Run HIL SW
Maximize FPGA's Computational Performance

Multi-Motor ELECTRIC CARS get Popular

Toyota

RAV4 E-Four Hybrid combines its Atkinson cycle 4-cylinder petrol engine works in tandem with two electric motors.

Source: Tesla

Lucid

Lucid Air Dream Edition's quad-motor powertrain can churn out 1,111 hp for a top speed of 168 mph.

Source: Auto

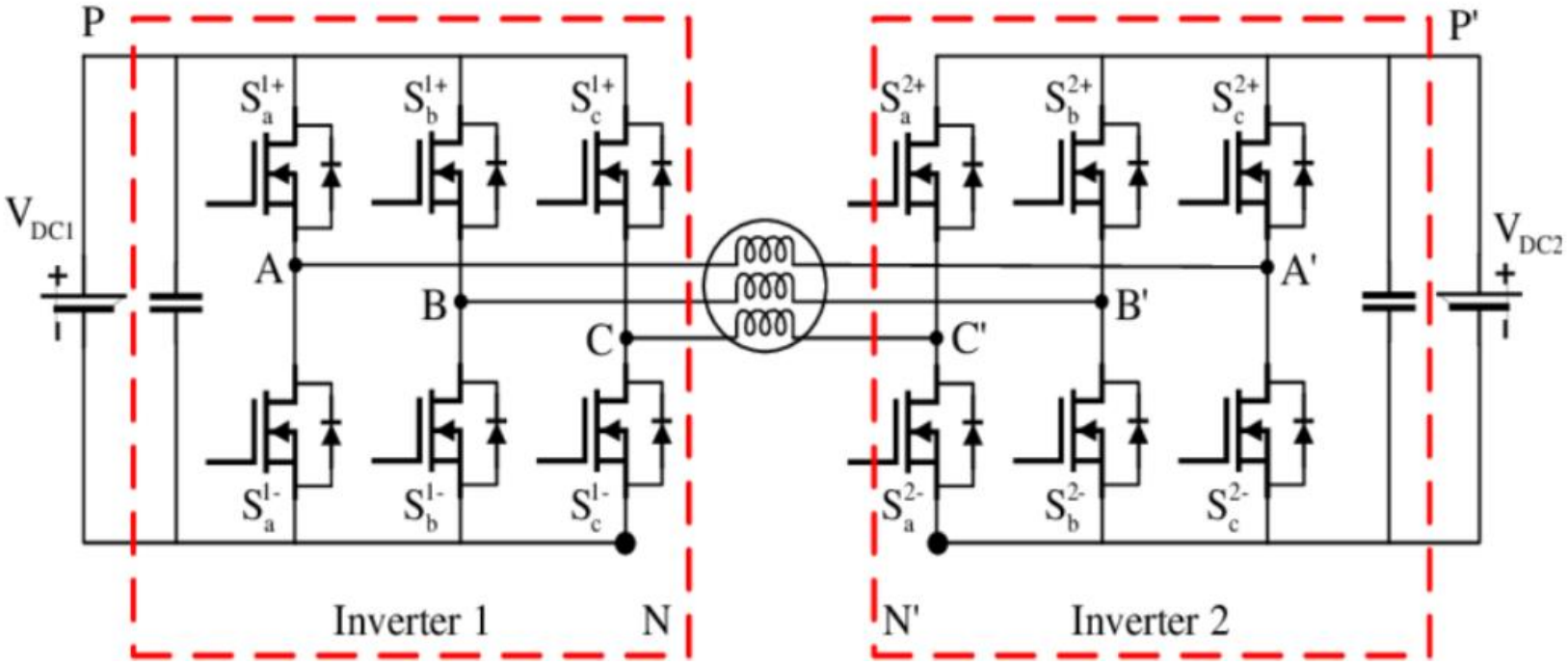
Tesla

Model S Plaid maintains 1,000 HP all the way to 200 mph with Tri-motor all-Wheel Drive

Source: Lucid Motor

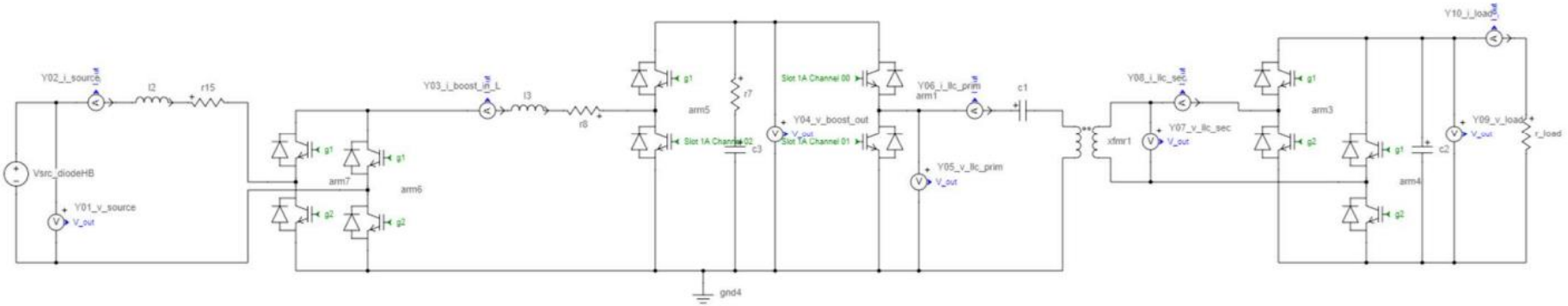
Dual Inverter and open winding motors

Can avoid the use of rare metals and also connect to both 400V & 800V charging stations



Resonant Converter

- Resonant Converters becoming the standard for OBC applications
- Also, GaN is starting to get considered
- Why? Faster switching means smaller and better efficiency



Voltage Source Converter vs. Resonant Converter

	Voltage Source Converter (VSC)	Resonant Converter
Control Strategy	Pulse Width (amplitude control)	Switching Frequency (Frequency controlled)
Gating Signal Frequency	1kHz – 100kHz	100kHz – 1MHz
Simulation Challenges	Getting the accurate amplitude applied	Getting the right frequency applied to avoid aliasing and ripple effects
Solution	Fast model loop rate (100x switching frequency)	Fast model loop rate Very high-resolution capture of switching events and compensation in the model

How EVPC trend affects ECU development?

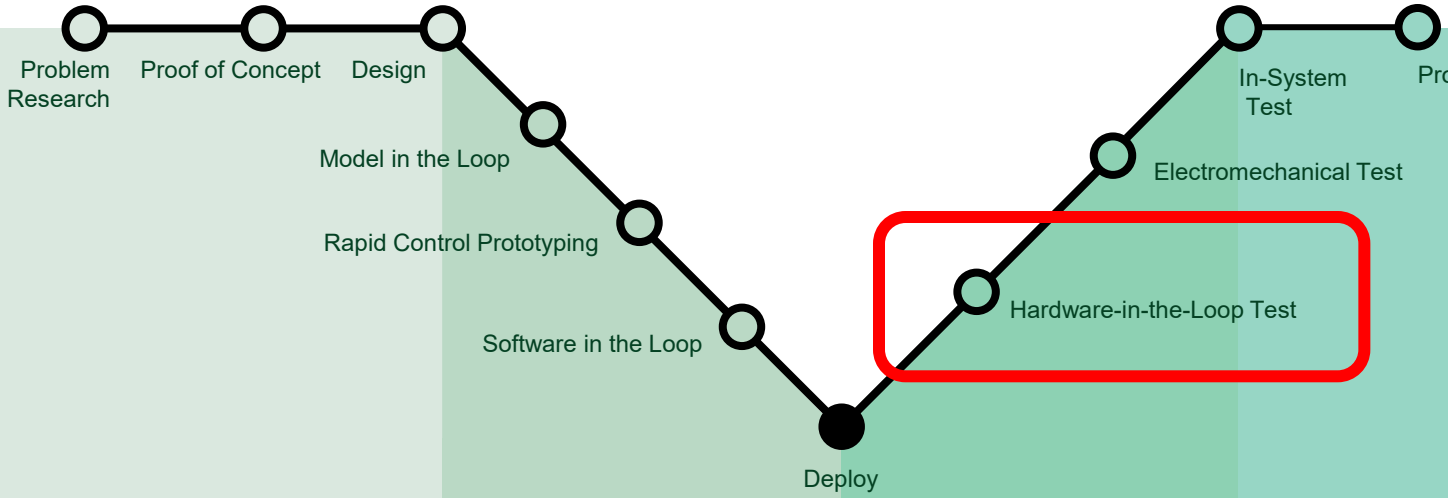
- EV Power Converting circuit is getting faster and complex
  - New materials and technologies are applied
  - Multiple functions are integrated

- New missions on ECU development
  - To control faster circuit
  - To control complex circuit

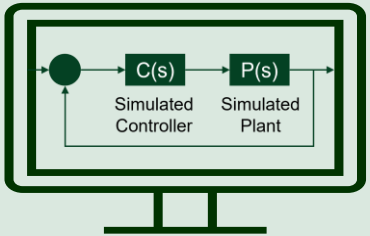
ECU Validation using HIL

- V diagram and HIL
- NI Platform for HIL application

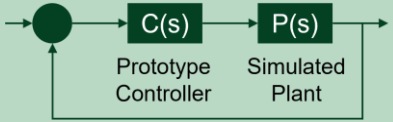
Testing Early and Often Before Production Test



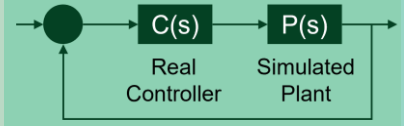
Design



Prototype

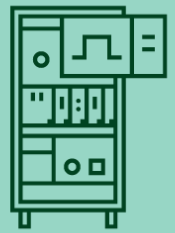


Software and Controller Test

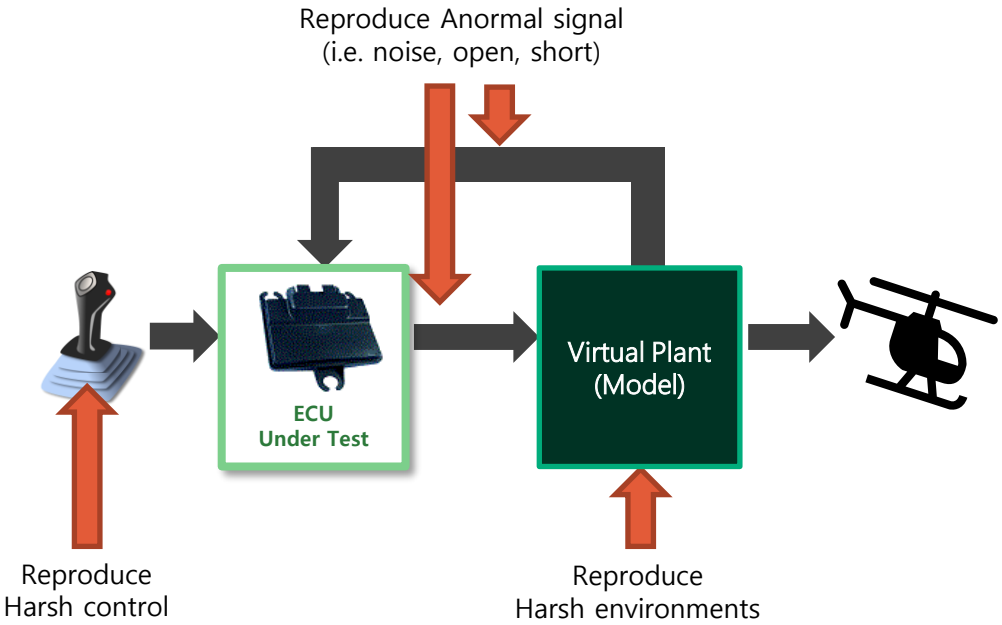


Physical Test

Real controller
+
Real plant



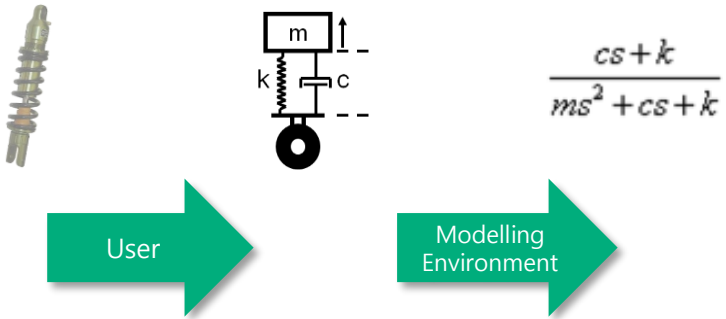
Hardware-In-the-Loop



1. Validate control in general behavior
2. Validation handling in abnormal behavior
   - A. Easy to reproduce harsh condition
     - Quantitative
     - Save time and cost
   - B. In case of control failure happens
     - Safety
     - No damage, No cost

What is Model?

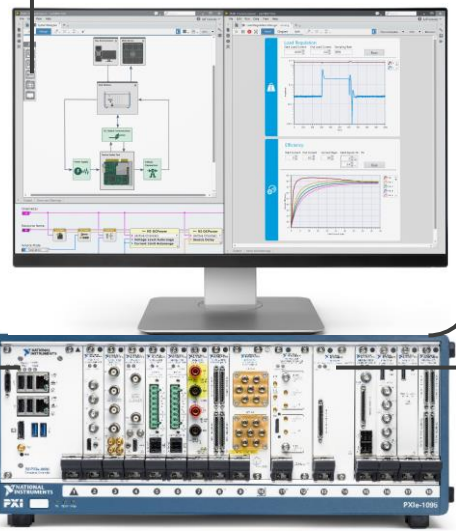
- Sample Model — Shock Absorber



Anatomy of a PXI Test and Measurement System

Software
Test Management and Code Development

Timing and Synchronization
PXI Chassis



Computer
PXI Embedded Controller

Instrumentation
PXI Modules

NI VeriStand

Accelerate Embedded Software Testing

Ready to Run Software for XIL

Create, deploy, and leverage closed loop control on Linux RT for X-in-the-loop systems.

Quickly Configure Systems

Configure I/O channels, alarming, data logging, stimulus generation, fault insertion, user interfaces and bus communications.

Model Integration

Integrate plant and controller models from Simulink and other 3rd party modeling environments adhering to FMI standard.

Test Automation

Use test sequences and scripting to configure, orchestrate systems through .NET APIs, Python, and ASAM XIL and integrate with CI/CD workflows.

Customizability

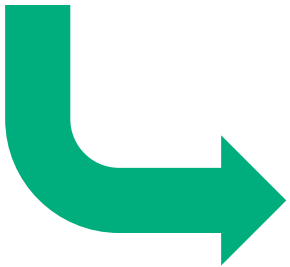
Adapt to changing requirements with an extensible software environment. Build plug-ins for 3rd party hardware and additional measurement types.

Unique challenges on EVPC ECU Validation

- Unique Process of EVPC ECU Validation
- FPGA technique to overcome challenge
- NI FPGA platform

Challenge on EVPC HIL system by market trend

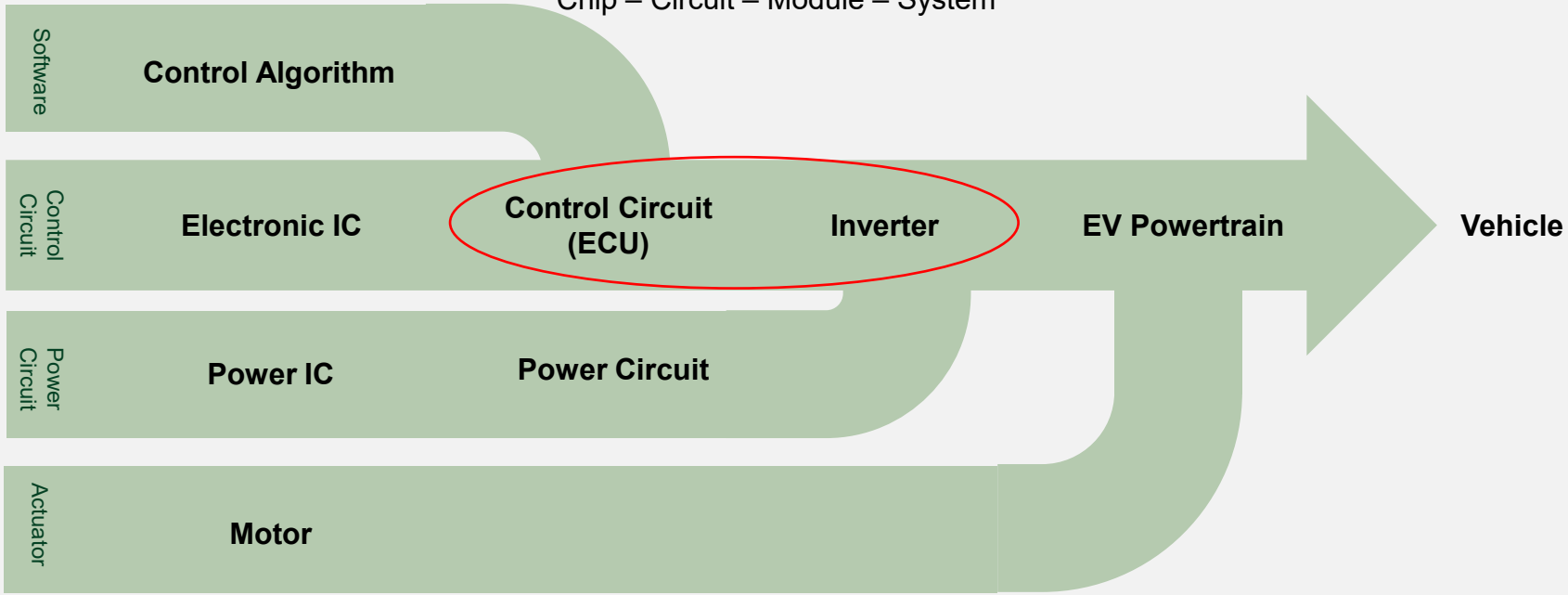
- New missions on ECU development
  - To control faster circuit
  - To control complex circuit



- New missions on ECU validation (HIL)
  - To simulate faster circuit
  - To simulate complex circuit

Example of EV Power Conversion Development Stage:

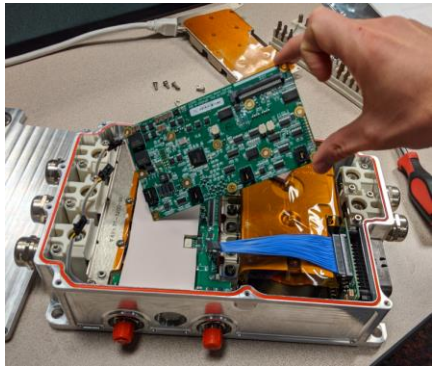
Chip – Circuit – Module – System

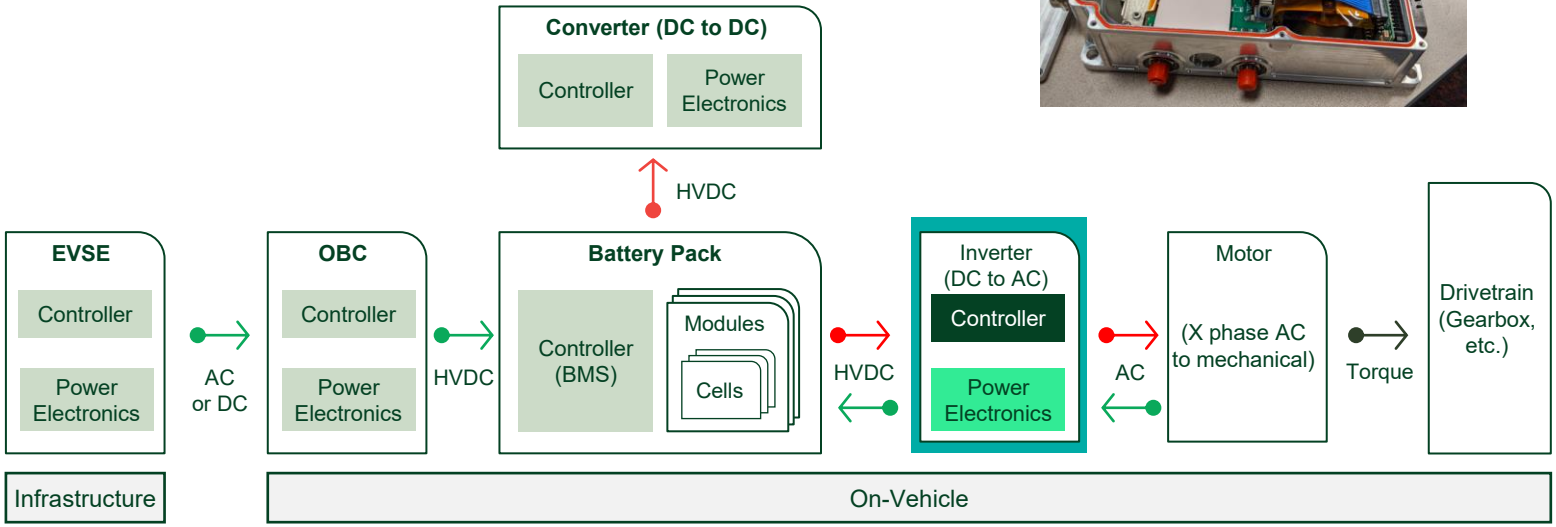


Software Test	Electronical / ECU Test	Electrical Power Test	Mechanical / Physical Test	Vehicle Test

NI Platform

EV Traction Inverter





Increasing COST, RISK, TIME TO FIX and EFFORT

Test Approaches Along the Design Lifecycle

MIL | SIL ⟷ FIELD

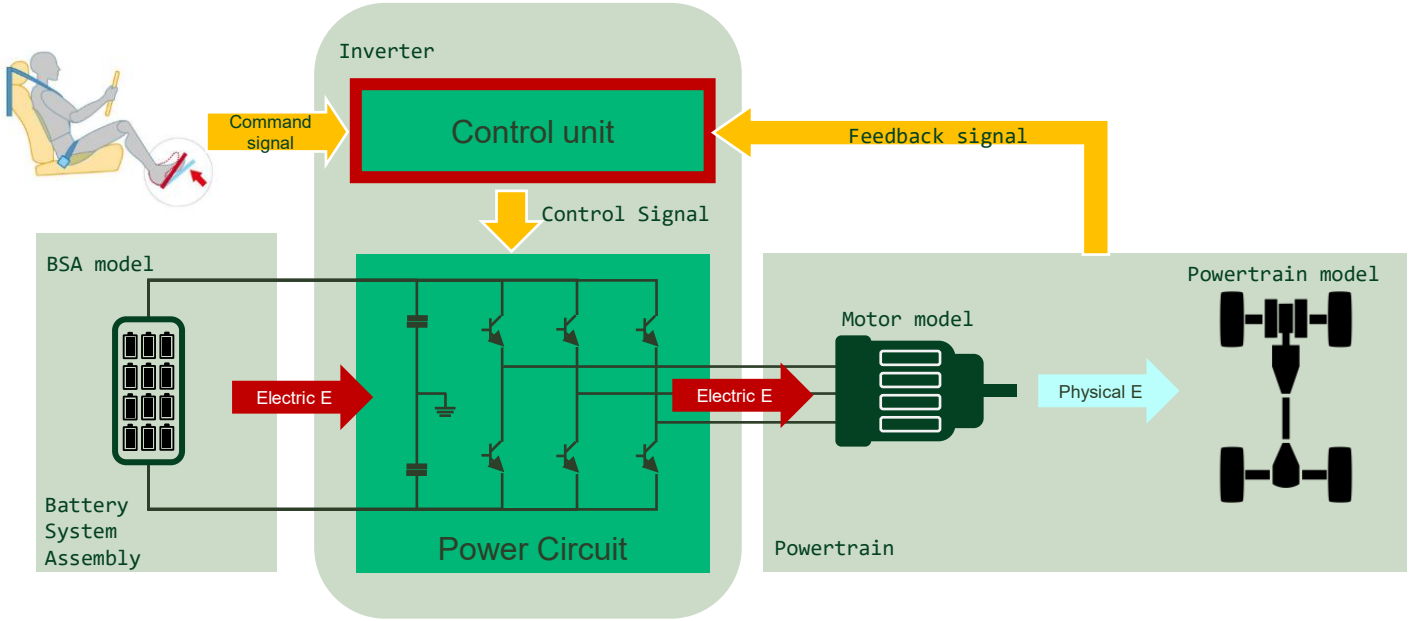
Lower cost, faster, less dependencies, but lower fidelity and introduces simulation/emulation complexity

REALISM →

← FLEXIBILITY

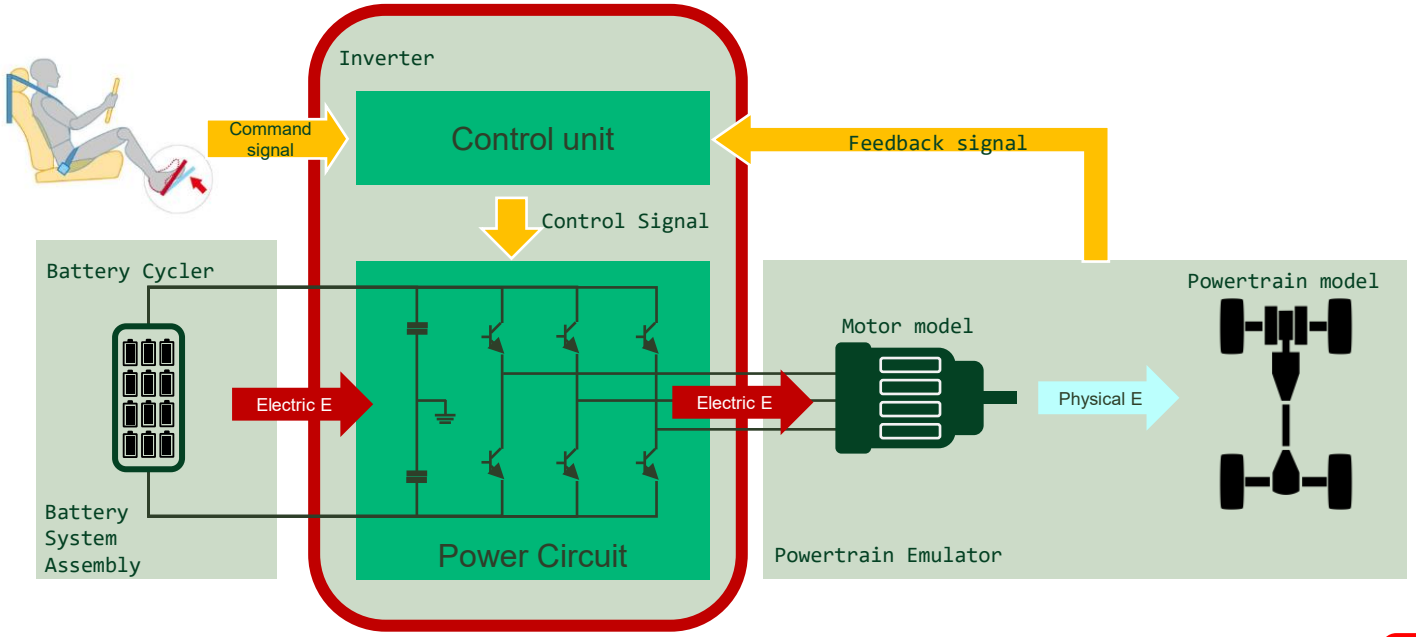
Higher fidelity but more expensive and time consuming

Inverter HIL: Signal level



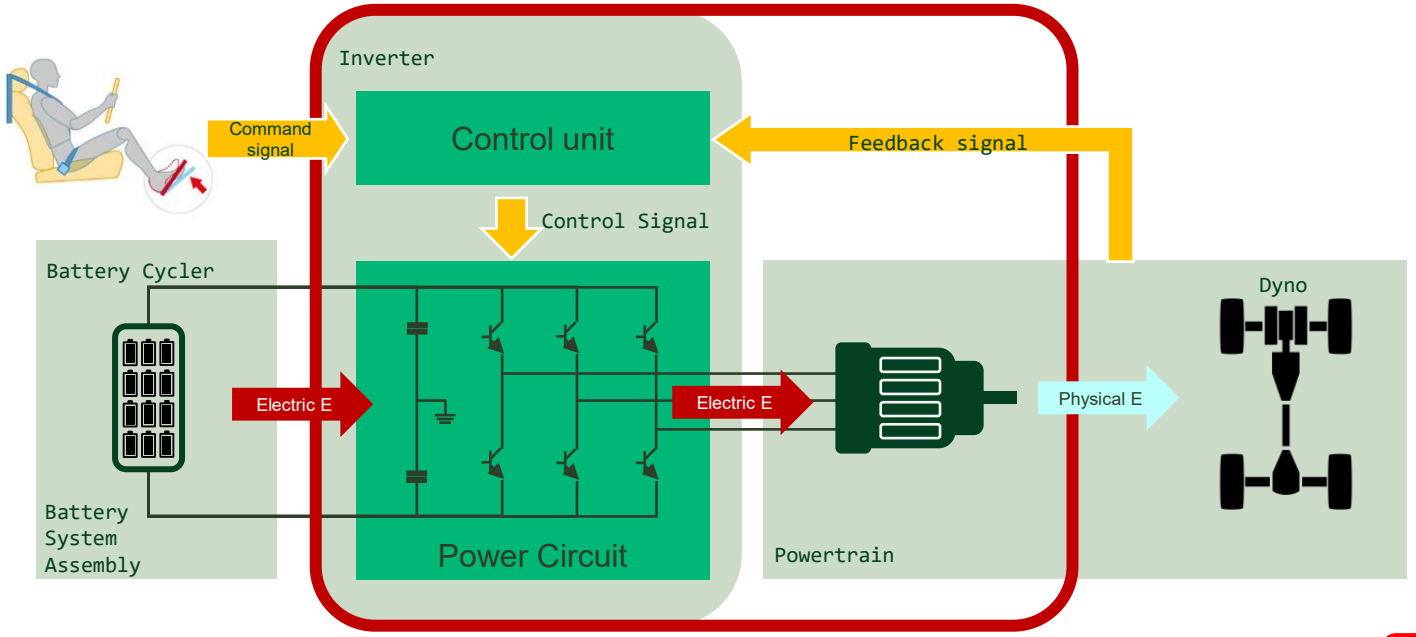
Real

Inverter HIL: Power level



Real

Inverter Test Cell: eDyno

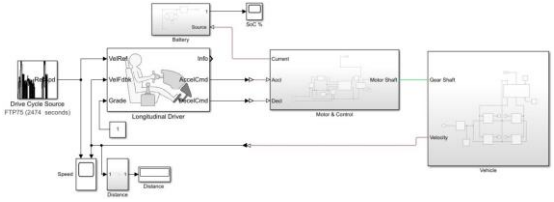


Real

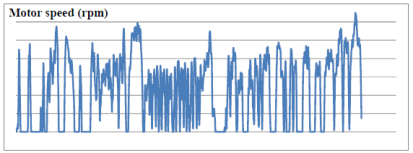
Emulator Based Testing

Real-Time and FPGA-Based Simulation

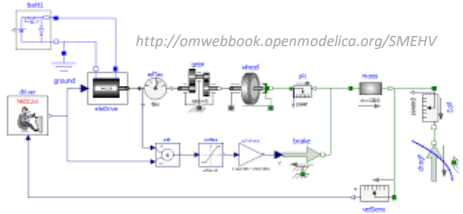
Vehicle Models



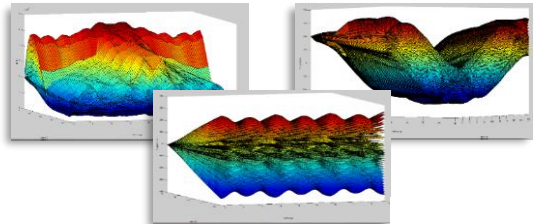
Drive Cycles



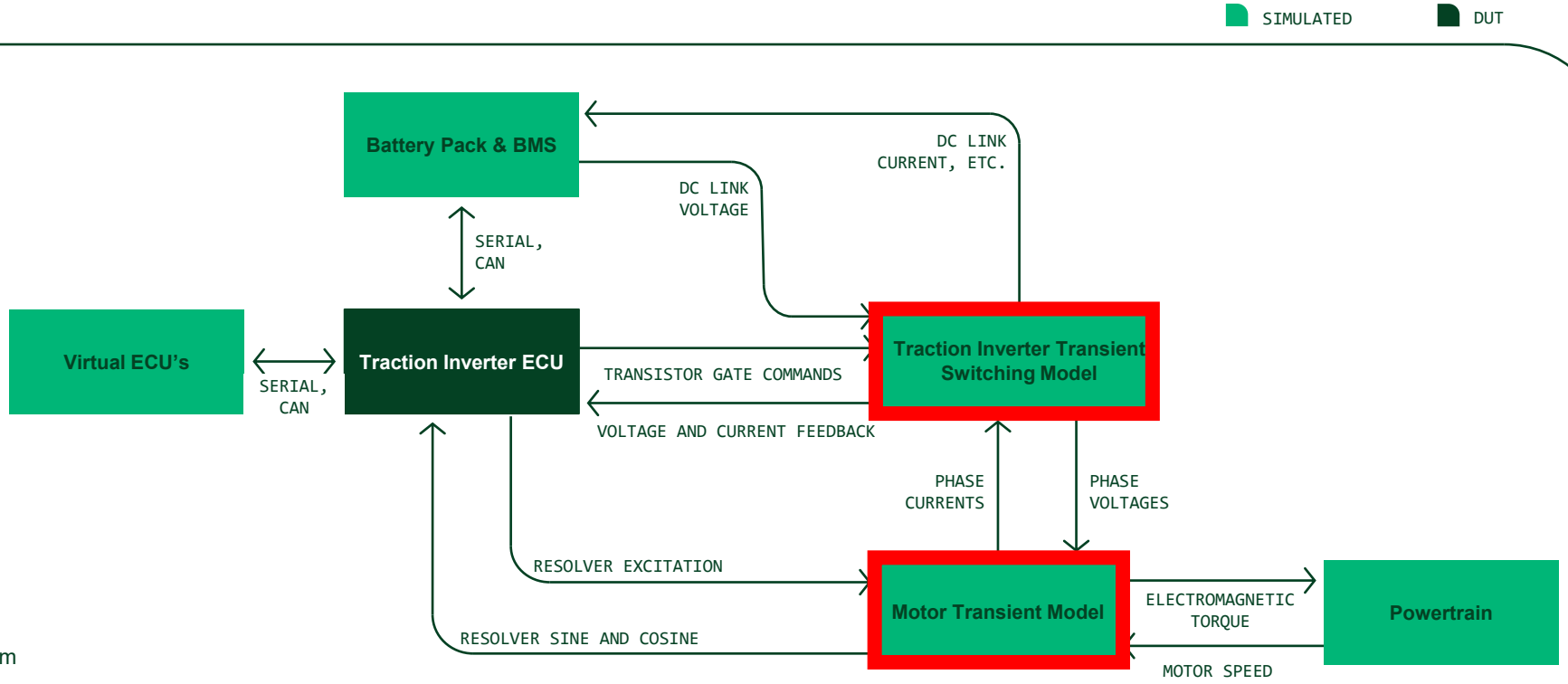
Mechanical Components



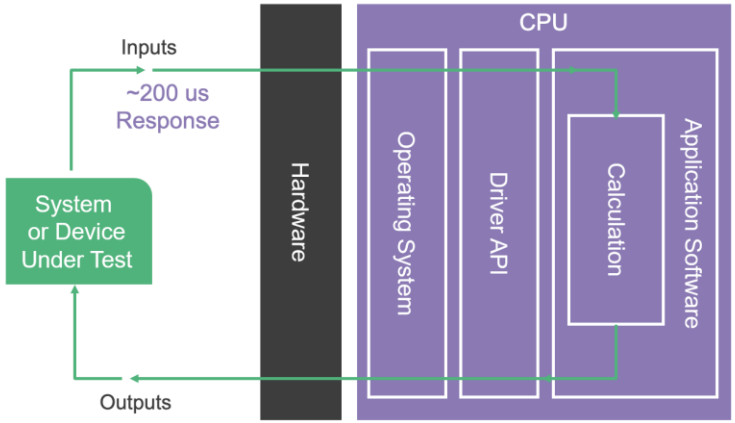
Motor Models



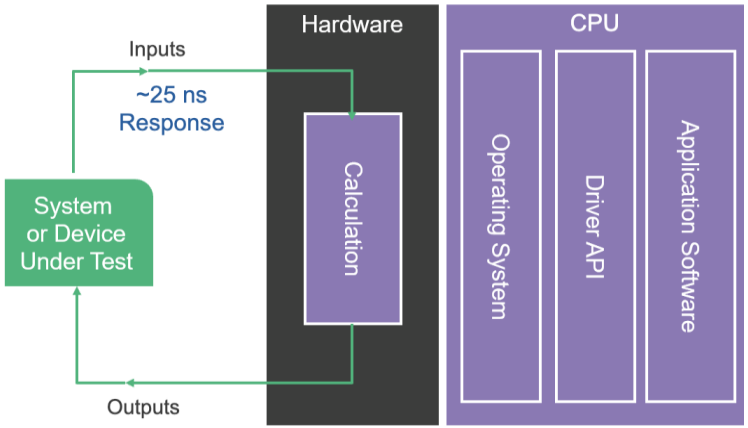
NI ITS Traction Inverter HIL Test



Choosing the Right Approach

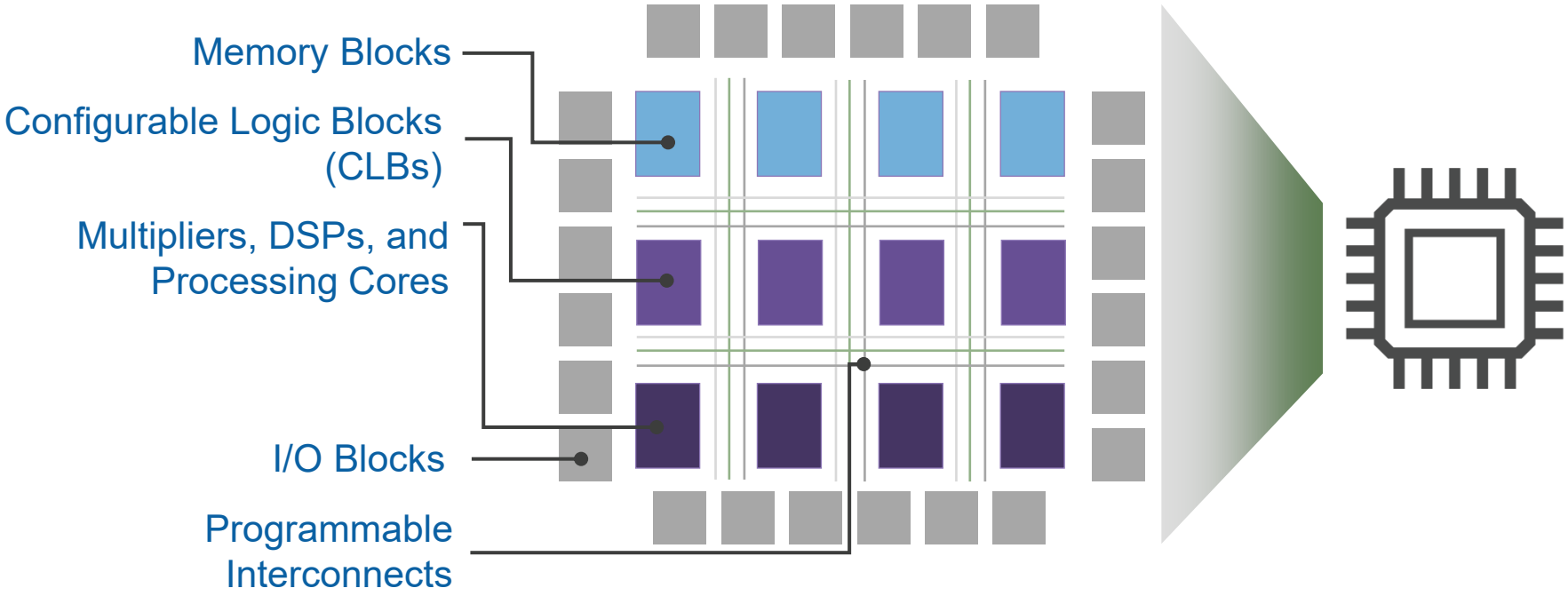


Processor Based Approach



FPGA Based Approach

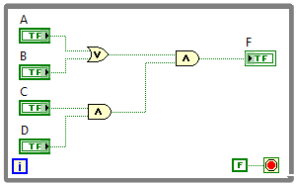
What is an FPGA?



- FPGA configured with user-generated binary file (.bin, .lvbitx)
  1. VHDL
  2. Verilog
  3. LabVIEW FPGA

Compilation Process

LabVIEW FPGA Code



Compile VHDL through Xilinx

```
-- Then we keep track of what the digital input was on the previous
-- clock cycle by inserting another flip flop
PreviousDigitalInputFF:
process( aReset, Clk )
begin
  if aReset then
    cPrevDigitalInput <= false;
  elsif rising_edge(Clk) then
    cPrevDigitalInput <= cDigitalInput;
  end if;
end process PreviousDigitalInputFF;

-- Then we have a little combinatorial logic to detect a rising edge
cRisingEdgeDetected <= cDigitalInput and not cPrevDigitalInput;

-- And finally we have a register that increments when that rising
-- edge is detected.
```

FPGA Logic Implementation

Translation
VHDL Generation

Optimization
Analyze Logic Reduction

Synthesis
Place and Route Timing Verification

Bit Stream Generation
Download and Run

2 questions on FPGA product

- Hardware aspect
  - Capacity
  - Signal I/O performance
  - Data throughput
- Software aspect
  - Efficiency
  - Accessibility
  - Flexibility

PXIe-7890/1- Signal Level FAM

Features

- 8/16 differential channel AI at 2 MS/s and 8/16 single-ended channel AO up to 2 MS/s
- 16/32 single-ended low-latency AO channels up to 4 MS/s per channel with calibrated latency of 188 nsec
- 64 single-ended DIO channels

Capabilities

- 400kHz PWM
- Simulate up to 4 motors on one FPGA, or 144 switches
- Capture gate signals at 2.5ns for sHIL+OBC
- Upload full JMAG, Maxwell motor models

Key Applications

- EV Inverter Test
  - 4 simultaneous motor models
- Broadbase
  - Large FPGA, low latency AO

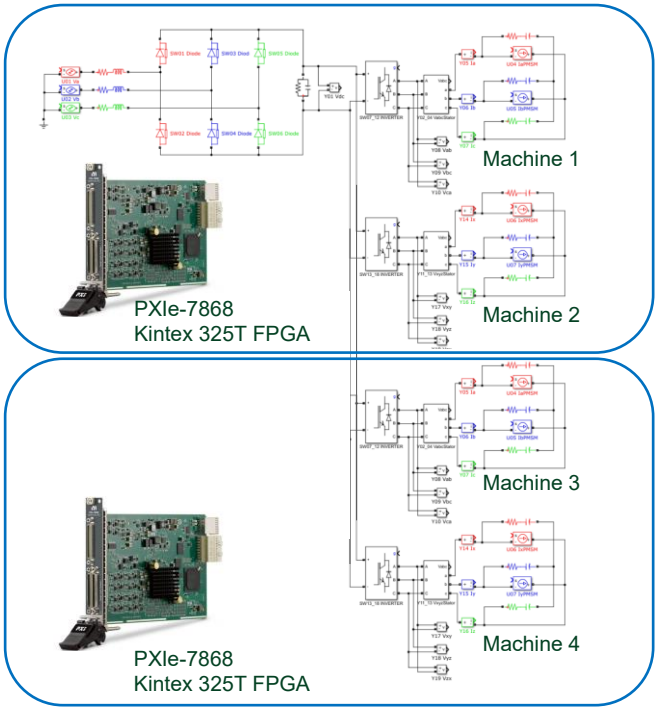
  enable complex control models

FPGA Backend Specifications

- Xilinx Kintex Ultrascale FPGA
  - KU060, 60 DMA
- 4 GB onboard DRAM
  - 2 x 2 GB Banks, 8.5 GB/s Bandwidth / bank
- PCIe Gen. 3 x 8 interface
- 64 single-ended DIO channels
- High-speed serial (2 QSFP+ Connector, up to 5 Gb/s)

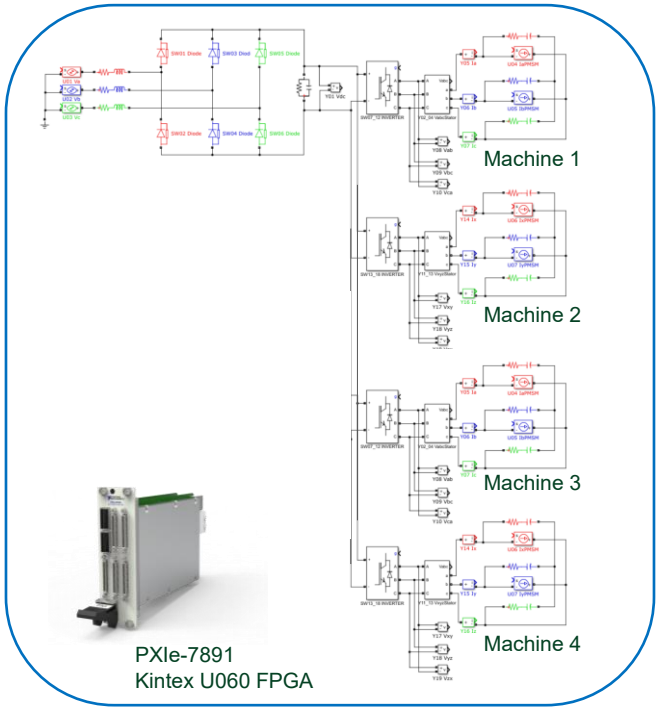
New PXIe-7891 – Quad-motor support on single FPGA

Today



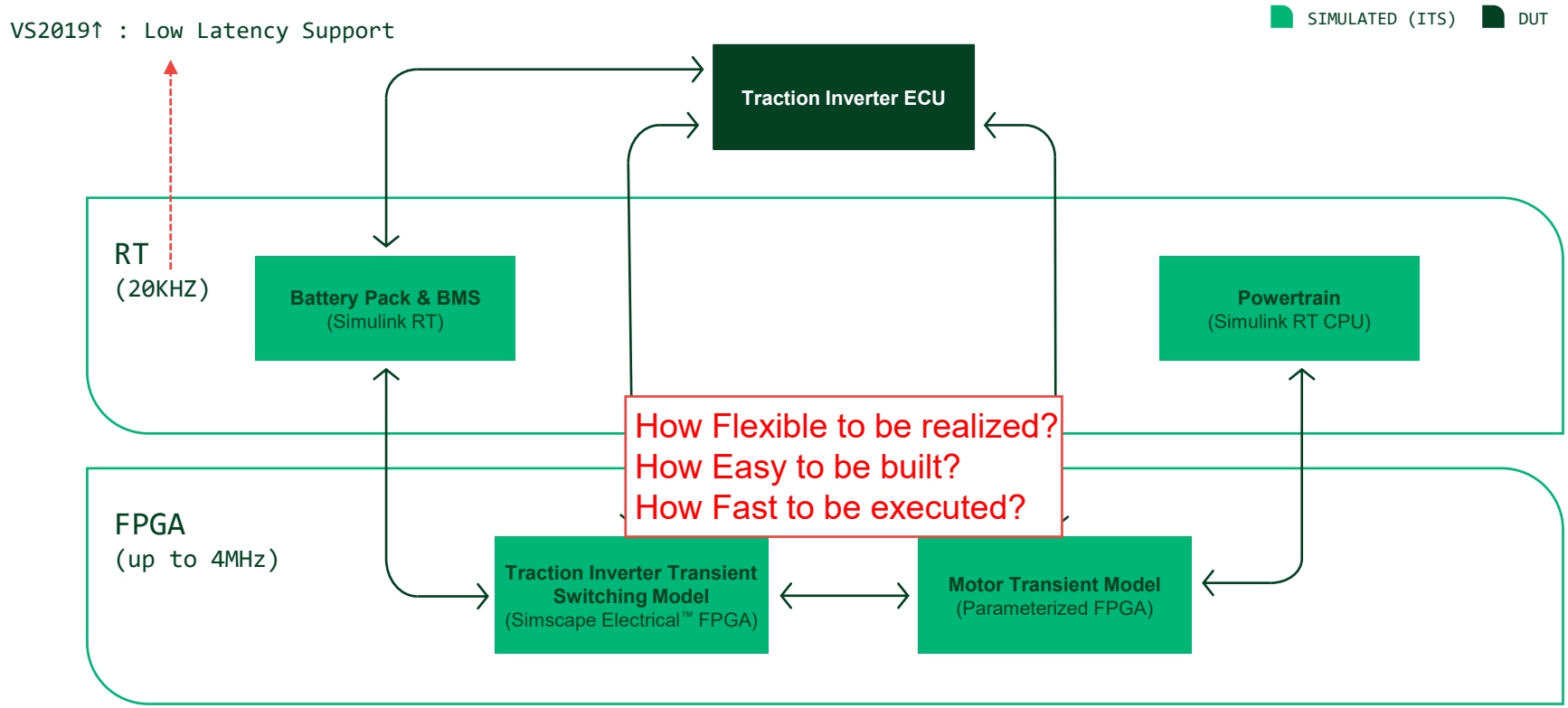
- Split a model into two parts and validate them (>10hr)
- Expect communication latency between FPGA (300 ~ 700 nsec)

With Kintex UltraScale FPGA



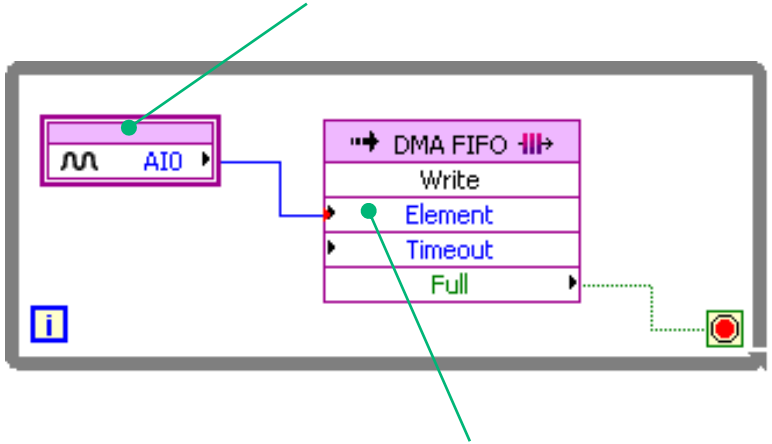
- Can deploy the entire model onto one FPGA (<1hr)
- No latency between machines

Model Co-simulation

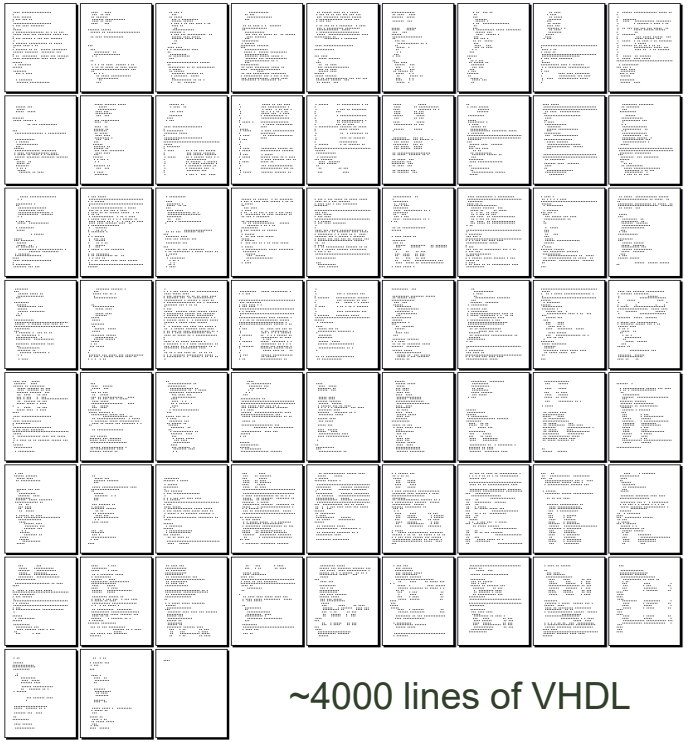


Abstraction of Hardware Complexities

Acquire analog data point-by-point



Directly transfer analog data to processor memory via FIFO for data logging, display, etc.



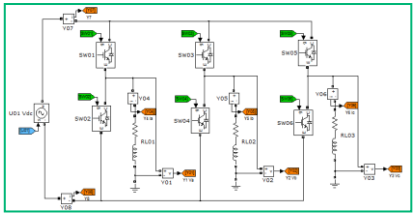
~4000 lines of VHDL

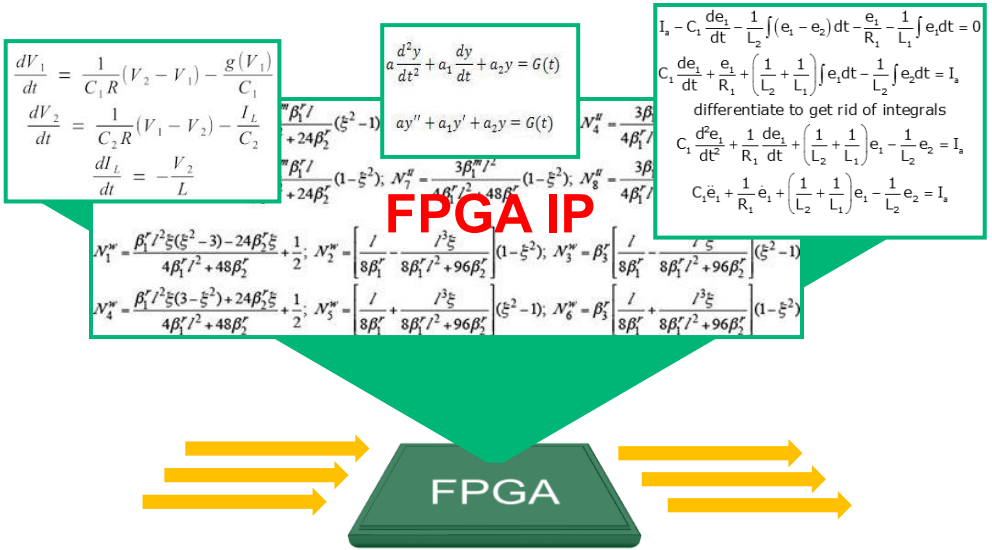
→ Able to expect integrator to apply feedback faster

SIMULATION OF POWER ELECTRONICS

FPGA-based real-time simulation is effective for meeting timing requirements

- **But**: implementing differential equations on FPGA is tricky and requires advanced FPGA programming skills





Collaborations to implement circuit model on FPGA

- With OPAL-RT (eHS Solver)
- With Mathworks (Simulink)

Partnership of NI & OPAL-RT

Ash Razdan, Director, Corporate Development, NI
Jean Bélanger, CEO & CTO, OPAL-RT TECHNOLOGIES

News

May 17, 2019

NI and OPAL-RT Sign Strategic Agreement to Work Together to Advance Electric Vehicle Testing Through Hardware-in-the-Loop Simulation

[MONTREAL, May17th 2019] NI (Nasdaq: NATI), the provider of a software-defined platform that helps accelerate the development and performance of automated test and automated measurement systems, and OPAL-RT announced today they have signed a strategic agreement to accelerate the development of hardware-in-the-loop (HIL) simulation technologies for the automotive market, with a focus on testing electric vehicles.

OPAL-RT TECHNOLOGIES

[MONTREAL, May 17th 2019] – NI (Nasdaq: NATI), the provider of a software-defined platform that helps accelerate the development and performance of automated test and automated measurement systems, and OPAL-RT announced today they have signed a strategic agreement to accelerate the development of hardware-in-the-loop (HIL) simulation technologies for the automotive market, with a focus on testing electric vehicles.

The agreement will establish a deeper partnership between the two companies with years of experience developing innovative HIL solutions. NI and OPAL-RT plan to deliver powerful FPGA-based solutions that combine NI's flexible and open test platform with OPAL-RT's expertise in high-fidelity power electronics modeling and deployment. NI and OPAL-RT's combined technologies are designed to help customers increase productivity and drive rapid innovation through an efficient workflow built on an open and customizable platform.

"Through this strategic partnership, we will strive to solidify the workflow for test departments to validate today's EV powertrain while we deliver a flexible approach to meet the rapidly changing and high-performance needs of the future," said Chad Chesney, vice president and general manager of the NI Transportation Business. "We believe our combined strengths can provide customers with an innovative test solution that enhances their flexibility and helps them build advanced test competencies on a common platform to generate a competitive advantage for their

Overview Motor & Drives Simulation

Complete motor library

- Permanent Magnet Synchronous Machines (IPM, BLDC, SPM)
- Induction Machines (DFIG, DFIM, SC)
- Switched Reluctance Machines (SRM)

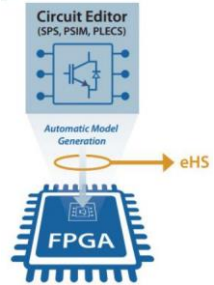
High Performance

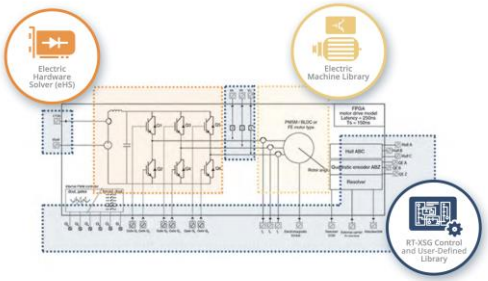
- Down to 100 ns time step
- Up to 144 switches per FPGA – no decoupling
- Up to 400 kHz switching frequency

Efficient Workflow

- Scenario Feature (automate up to hundreds of scenarios)
- Flexible modelling environment
  - SimScape Power Systems, Simulink

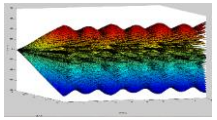
FPGA Simulation solver



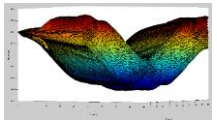


Import of spatial harmonic tables (FEA)

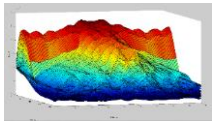
- Torque, Flux & Inductance Table

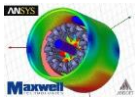


JMAG



MotorSolve BLDC



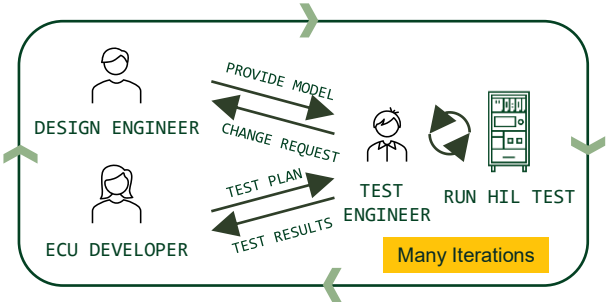


eHS Workflow brings 10x productivity gain

Challenge: Many iterations with multiple hours to set up machine emulation on FPGA for the first test; MIL models do not work on FPGA

Solution: Deploy Simscape circuit models on FPGA without any bitstream generation using OPAL-RT eHS solver, NI VeriStand, and NI FPGA target

Value: Streamline MIL to HIL workflow to run first test earlier for new test plan



APPLICATION: BOOST CONVERTER + INVERTER + EMOTOR

Typical Workflow

Create/Edit Circuit Model (MIL) — Simscape → Solve Circuit Equation — circuit equation → Create HDL Implementation Model — Simulink → Generate FPGA Bit File & Manual Edit — HDL → FPGA Deployment → Validate Model Behavior → Operationalize HIL Test

CALIBRATE MODEL BEHAVIOR

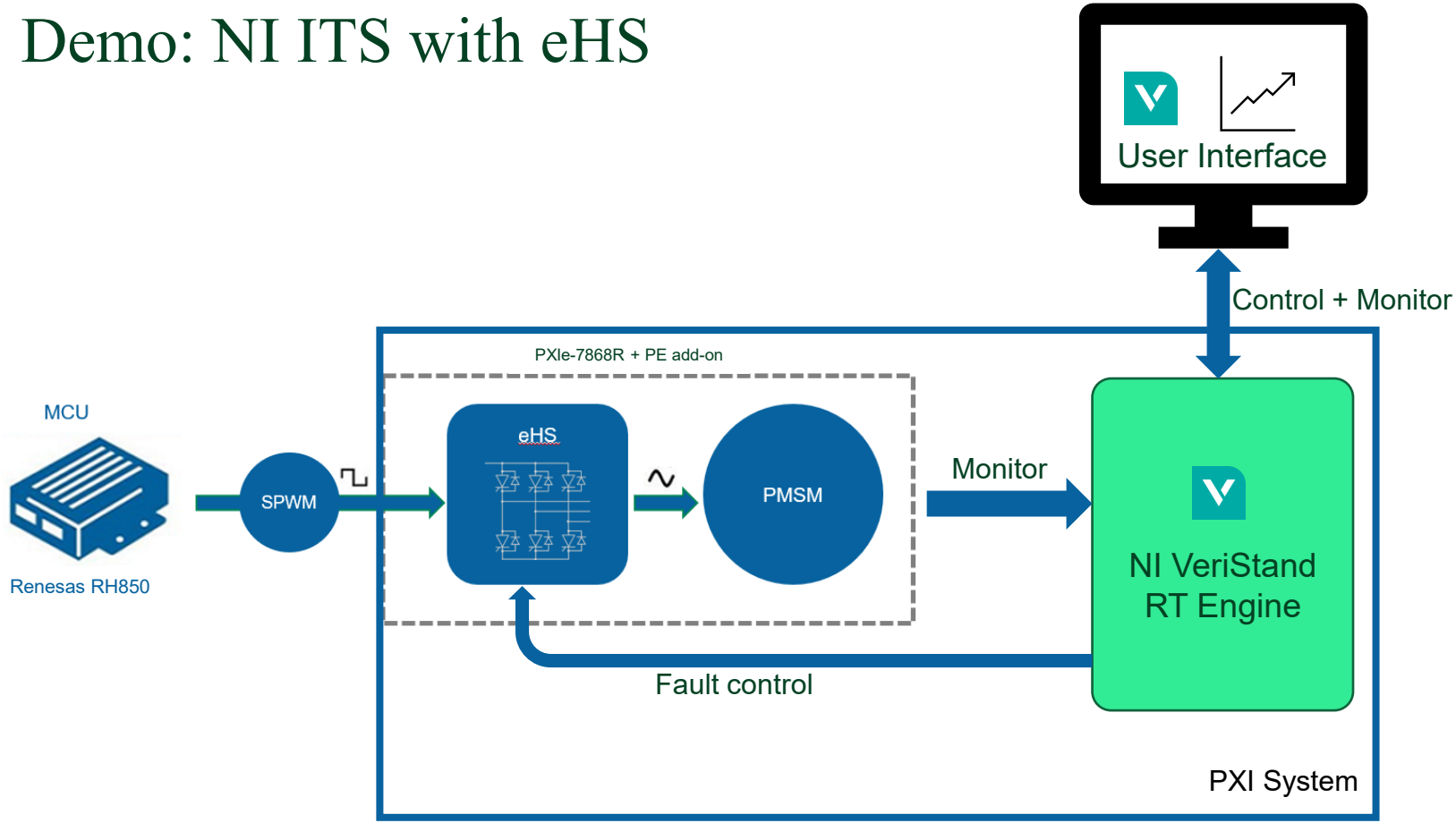
10 hours to 1hour

eHS Workflow

Create/Edit Circuit Model (MIL) — Simscape → Modify the Circuit in Seconds Without any Bitstream Generation → Validate model behavior → Operationalize HIL Test

CALIBRATE MODEL BEHAVIOR

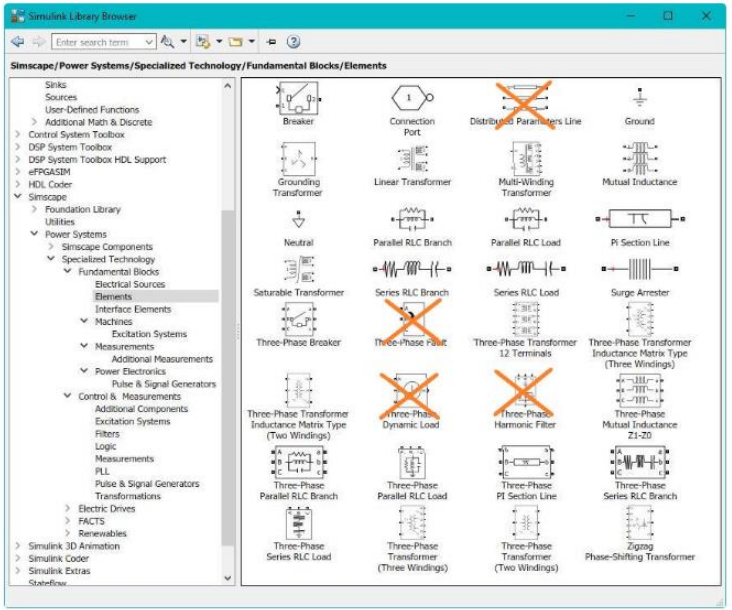
Demo: NI ITS with eHS



eHS SUPPORTED BLOCKS in Simulink

Simscape Power Systems

- Electrical Sources
  - AC and DC Current and Voltage sources
- Electrical Elements
  - RLC, Breakers, Transformers
- Power Electronics
  - IGBTs and diodes
  - Ideal switch
  - MOSFET
  - Bridge blocks
- Measurements
  - Current and Voltage



See complete list in:
https://opal-rt.atlassian.net/wiki/spaces/PNIVS/pages/140741224/Simscape+Power+Systems+Simulink

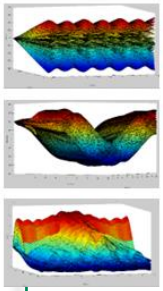
MACHINES

Motors integrated with Finite Element Analysis (FEA) tools such as JMAG-RT & ANSYS MAXWELL include the capability to simulate:

- The effects of rotor asymmetry
- Back-EMF harmonics
- Saturation effects
- Cogging torque

Import of spatial harmonic tables (FEA)

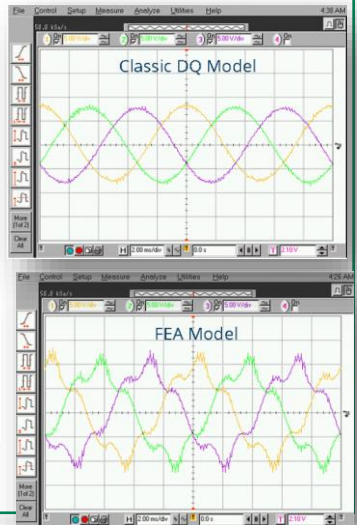
- Torque, Flux & Inductance Table

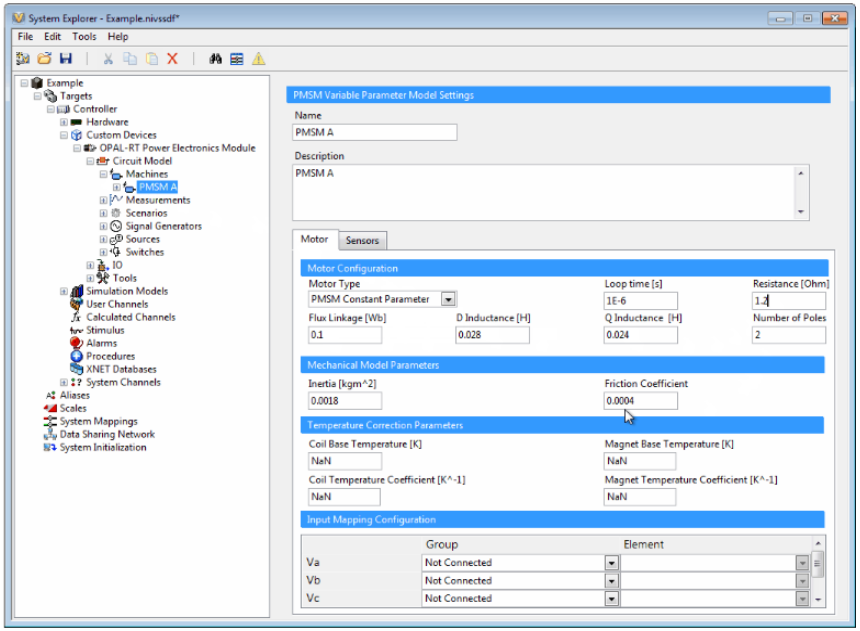


JMAG

MotorSolve BLDC

ANSYS Maxwell



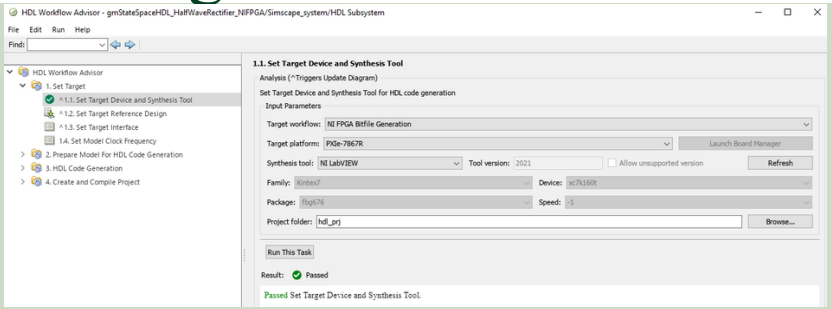


NI R&D Activities - HDL Coder Integration

Previous NI workflow for LabVIEW integration of HDL Coder was not optimal and difficult for customers to use.

Following successful evaluation, NI collaborated with MathWorks to add a new NI Workflow into HDL Coder Workflow Advisor

Capability shipped in R2022b as a MATLAB Add-on; additional improvements in subsequent releases



R2022b

Ship NI Workflow in HDL Workflow Advisor

- Initial support NI R-Series HW
- Support interface type: Register & Board I/O
- Invoke NI LabVIEW for integration and FPGA synthesis

R2023a – 23.0 Release

- Expanded support for NI R-Series boards
- Usability improvements with HDL Coder and NI Workflow

R2023a, 2023b – 23.5 and 24.0 Release

- Added support for NI FlexRIO boards and Xilinx Ultrascale FPGAs
- Bug fixes and usability improvements with HDL Coder and NI Workflow

Turn-key solution with ACEWORKS

- NI ITS
- Collaboration with ACEWORKS

NI SOLUTION

Inverter Test System

Signal-Level Traction Inverter Validation

HIL Real-Time Powertrain Simulation

1, 2, or 4 DUT Configurations

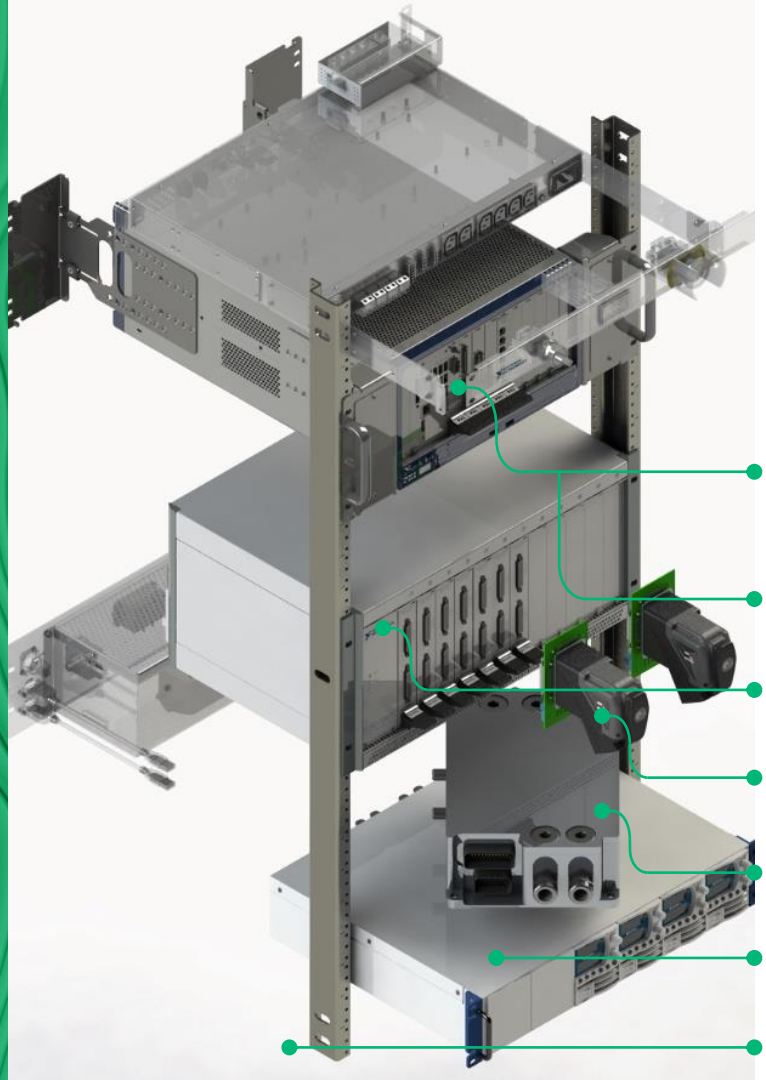
Integrated Model Workflow

Signal Banked Mass Interconnect

Faster Deployment and Procurement

ITS Architecture & Advantages

- Customer defined
- Flexible and scalable
- High performance
- Open for integration



Software	SystemLink – data and system management TestStand – test executive VeriStand – real-time test and model integration Opal-RT add-on – FPGA based PE modeling LabVIEW – programming and customization
PXI	Measurements and I/O Communications Power Electronics Models in FPGA
SLSC	Switch, Load, Signal Conditioning for fault insertion and routing signal paths. Ease of connection and wiring.
Connectivity	Cabling references for flexible connections to DUTs
DUT	Traction inverter ‘control board’ aka ‘MCU/VCU’ aka ‘cracked inverter’
RMX	Programmable loads and DUT power
ATE Core Configurations	Complete Test Systems Delivered

NI × ACEWORKS Partnership

ACEWORKS

- **NI system integration partner specialized in HIL** (since 2009)
- ACEWORKS SLSC modules (such as ACE-BASE-FIU32, …)
- VeriStand custom devices (such as XNET CAN/LIN, …)
- VeriStand user training program
- Major HIL domain (xEV Powertrain)
  - Inverter & motor (Signal-Level and Power-Level)
  - ICCU (Onboard charger, DC-DC converter)
  - BMS (Battery Management System)

Integration Partner
SYSTEM INTEGRATOR

ACEWORKS won the **Best Collaboration Award** at NI Korea Partner Day 2023.

NI Days 2025 Participation:

- **ICCU & Power Electronics HIL demo** & exhibition
- **Technical session seminar** on 'HILSmart Solution for MBD-based Electric Vehicle Control SW Development and Verification'

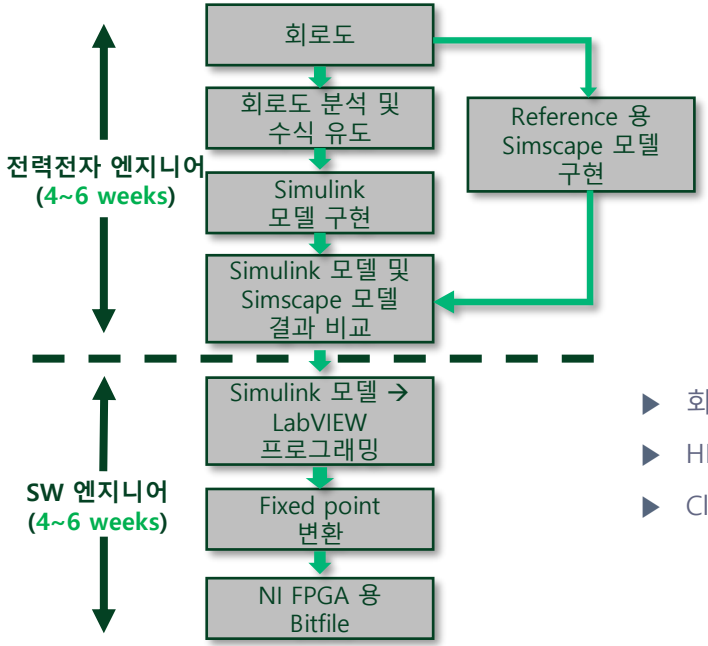
NI x ACEWORKS HIL Platform

The HIL Platform is mainly used for the BMS SW development and verification of a Global OEM 'H'.

NI Best Collaboration Award

ACEWORKS Advanced HIL solution (for Power Electronics)

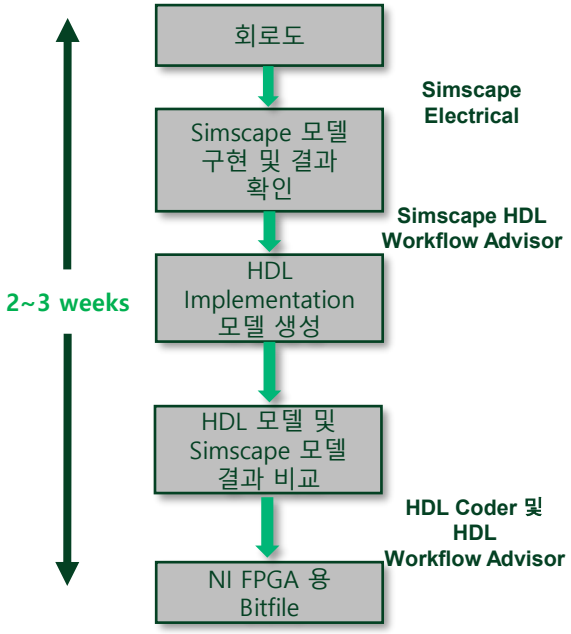
- Usability improvements with HDL Coder and NI Workflow
- Convert Simscape circuit models to HDL-compatible Simulink Implementation Models



[기존 Workflow]

- 회로도 수작업 수식 유도 생략
- HDL 모델 및 Bitfile 생성 자동화
- Closed-loop 테스트 까지 빠르게 연계

→ 전체 개발 기간 단축 가능



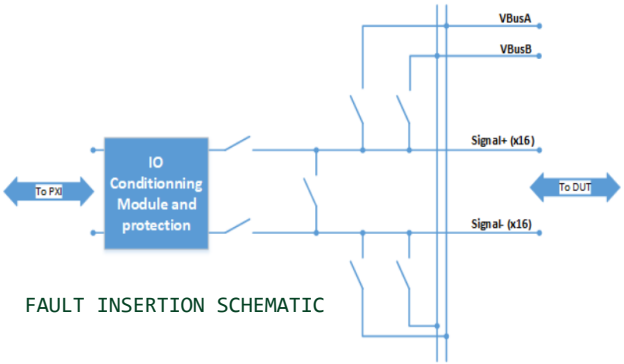
[개선된 Workflow (Mathworks 기반)]

Fault Insertion

SLSC – Switch, Load, and Signal Conditioning

Available Faults (per channel):

- Open
- Short
  - Signal Pair
  - VBus
  - GND



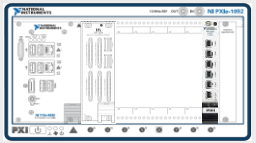
FAULT INSERTION SCHEMATIC

Module	Description	Fault Ins.
SLSC-12201	32 DIO: 5V to 33V	N
ACE-BASE-FIU32	32 CH, SLSC Base Module, Passthrough	Y
ACE-COMM-FIU12	12 CH, CAN | LIN Bus Interface	Y
ACE-RSM-FIU16	16 CH, Resistor Sim., 50Ω to 4MΩ	Y
ACE-PB-DIN08	8 DI, High Speed, piggyback board	Y
ACE-PB-DOUT08	8 DO, High Speed, piggyback board	Y
ACE-PB-AIN08D	8 AI, Differential Input, piggyback board	Y
ACE-PB-AOUT08	8 AO, Single-ended output, piggyback board	Y
ACE-PB-AOUT08D	4 AO, Differential output, piggyback board	Y

Number of modules depends on config – refer to sHIL Signal List for more details

Signal-Level Inverter HIL Options

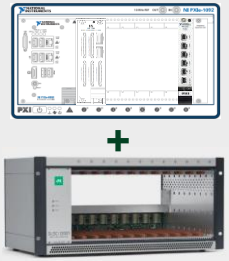
sHIL Base Bundle
(Basic IO for DIY)



Test Development
System Completion
DUT-specific Customization
Harness / Breakout Box
Mass Interconnect
Custom Cabling
Tester Design
Core Rack: Safety, Display, Power
Fault Insertion
Signal Conditioning

Instrumentation

sHIL Bundle w/ SLSC Options
(Complete IO for DIY)



Test Development
System Completion
DUT-specific Customization
Harness / Breakout Box
Mass Interconnect
Custom Cabling
Tester Design
Core Rack: Safety, Display, Power

Fault Insertion
Signal Conditioning
Instrumentation

Inverter Test System
(First-level Integrated HIL)

Test Development
System Completion
DUT-specific Customization
Harness / Breakout Box

Mass Interconnect
Custom Cabling
Tester Design
Core Rack: Safety, Display, Power
Fault Insertion
Signal Conditioning
Instrumentation

ACEWORKS

NI

INSTRUMENTATION PLATFORM

TEST SYSTEM PLATFORM

Summary

Key Takeaways

1. Multiple stages of EV Power Conversion HIL up to DUT development stages
   : Signal-level and Power-level EV

2. For sHIL, FPGA technology is essential to simulate power converting circuits.
   Especially, requirements on FPGA is getting higher up to market trend

3. NI FPGA has advantages on 2 aspects to simulate power circuit model.
   - FPGA hardware: Faster digital IO and higher capacity
   - FPGA algorithm: Comprehensive and faster development than using HDL
     - Option#1: PE Add-on for NI VeriStand enabling User-DIY but limited flexibility
     - Option#2: Simulink HDLCoder with limitless flexibility but require support from experts

4. NI provides various option of building EV PC sHIL system: from platform to system (NI-ITS)

5. ACEWORKS could provide value of..
   - Seamless solution delivery regardless of various option
   - Guaranteed quality of system with expertise

Thank you