uModule & uSLIC
전력 설계의 단순화

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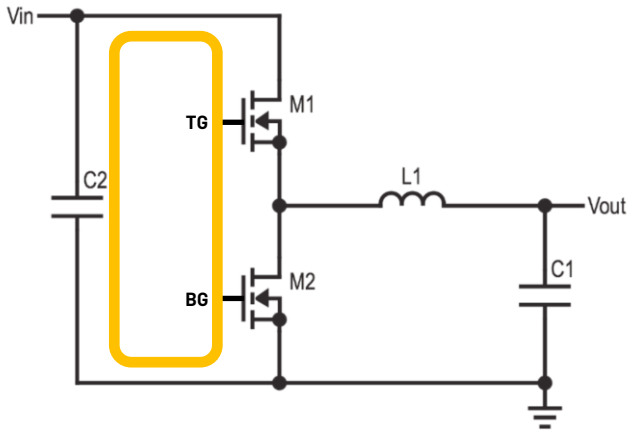
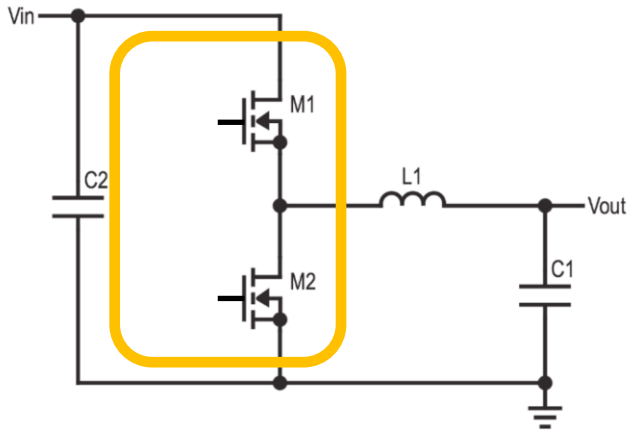
Past and Present

Buck Converter Integration Levels

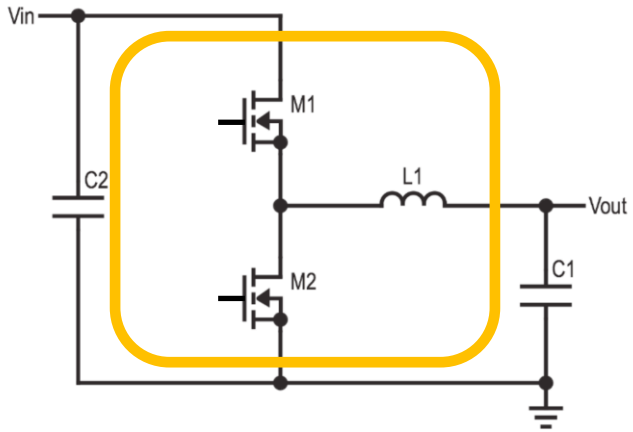
Controller



Monolithic



uModule



특징	Controller	Monolithic	uModule
집적도	낮음	중간	높음
효율	매우 높음 최적화 시 95%+	높음 90~95%	높음 Monolithic ±1~2%
설계 난이도	어려움 외장 부품/레이아웃 최적화 필요	중간 외장 인덕터, 패시브 최적화 필요	쉬움 Plug and Play
디자인 사이즈	큼 외장 부품 다수	중간	작음 부품 수 감소
열 관리	주의 요함 발열 경로 설계 필수	중간	최적화 패키지 차원
EMI 리스크	높음 루프/게이트 드라이브 영향	중간	낮음
부품 단가	낮음	중간	높음

Controller vs uModule

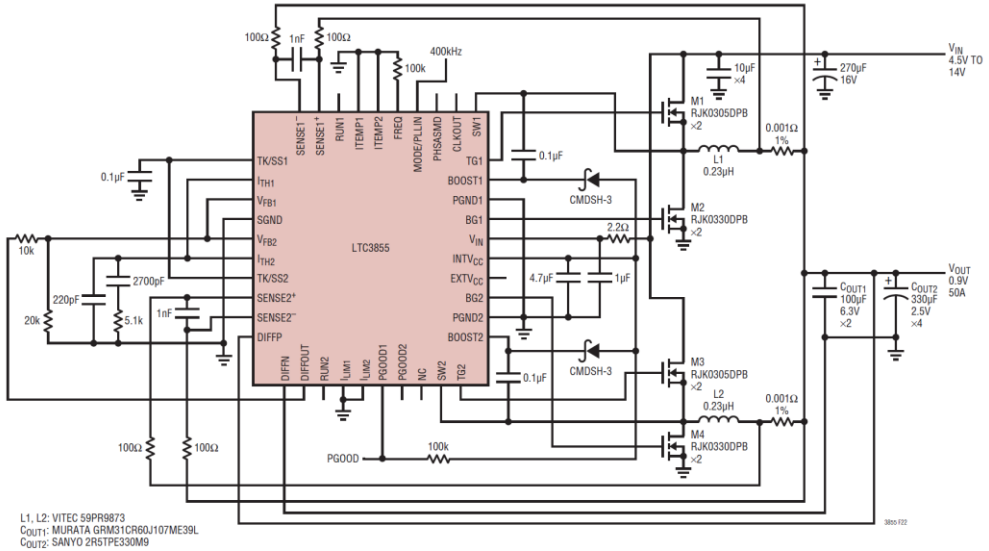


Figure 22. Small Size, Dual Phase 0.9V, 50A Supply, f_{SW} = 400kHz

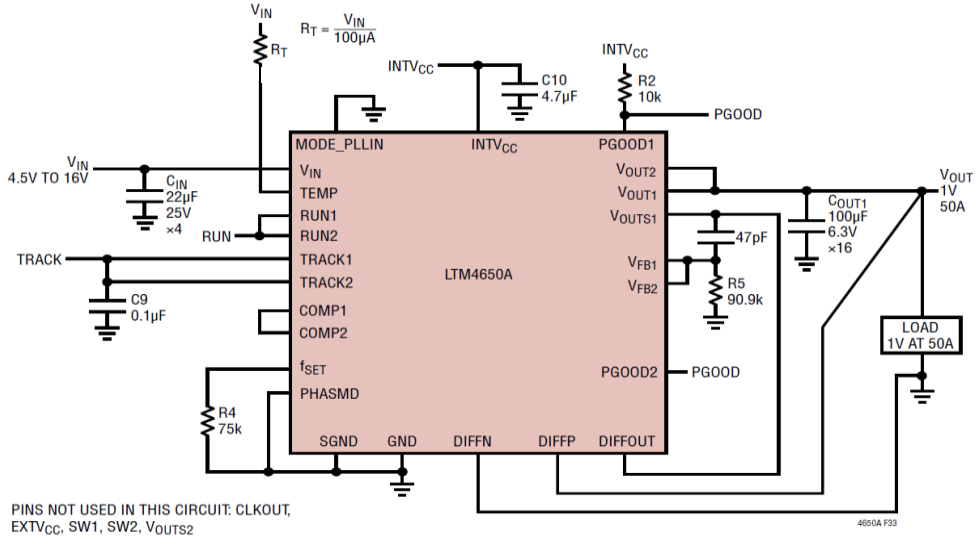
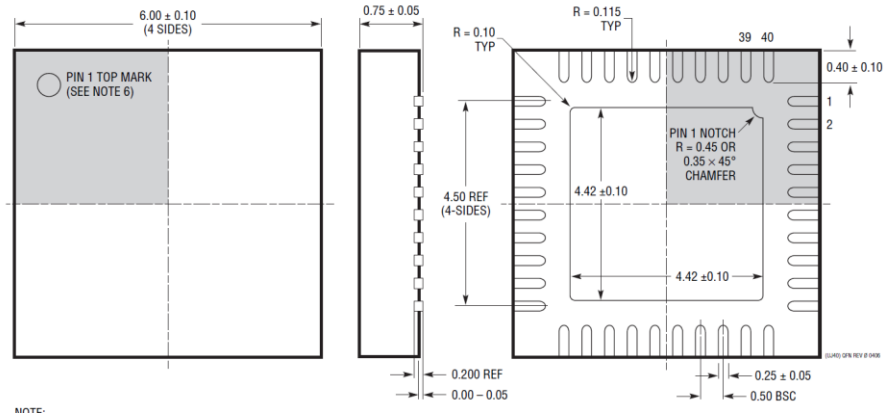
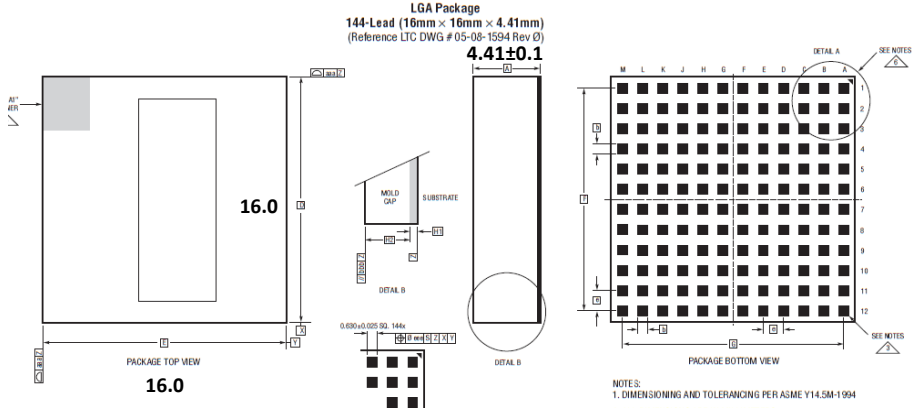
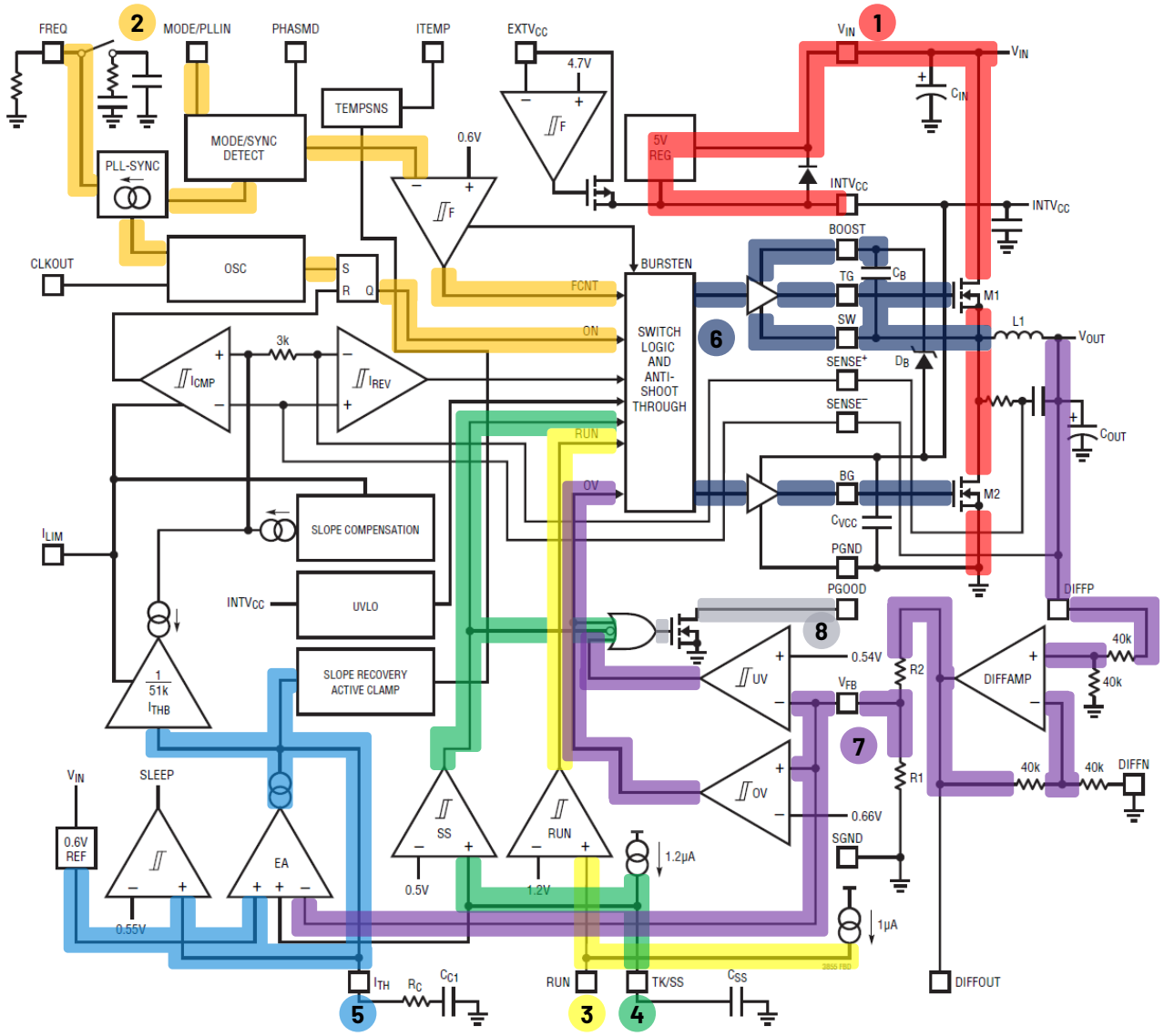


Figure 33. LTM4650A 2-Phase, 1V at 50A Design





Controller Circuit Operation Sequence



Controller Circuit Design : Switching Frequency

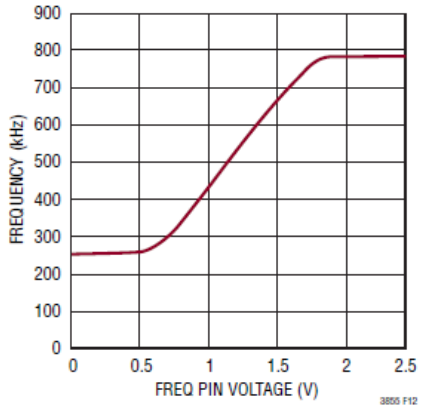


Figure 12. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

		MIN	TYP	MAX	
I_{FREQ}	Frequency Setting Current	9	10	11	μA

- $300kHz \fallingdotseq V_{freq}$
- $0.75V = 10uA \times 75K\Omega (= R_{freq})$

- 인덕터 값 선정
- Duty Cycle 영향
- 전력 손실
- EMI 스펙트럼 변화
- Cin, Cout 용량

		MIN	TYP	MAX	
$t_{ON(MIN)}$	Minimum On-Time		90		ns

- $V_{OUT.min} = V_{IN} \times f_{sw} \times t_{on.min}$
- $0.81V = 20V \times 450kHz \times 90ns$

Controller Circuit Design : Inductor Selection

STANDARD ELECTRICAL SPECIFICATIONS

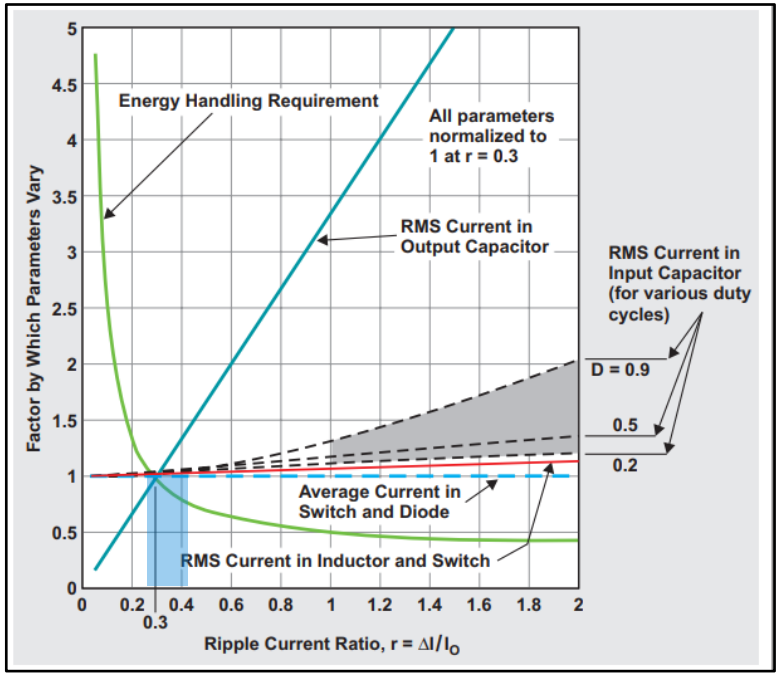
L_0 INDUCTANCE ± 20 % AT 100 kHz, 0.25 V, 0 A (µH)	DCR TYP. 25 °C (mΩ)	DCR MAX. 25 °C (mΩ)	HEAT RATING CURRENT DC TYP. (A) (1)	SATURATION CURRENT DC TYP. (A) (2)	SRF TYP. (MHz)
0.10	2.7	2.9	21.0	25.0	266
0.22	4.1	4.5	17.0	13.0	146
0.33	5.5	5.9	13.0	7.5	108
0.47	7.1	7.7	12.5	8.0	83
1.0	16.8	18.1	7.5	7.0	66
2.2	34.9	37.7	5.0	5.5	41
3.3	53.5	57.8	4.1	4.7	29
4.7	75.3	81.3	3.2	3.0	27
5.6	85.2	92.0	3.0	2.2	24
6.8	114.0	121.0	2.8	2.1	21
10.0	169.3	182.8	2.2	2.0	17

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}}\left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L}\right)$$

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

$$L_{MIN} > \frac{V_{OUT}}{f_{SW} \bullet I_{LOAD(MAX)}} \bullet 1.4$$



Controller Circuit Design : Current Sense

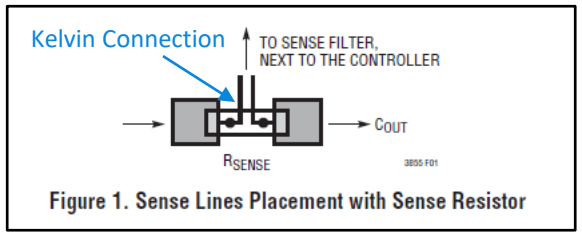
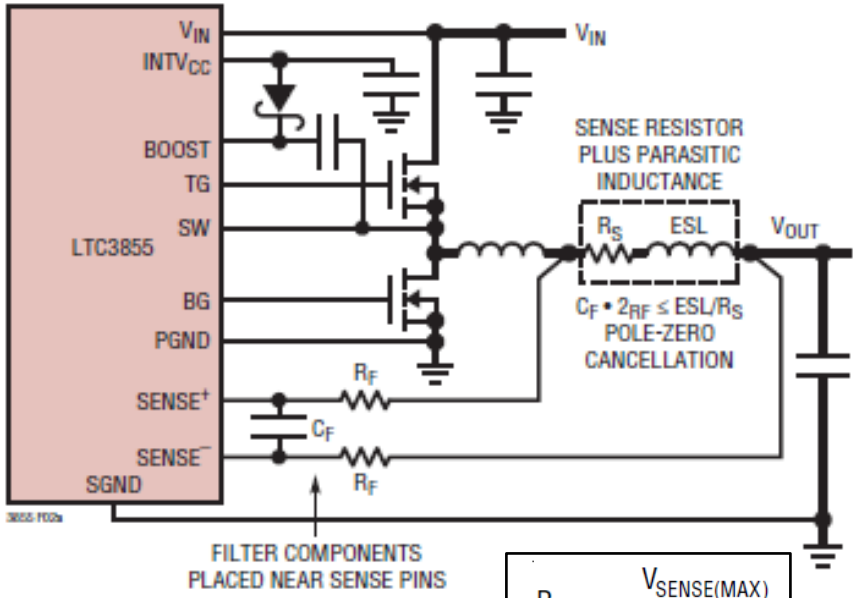
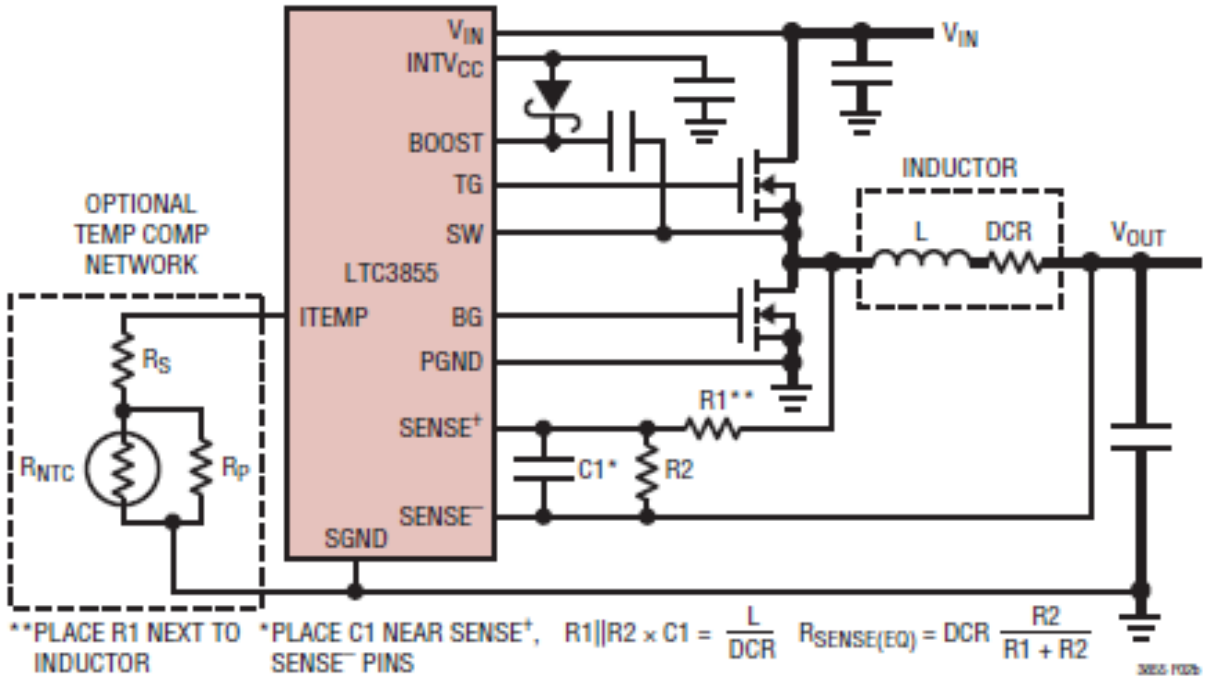


Figure 1. Sense Lines Placement with Sense Resistor



$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{(MAX)} + \frac{\Delta I_L}{2}}$$



$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{(MAX)} + \frac{\Delta I_L}{2}}$$

$$R1||R2 = \frac{L}{(DCR \text{ at } 20^{\circ}C) \bullet C1}$$

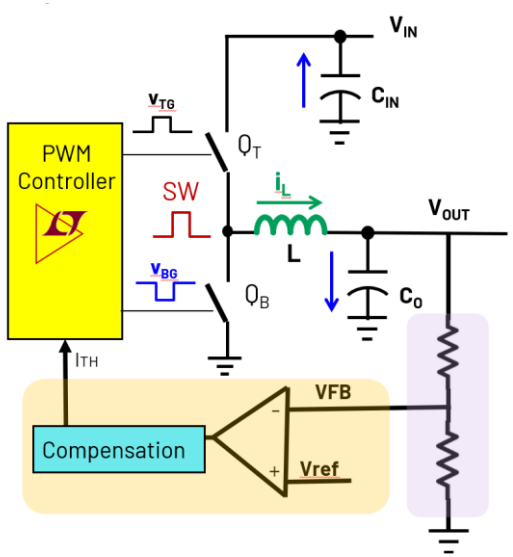
$$\Delta V_{SENSE} = \frac{V_{IN} - V_{OUT}}{R1 \bullet C1} \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

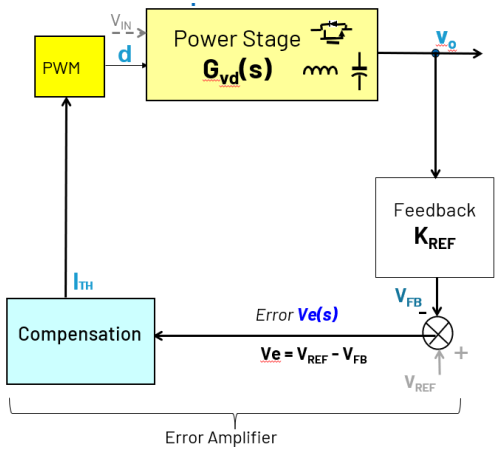
$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{(MAX)} \text{ at } T_{L(MAX)}}$$

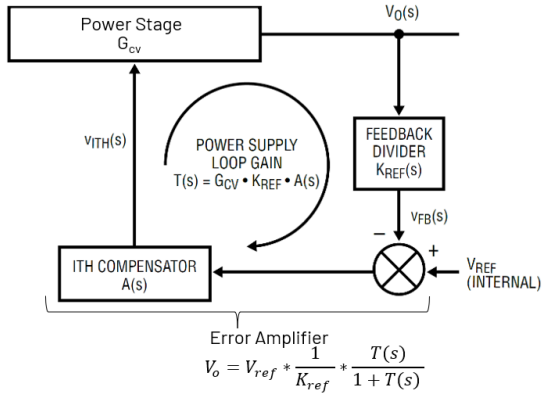
The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D}; \quad R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

Controller Circuit Design : Loop Stability



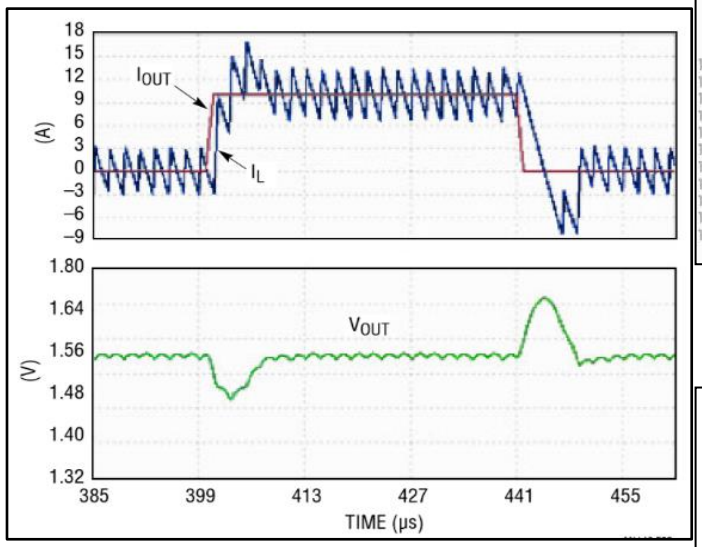




$$V_o = V_{ref} * \frac{1}{K_{ref}} * \frac{T(s)}{1+T(s)}$$

Loop gain: $T(s) = G_{CV}(s) \cdot K_{REF}(s) \cdot A(s)$

높은 대역폭 & 안정



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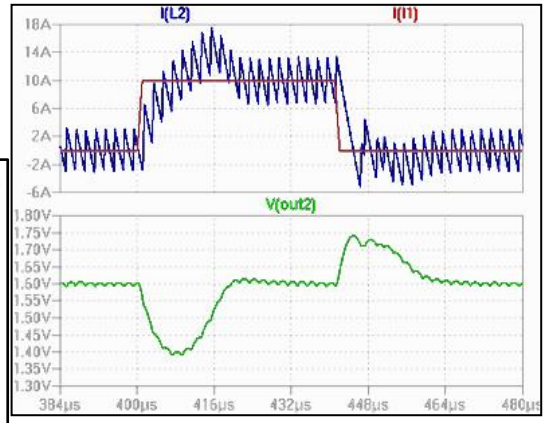

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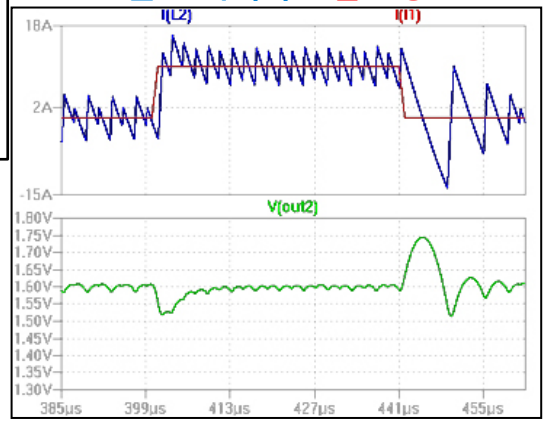
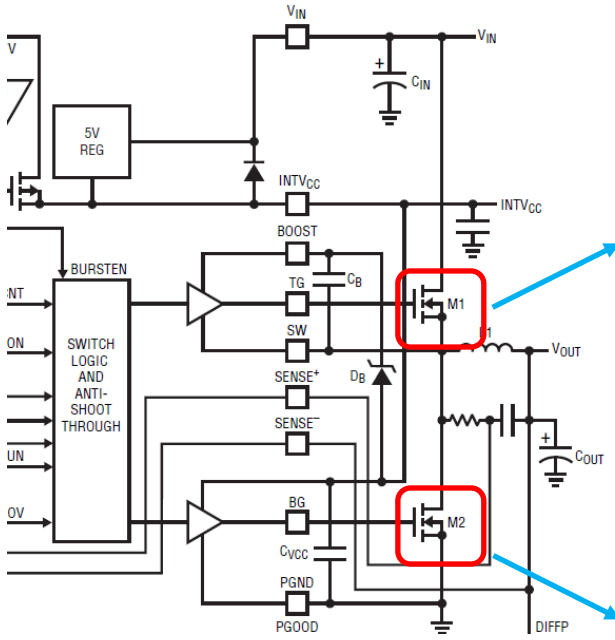


Controller Circuit Design : MOSFET Selection



$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC}-V_{TH(MIN)}}+\frac{1}{V_{TH(MIN)}}\right]\bullet f_{OSC}$$

*또는 C_{RSS}

MOSFET results in: $R_{DS(ON)}$ = 13mΩ (max), V_{MILLER} = 2.6V, $C_{MILLER} \cong$ 150pF. At maximum input voltage with T_J (estimated) = 75°C:

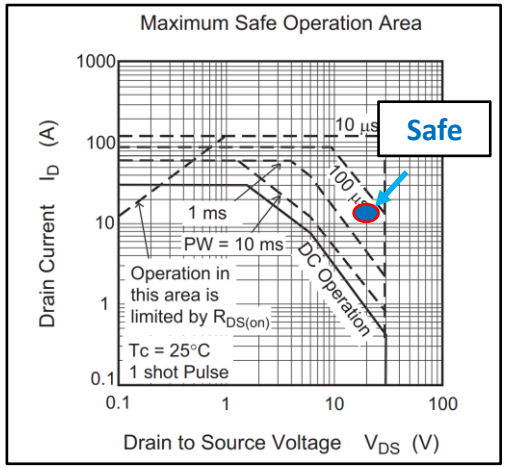
$$P_{MAIN} = \frac{1.8V}{20V}(15A)^2[1+(0.005)(75°C-25°C)]\bullet (0.013\Omega)+(20V)^2\left(\frac{15A}{2}\right)(2\Omega)(150pF)\bullet\left[\frac{1}{5V-2.6V}+\frac{1}{2.6V}\right](400kHz)$$
$$= 329mW + 288mW$$
$$= 617mW$$

$$P_{SYNC} = \frac{V_{IN}-V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

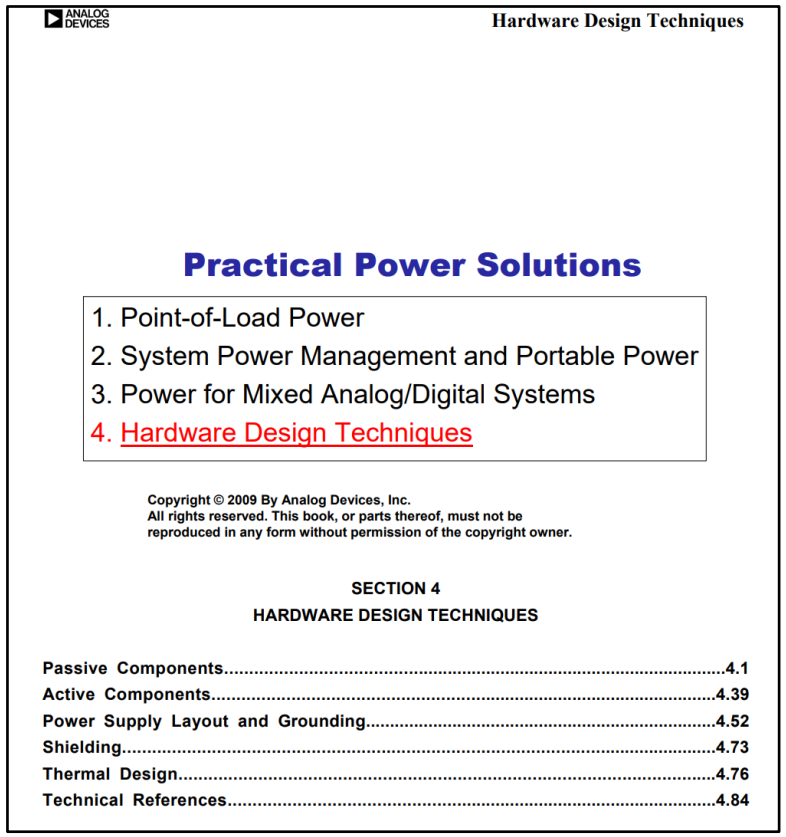
A Renesas RJK0330DPB, $R_{DS(ON)}$ = 3.9mΩ, is chosen for the bottom FET. The resulting power loss is:

$$P_{SYNC} = \frac{20V-1.8V}{20V}(15A)^2\bullet[1+(0.005)\bullet(75°C-25°C)]\bullet 0.0039\Omega$$

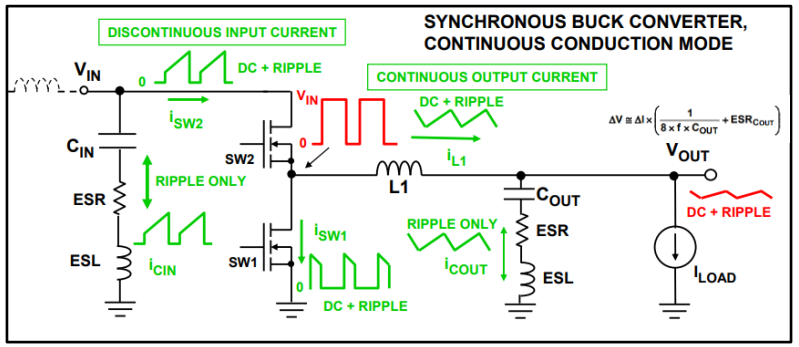
P_{SYNC} = 1W



Controller Circuit Design : Input & Output Capacitor

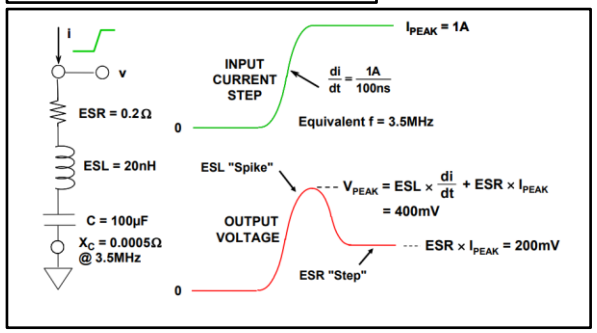


https://www.analog.com/media/en/training-seminars/design-handbooks/Practical-Power-Solutions/Section4.pdf

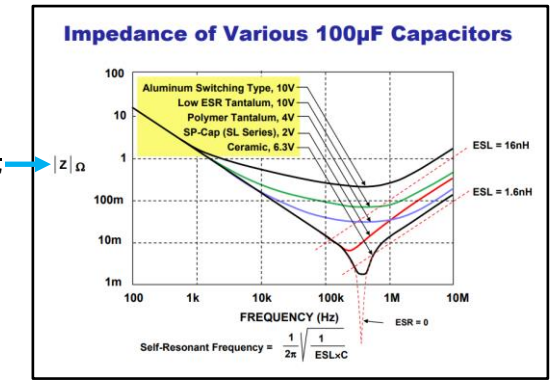


$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2}$$

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$



$$|Z| = \frac{I}{\omega C}$$



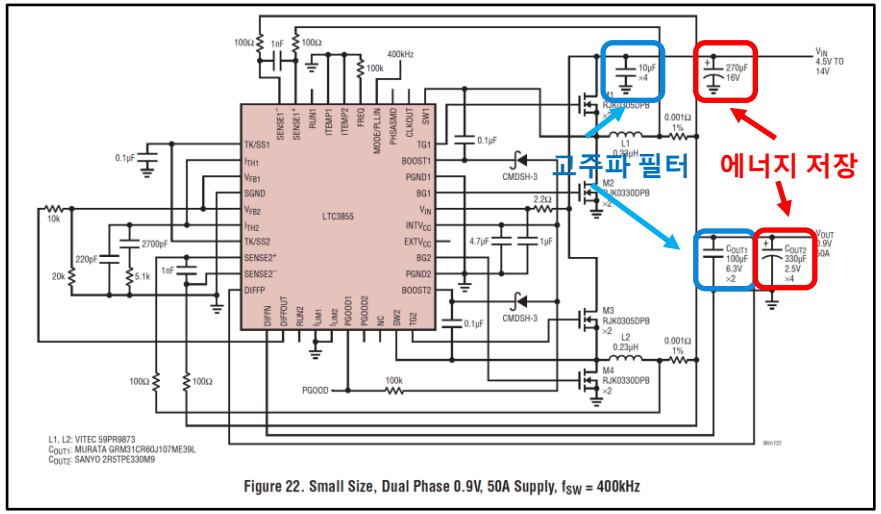
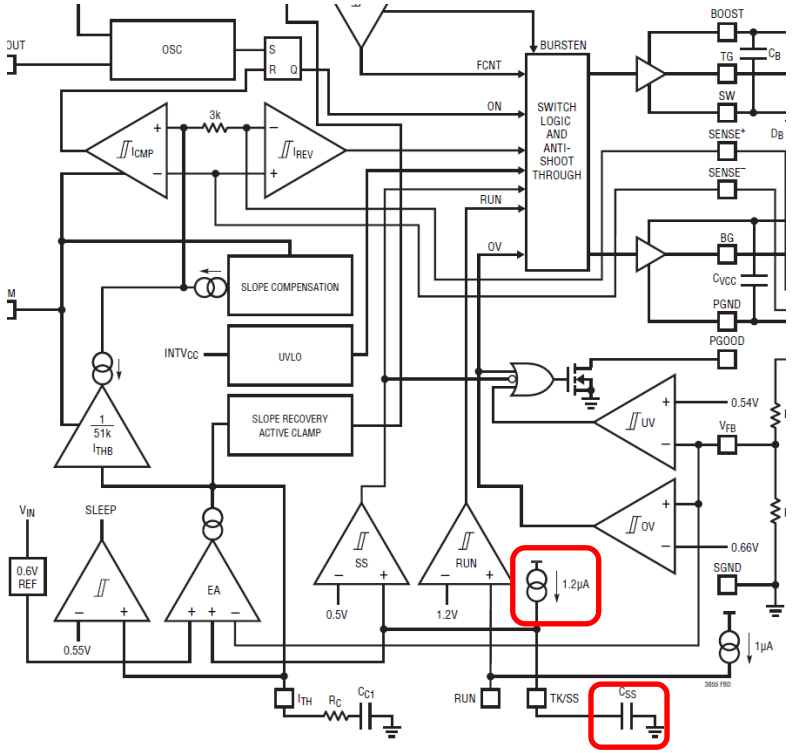


Figure 22. Small Size, Dual Phase 0.9V, 50A Supply, f_{SW} = 400kHz

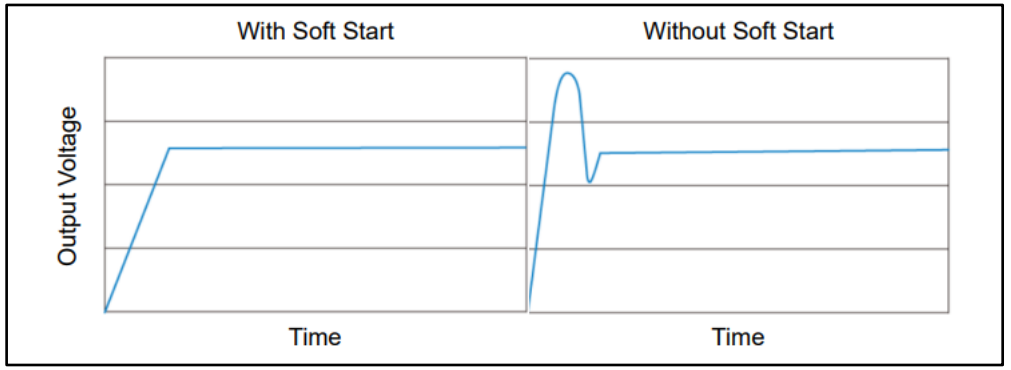
Controller Circuit Design : Soft Start



$$t_{SOFTSTART} = 0.6 \bullet \frac{C_{SS}}{1.2\mu A}$$

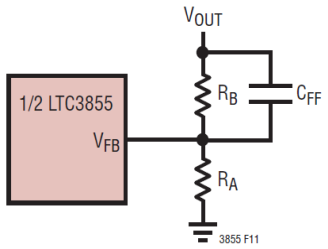
- $Q = C \times V$
- $I = C \times \frac{\Delta V}{\Delta t}$ (ΔV ← 0.6V, Δt ← Tss)

1.2uA Css



Controller Circuit Design : Output Voltage

To improve the frequency response, a feed-forward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.



$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

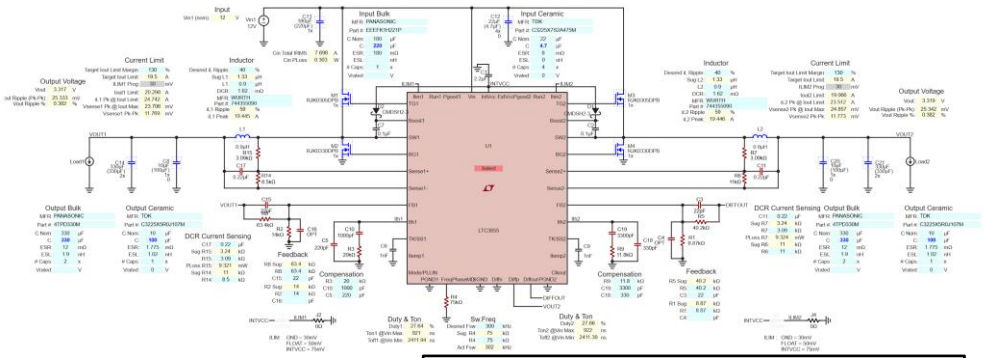
1Ω	10Ω	11Ω	12Ω	13Ω	15Ω	16Ω	18Ω	20Ω	22Ω	24Ω	24.9Ω	27Ω	30Ω
33Ω	36Ω	39Ω	43Ω	47Ω	49.9Ω	51Ω	56Ω	62Ω	68Ω	75Ω	82Ω	91Ω	100Ω
110Ω	120Ω	124Ω	130Ω	140Ω	150Ω	160Ω	180Ω	200Ω	210Ω	220R	240Ω	249Ω	270Ω
280Ω	300Ω	316Ω	330Ω	360Ω	374Ω	390Ω	412Ω	430Ω	470Ω	499Ω	510Ω	560Ω	590Ω
604Ω	620Ω	680Ω	750Ω	806Ω	820Ω	910Ω	1K	1.05K	1.1K	1.15K	1.2K	1.24K	1.3K
1.4K	1.5K	1.6K	1.65K	1.74K	1.8K	2K	2.1K	2.2K	2.32K	2.4K	2.49K	2.7K	2.8K
2.94K	3K	3.09K	3.3K	3.4K	3.6K	3.74K	3.9K	4.02K	4.3K	4.42K	4.64K	4.7K	4.99K
5.1K	5.23K	5.49K	5.6K	5.9K	6.04K	6.2K	6.49K	6.8K	7.15K	7.5K	8.06K	8.2K	9.1K
10K	11K	12K	13K	14K	15K	16K	18K	20K	21K	22K	24K	24.9K	27K
28K	30K	33K	36K	39K	40.2K	43K	47K	49.9K	51K	56K	59K	60.4K	62K
68K	75K	82K	91K	100K	120K	130K	150K	180K	200K	220K	270K	300K	330K
390K	470K	499K	560K	680K	1M								

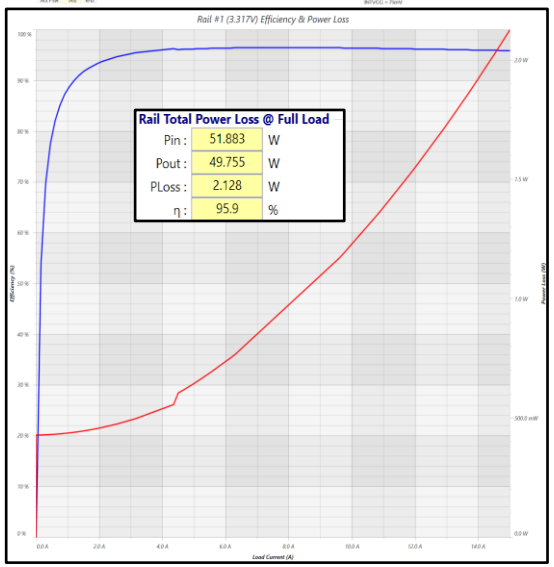
- $f_{zero-CFF} = \frac{1}{2\pi \times C_{FF} \times R_B}$
- $f_{pole-CFF} = \frac{1}{2\pi \times C_{FF} \times (R_B || R_A)}$
- $C_{FF} = \frac{1}{2\pi \times f_x} \times \frac{1}{\sqrt{R_B \times (R_B || R_A)}}$
- $f_x = \frac{K}{V_{OUT} \times C_{OUT}}$

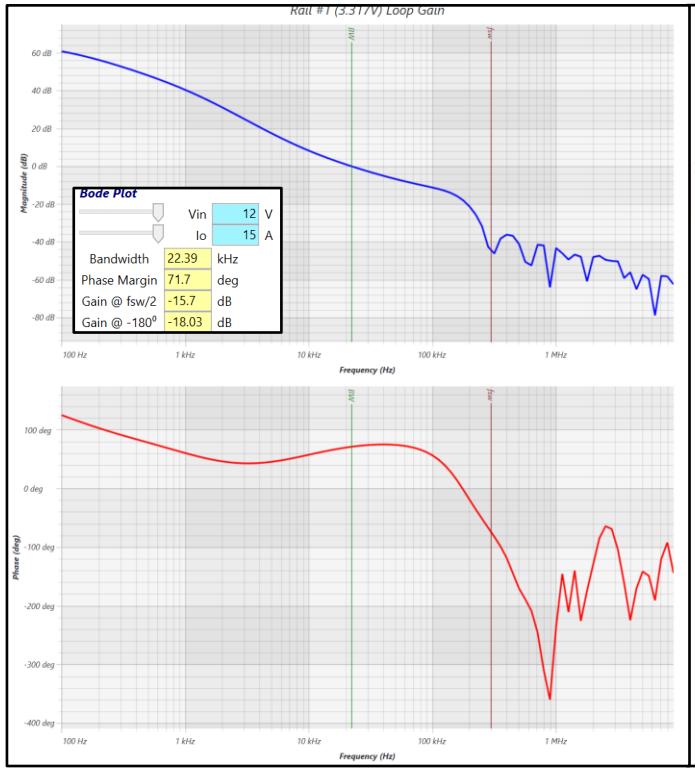
(단, K = 제어 루프 고유 상수로 제품마다 다름)

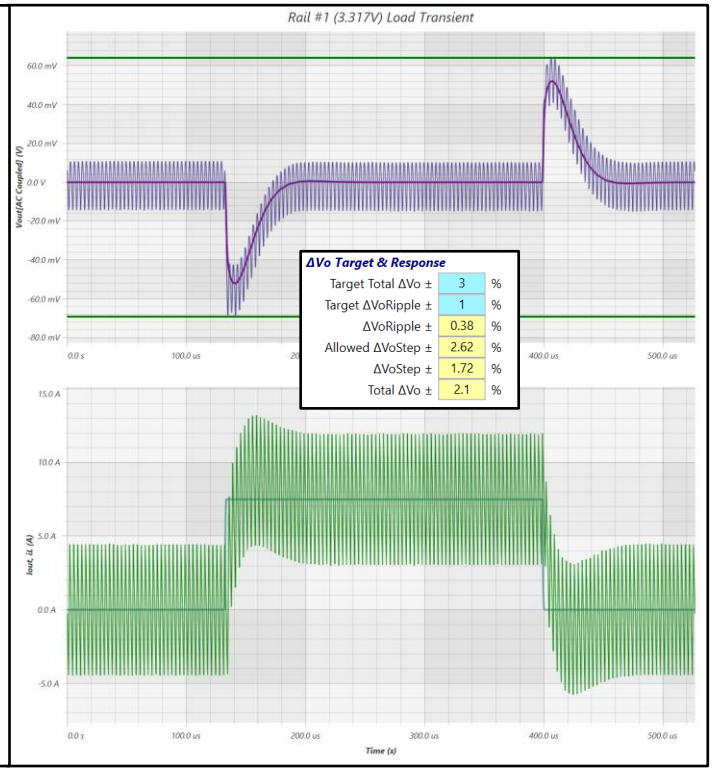
Controller Circuit Design Simulation Result

- LTpowerCAD.exe Configuration
  - 12Vin
  - 300kHz
  - 3.3Vout @15A/ch



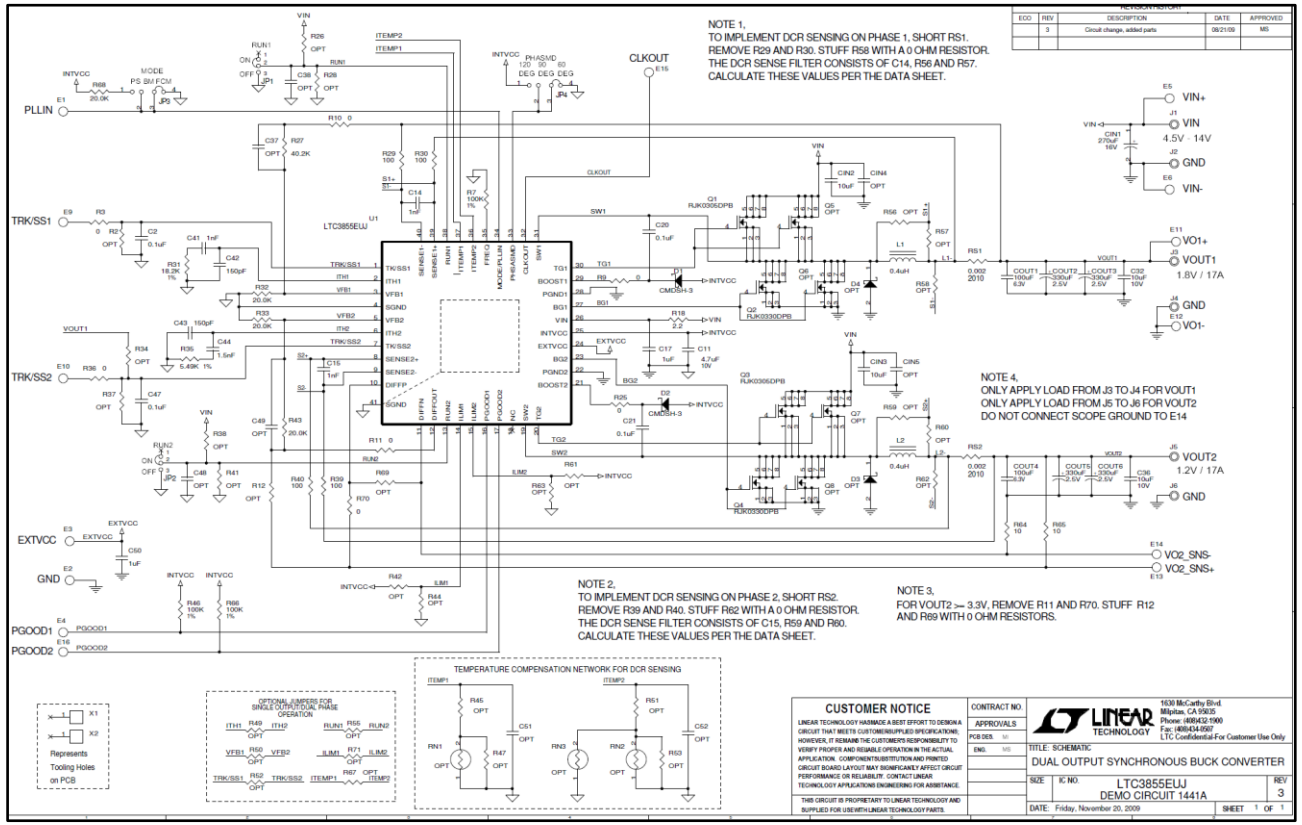


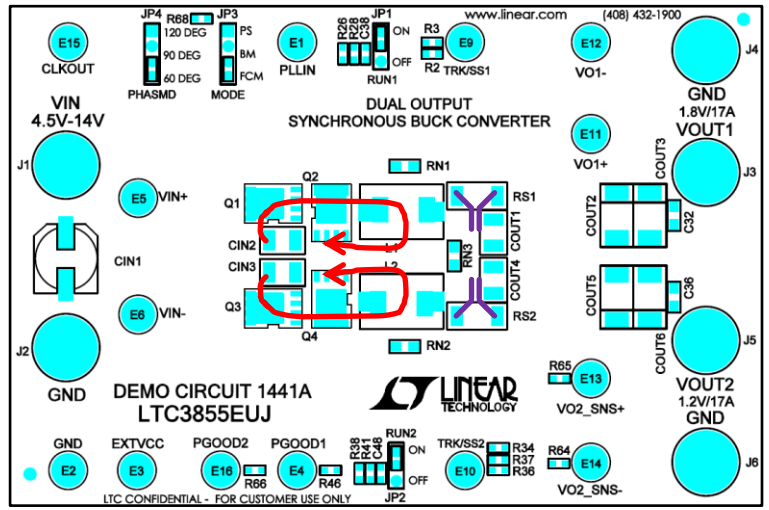


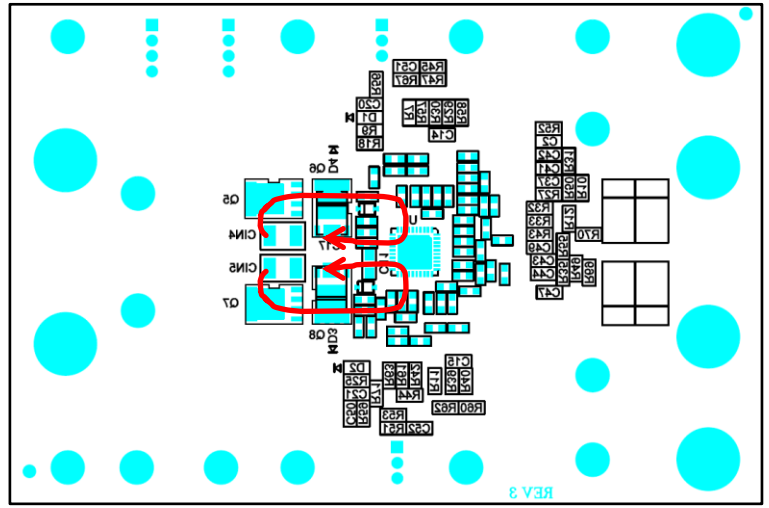


- Target Compensation Network
  - Bandwidth $\leq \frac{1}{5} \sim \frac{1}{10} f_{sw} (= 300kHz)$
  - Phase Margin $\geq 45^{\circ}$
  - Gain @$\frac{f_{sw}}{2} \leq$ -8dB
  - Gain @-180° $\geq$ 10dB

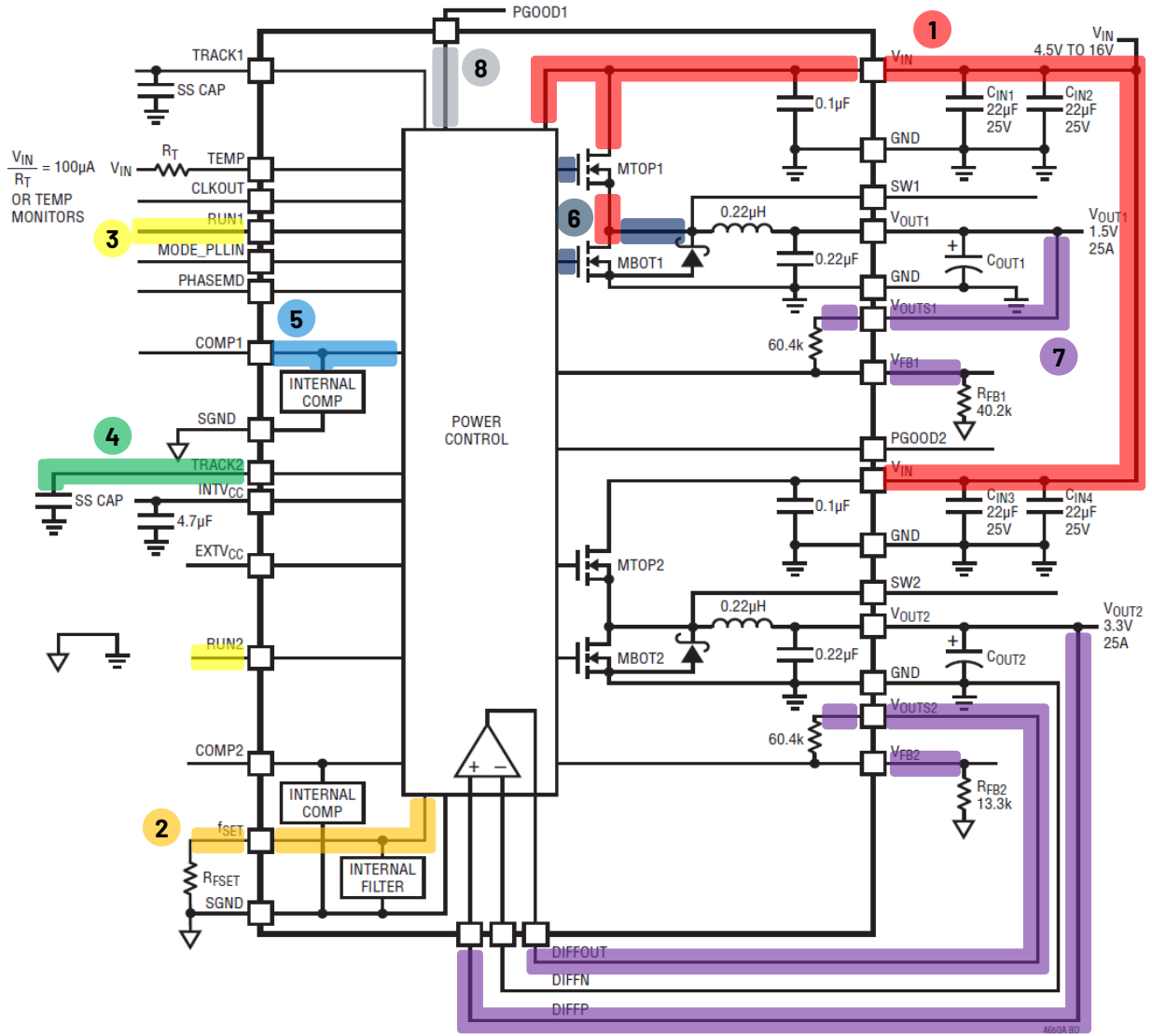
Controller Artwork Design







uModule Circuit Operation Sequence



uModule Circuit Design

- Switching Frequency

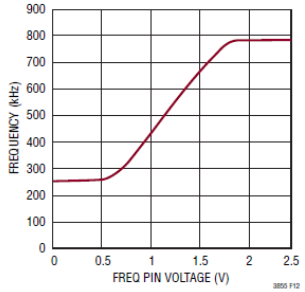


Figure 12. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

- Soft Start

$$t_{SS} = 0.6 \bullet \frac{C_{SS}}{1.3\mu A}$$

- Output Voltage

$$V_{OUT} = 0.6V \bullet \frac{60.4k + R_{FB}}{R_{FB}}$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT}	0.6V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
R_{FB}	Open	90.9k	60.4k	40.2k	30.2k	19.1k	13.3k	8.25k

- Input & Output Capacitor

Input Capacitors

The LTM4650A module should be connected to a low AC-impedance DC source. For the regulator input, two 22µF input ceramic capacitors per channel are used for RMS ripple current. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η% is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, Polymer capacitor.

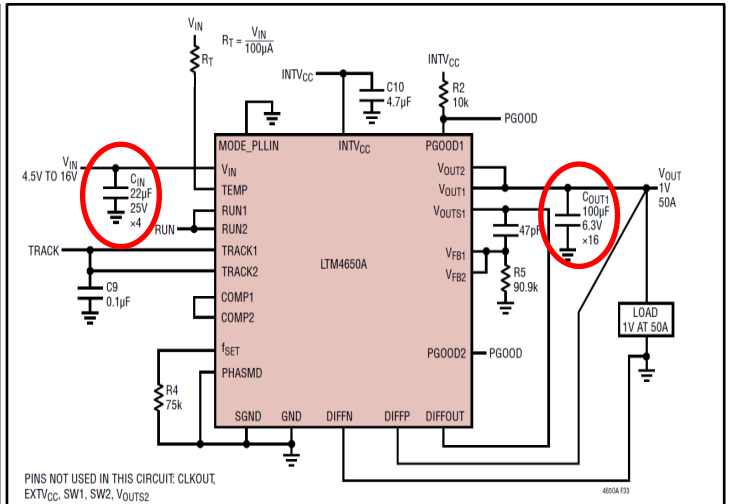


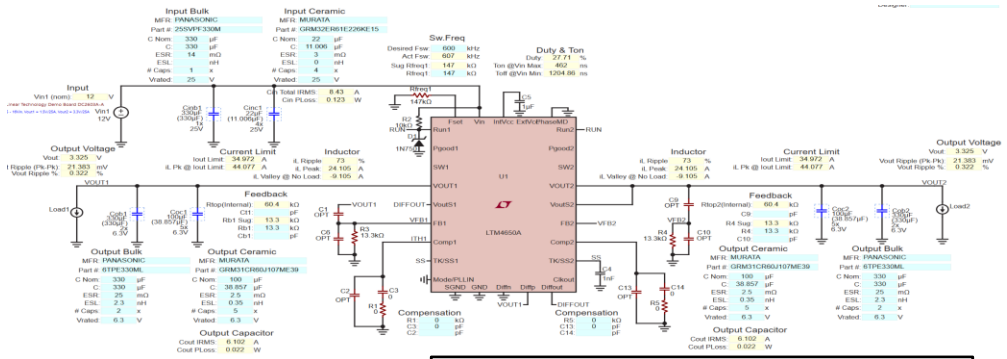
Figure 33. LTM4650A 2-Phase, 1V at 50A Design

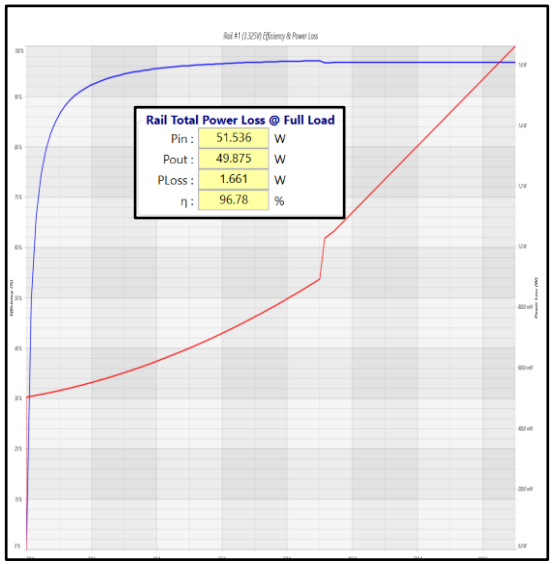
Output Capacitors

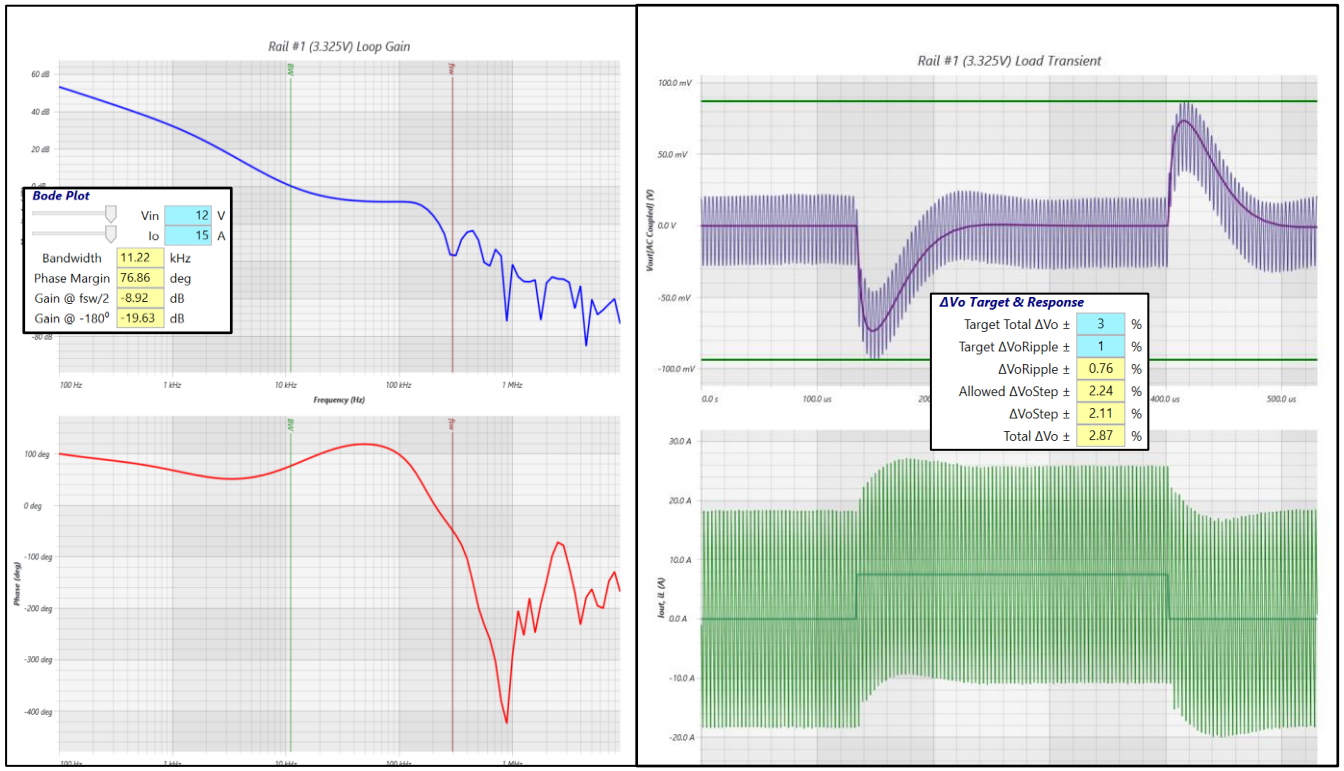
The LTM4650A is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, the low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 300µF to 800µF per output channel. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 6 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 25% load step. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 6

uModule Circuit Design Simulation Result

- LTpowerCAD.exe Configuration
  - 12Vin
  - 600kHz
  - 3.3Vout @15A/ch

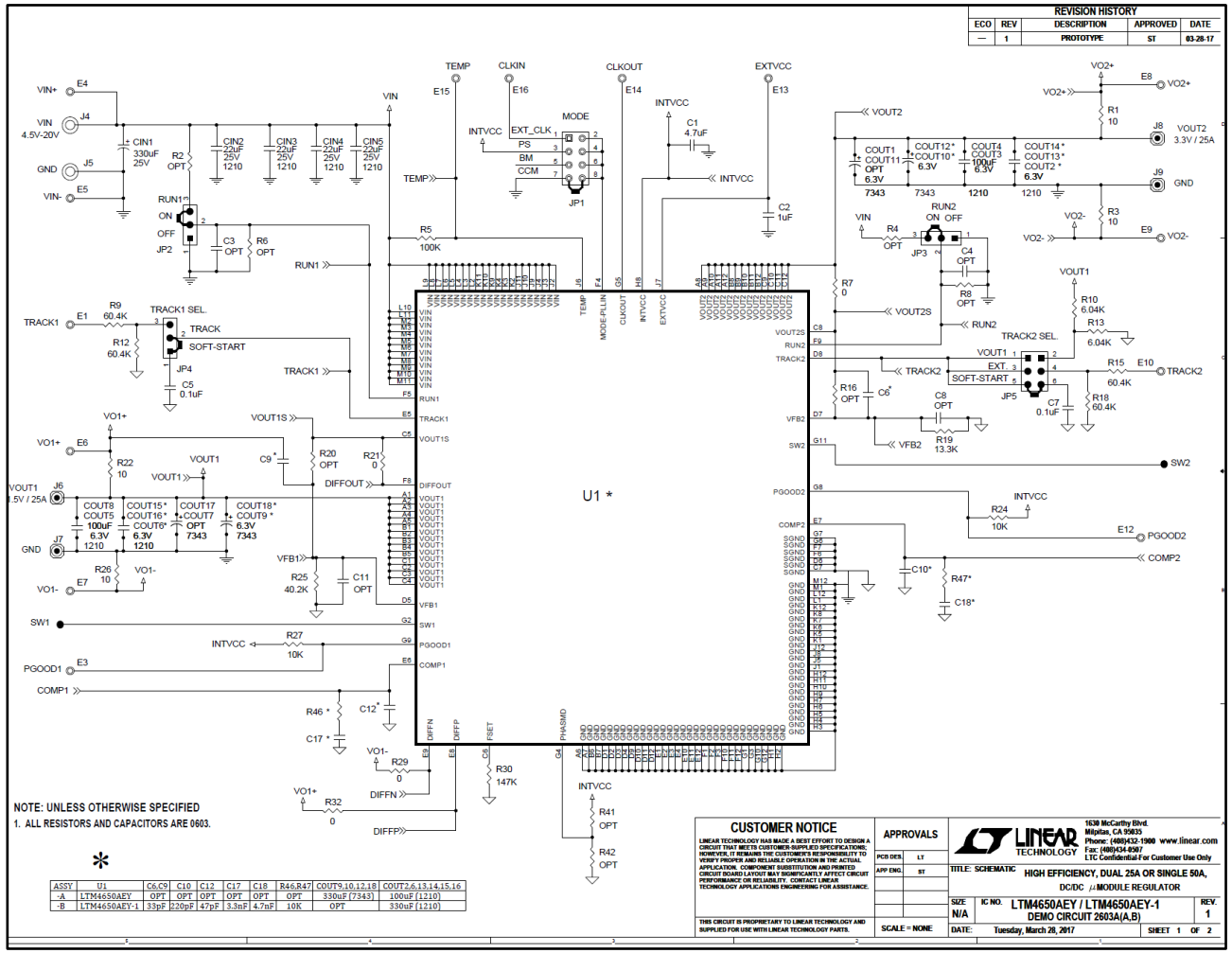


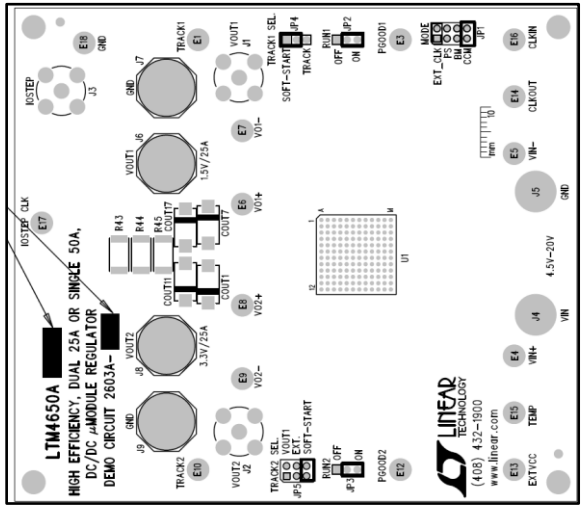


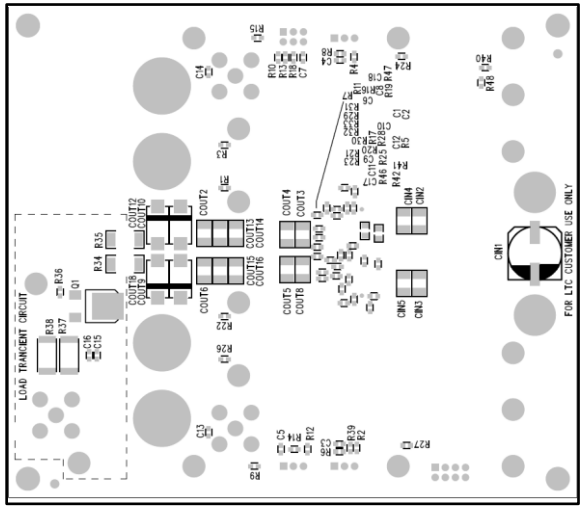


- Target Compensation Network
  - Bandwidth $\leq \frac{1}{5} \sim \frac{1}{10} f_{sw} (= 600kHz)$
  - Phase Margin $\geq 45^{\circ}$
  - Gain @$\frac{f_{sw}}{2} \leq$ -8dB
  - Gain @-180° $\geq$ 10dB

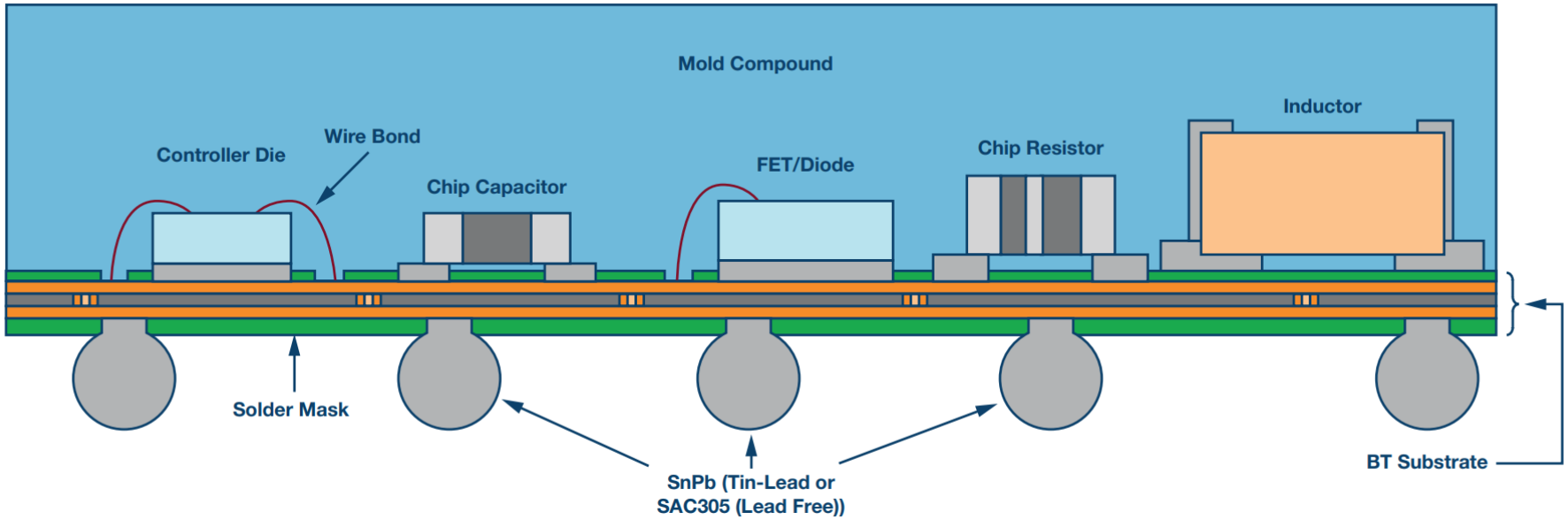
uModule Artwork Design



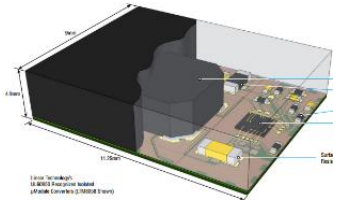




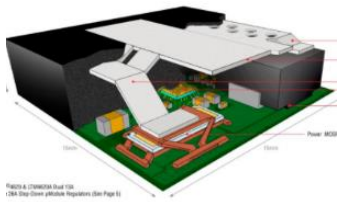
uModule Packge Cross Section



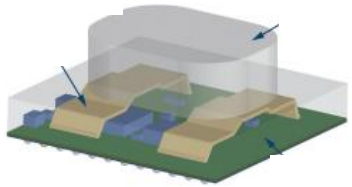
uModule Package Evolution



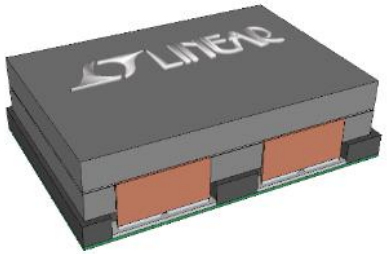
Gen 1: 2006
Standard Mold
10A in 15mm x 15mm



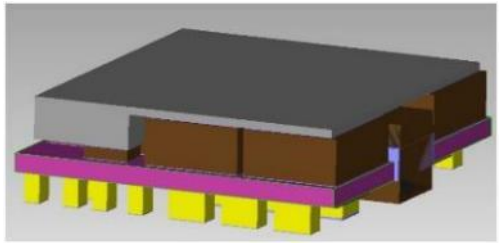
Gen 2: 2012
Integrated Heat Sink
26A in 15mm x 15mm



Gen 3: 2016
Component on Package
40A in 16mm x 16mm



Gen 4: 2018
Component on Package
125A in 15mm x 22mm



Gen 5: 2022
Open Frame
150A in 22mm x 24mm
200A in 22mm x 24mm

Silent Switcher Technology

SS1 Ultralow EMI 방출 → 노이즈 위험성 감소

높은 스위칭 주파수에서도 높은 효율

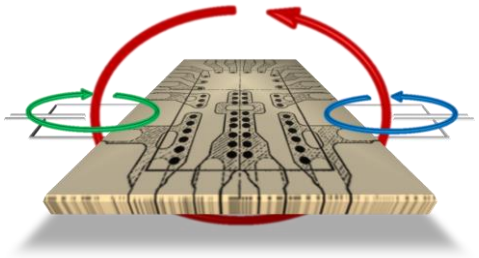
SS2 Silent Switcher 구조에 필요한 바이패스 커패시터 내장

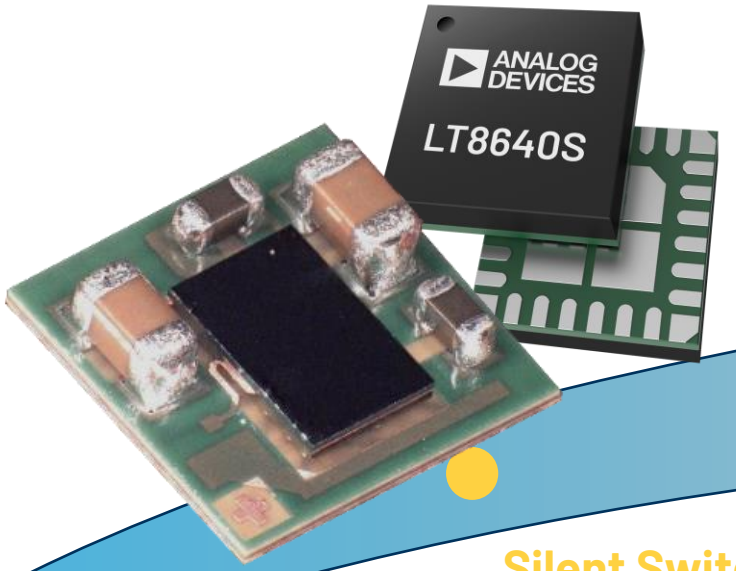
PCB 레이아웃 민감도 최소화

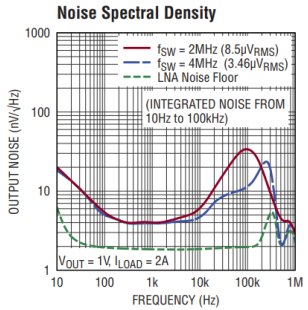
SS3 Ultralow LF 노이즈(0.1Hz to 100kHz)

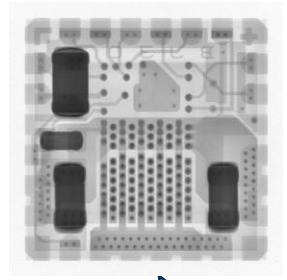
초고속 과도 응답

전체 시스템 성능 향상









Silent Switcher®1

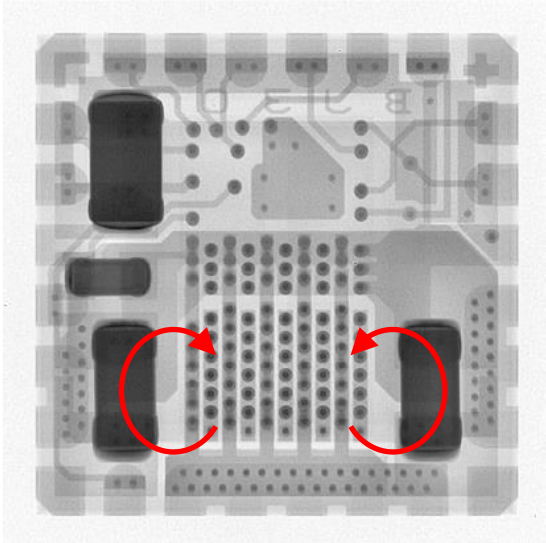
Silent Switcher®2

Silent Switcher®3

µModule with Silent Switcher

- Silent Switcher의 저주파(10Hz ~ 100kHz) 노이즈 성능 향상
- 고전류 환경에서 LDO Post Filter 방식은 더 이상 실용적이지 않음
- 6.25mm × 6.25mm CoP uModule 플랫폼 활용

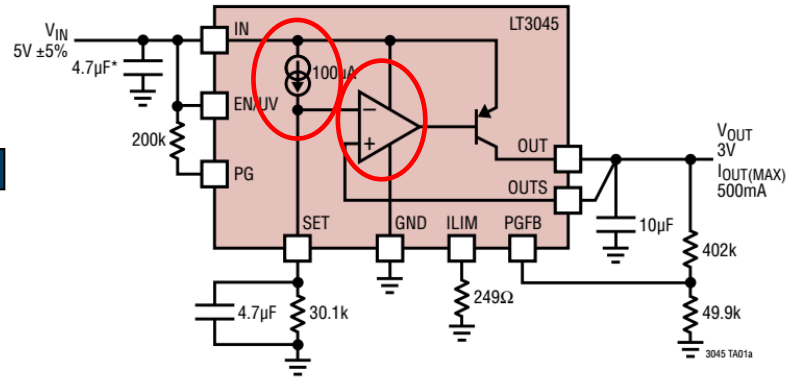
Silent Switcher



LT864xS

Silent Switcher 2

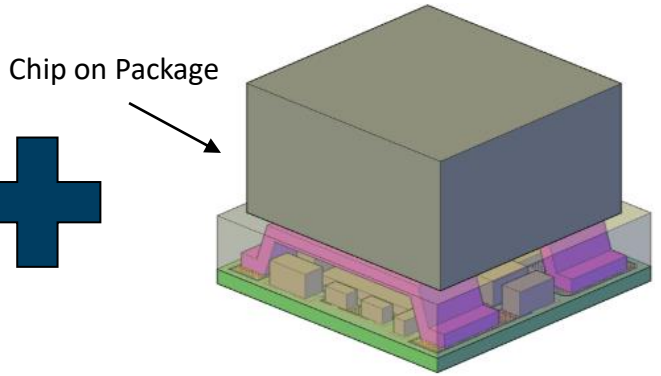
Low Noise
Current Reference
Error Amplifier



LT3045

Ultralow Noise LDO

Tiny CoP µModule



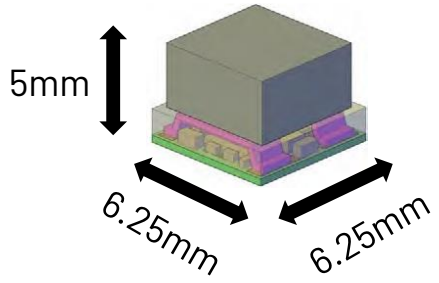
LTM4702/4703/4707

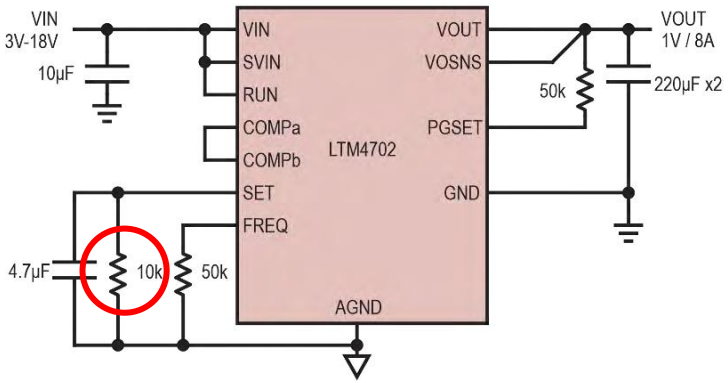
6.25mm × 6.25mm BGA

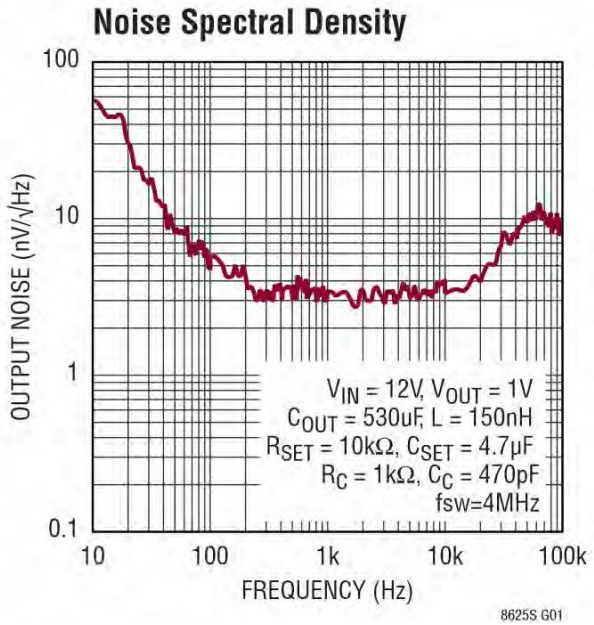
LTM4702: 18Vin, 8A Silent Switcher µModule Regulator

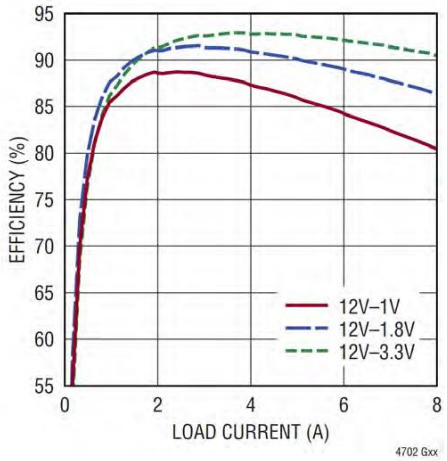
FEATURES

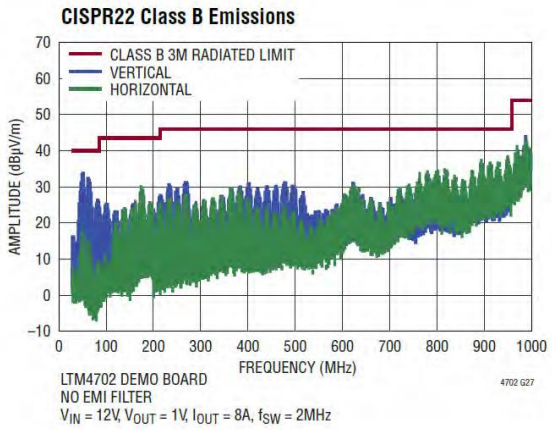
- **Complete Solution in <1cm² (Single-Sided PCB) or 0.5cm² (Dual-Sided PCB)**
- **Low Noise Silent Switcher®3 Architecture**
- **Ultralow EMI Emissions on Any PCB**
- **Ultralow RMS Noise (10Hz to 100kHz): 4µV_{RMS}**
- **Ultralow Spot Noise: 4nV/√Hz at 10kHz**
- **Input Voltage Range: 2.7V to 18V**
- **Output Voltage Range: 0V to 6V**
- **8A Maximum Continuous Output Current**
- **Fast Minimum Switch On-Time: 15ns**
- **Precision Current Reference: 100µA ±0.8% Over Temperature**
- **Fast Start-Up Capability**
- Wide Frequency Range: 300kHz to 4MHz
- Multiphase Parallel with Current Sharing
- Programmable Power Good
- Wide Temperature Range: –55°C to 150°C
- 6.25mm × 6.25mm × 5.02mm BGA Package



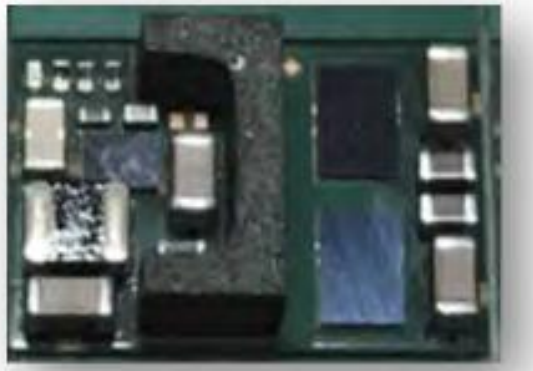


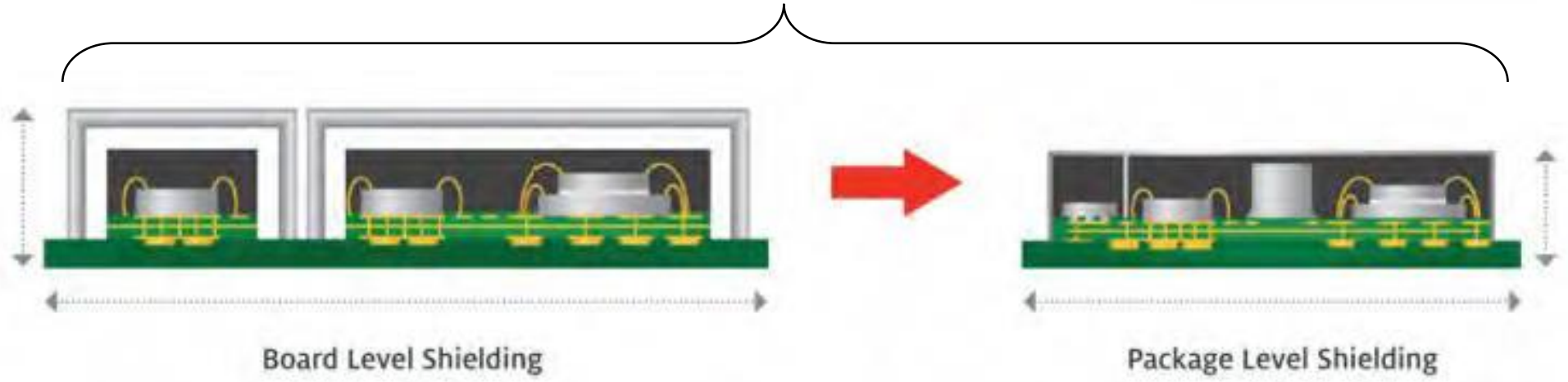




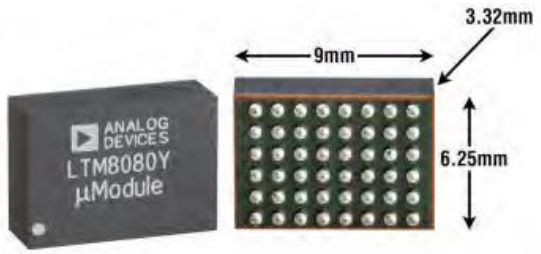


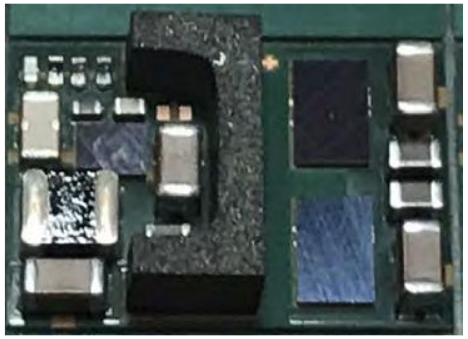
Lowest Noise LDO — Recent Technology Innovations





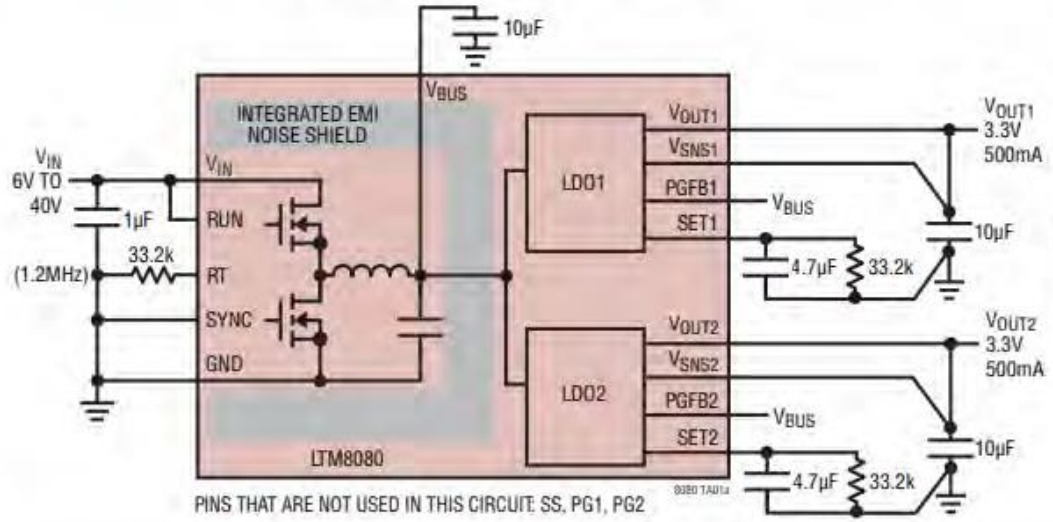
LTM8080: Dual-500mA LDO with Switcher & Shield



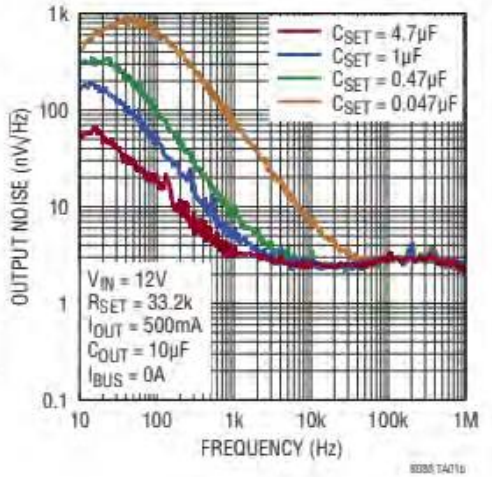


TYPICAL APPLICATION

Dual 3.3V/500mA from 6V to 40V Input



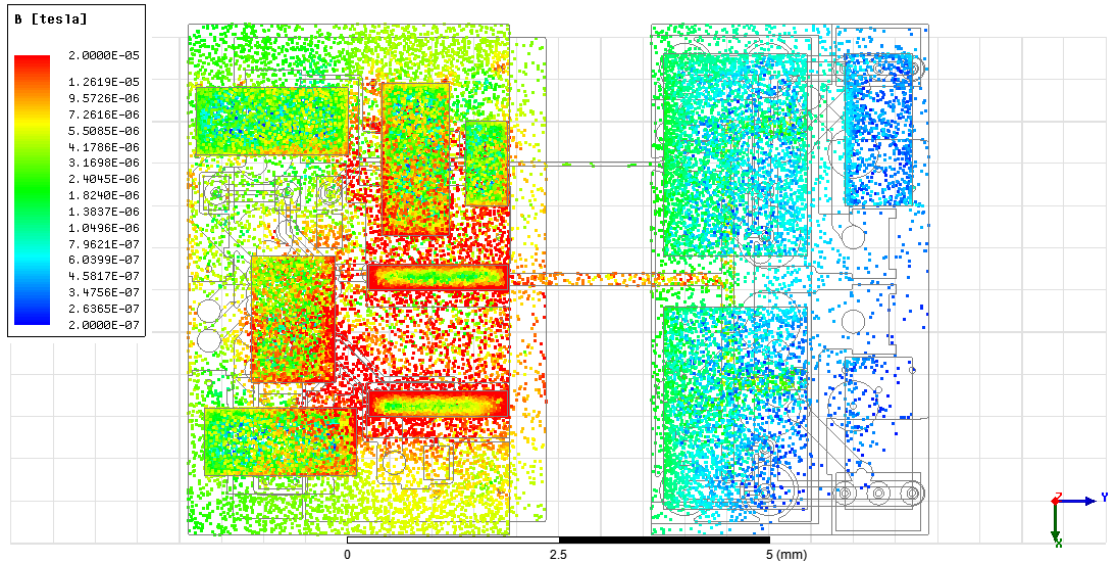
Noise Spectral Density



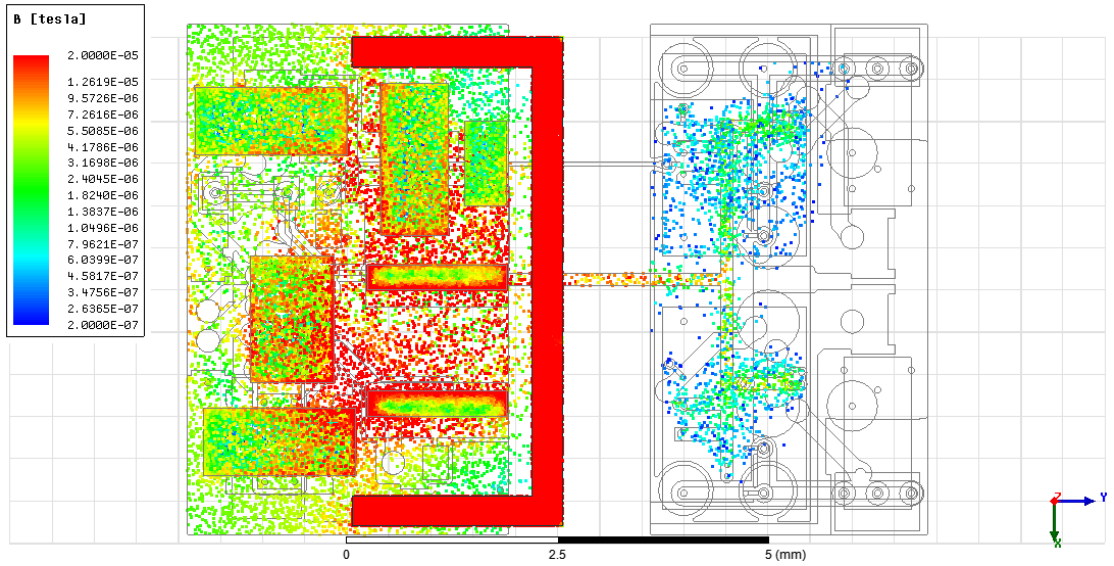
Rev. A

LTM8080: Noise Reduction with Magnetic Shield (Simulation)

LTM8080E01 w/o Magnetic Shield



LTM8080E01 w/ Magnetic Shield

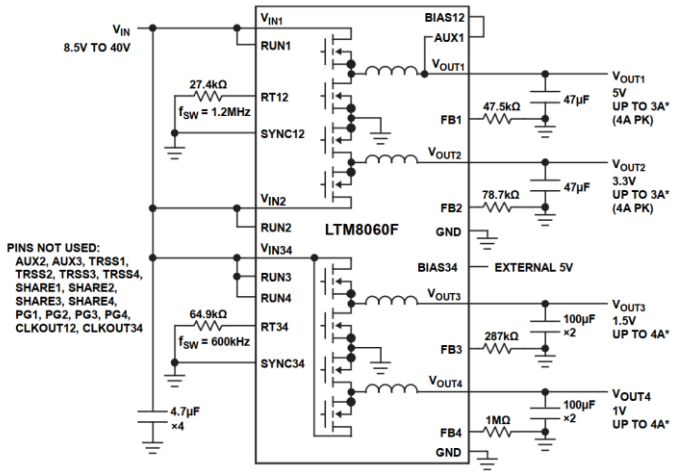


- Maxwell FEA (Finite Element Analysis) simulation 결과
  - Magnetic Shield가 Switcher → LDO로 유입되는 자기장 노이즈를 크게 저감 시킴

LTM8060F: µModule EMI Shield Advantages

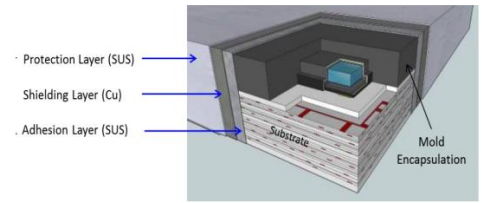
Package Level EMI Shield Advantages vs. Board Level EMI Shield

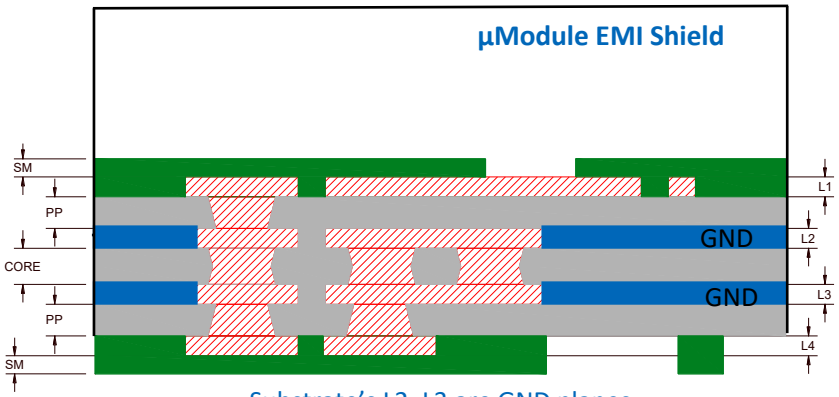
- 패키지 레벨의 EMI Shield는 보드 레벨 Shield 대비 소형/낮은 높이/경량/저렴함
- 생산 시 Clip&Cage 장착 공정이 불필요하게 되어 제조 단계 감소



Package Level Conformal Shielding

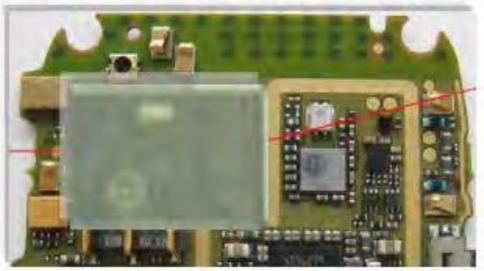
Structure





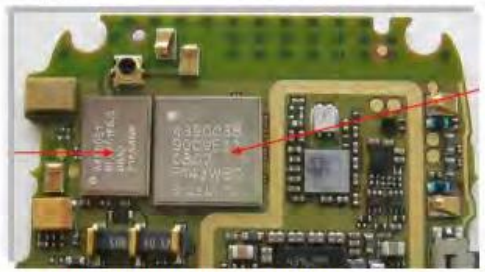
Substrate's L2, L3 are GND planes

Board Level Metal Lid Shielding



Applications: Transmit + TRX Module
Shielding: Stamped Metal Shield
Board real estate: ~301mm2
Total Height: ~1.8mm
Material cost: ~$0.2USD

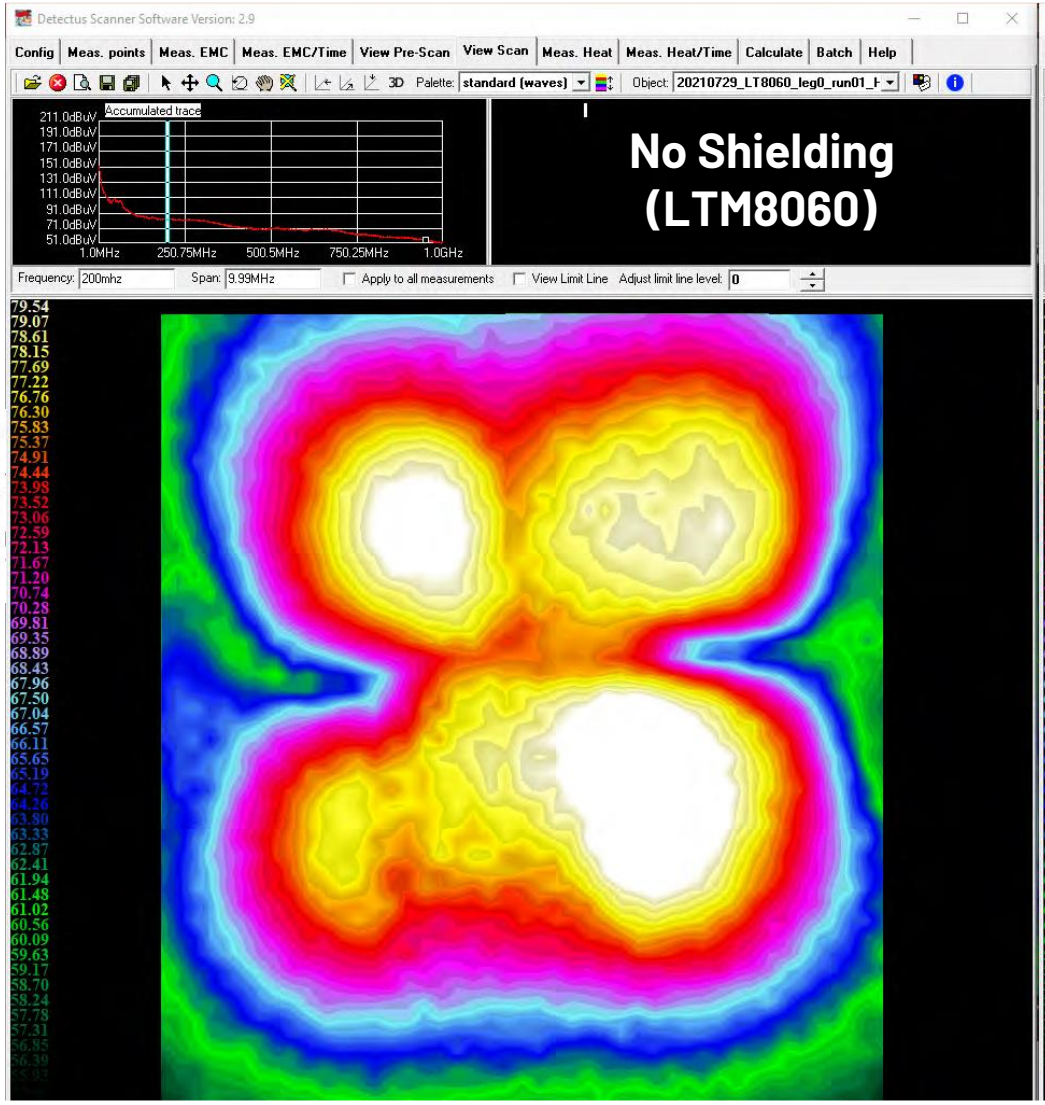
Package Level Conformal Shielding

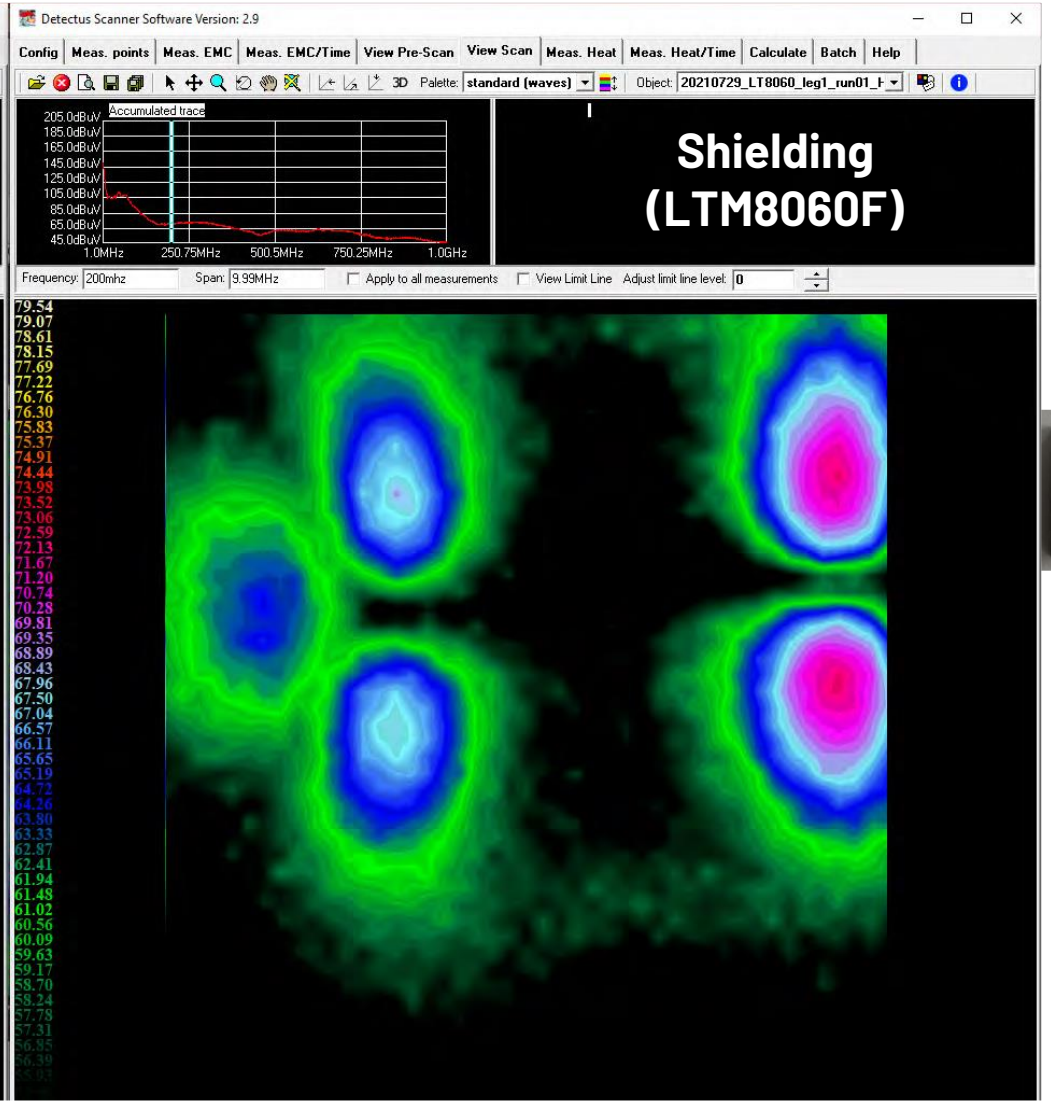


Applications: Transmit + TRX Module
Shielding: Conformal Shielding
Board real estate: ~175mm2
Total Height: ~1.2mm
Material cost: ~$0.07USD

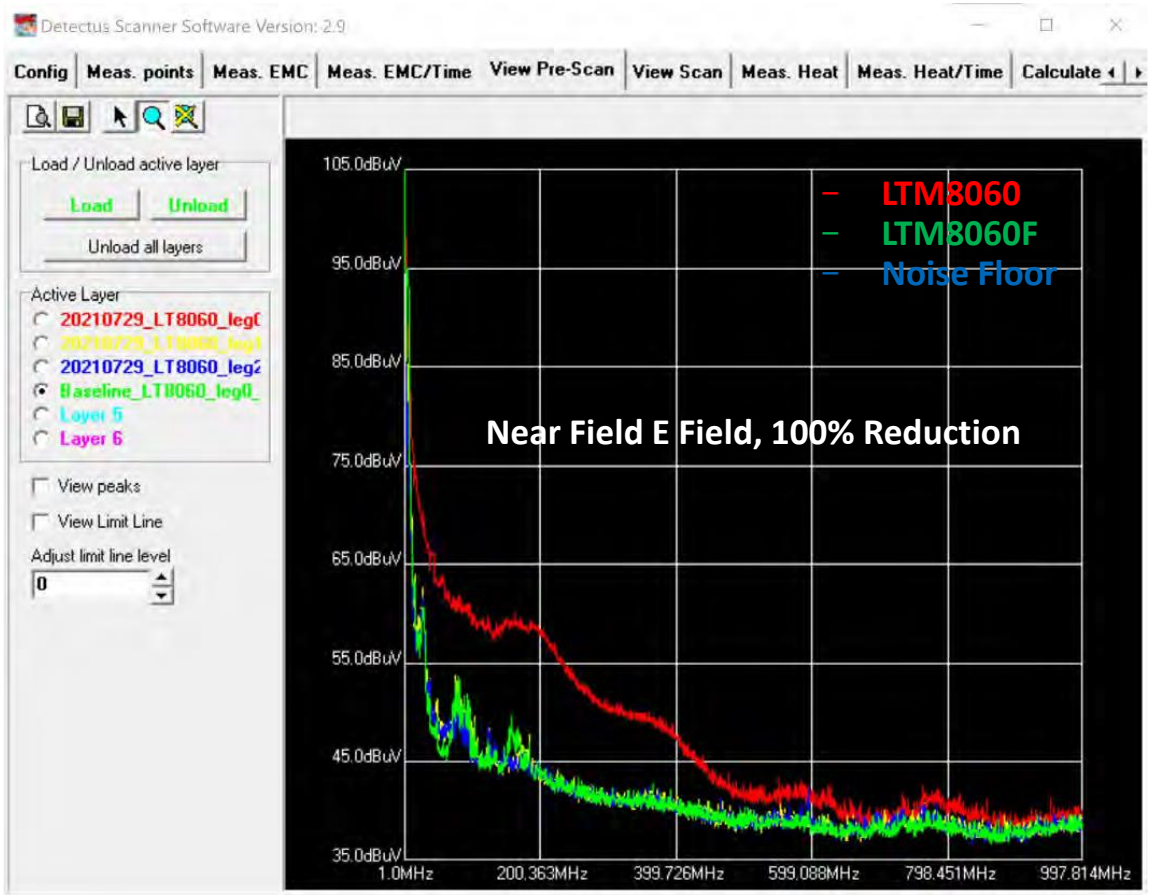
X-Y Form Factor → 42% smaller
Z Height → 33% thinner
Cost → 64% lower

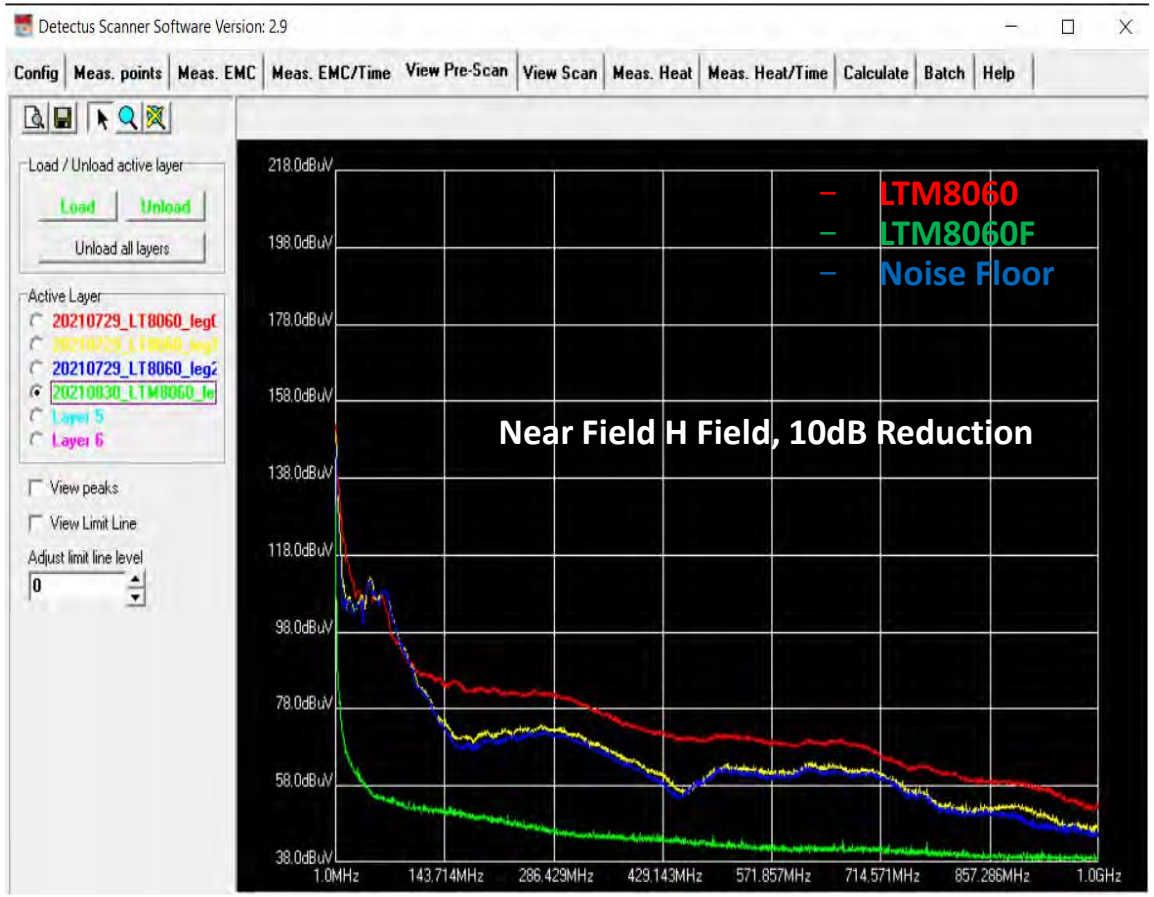
LTM8060F Near Field Scan and Test Conditions





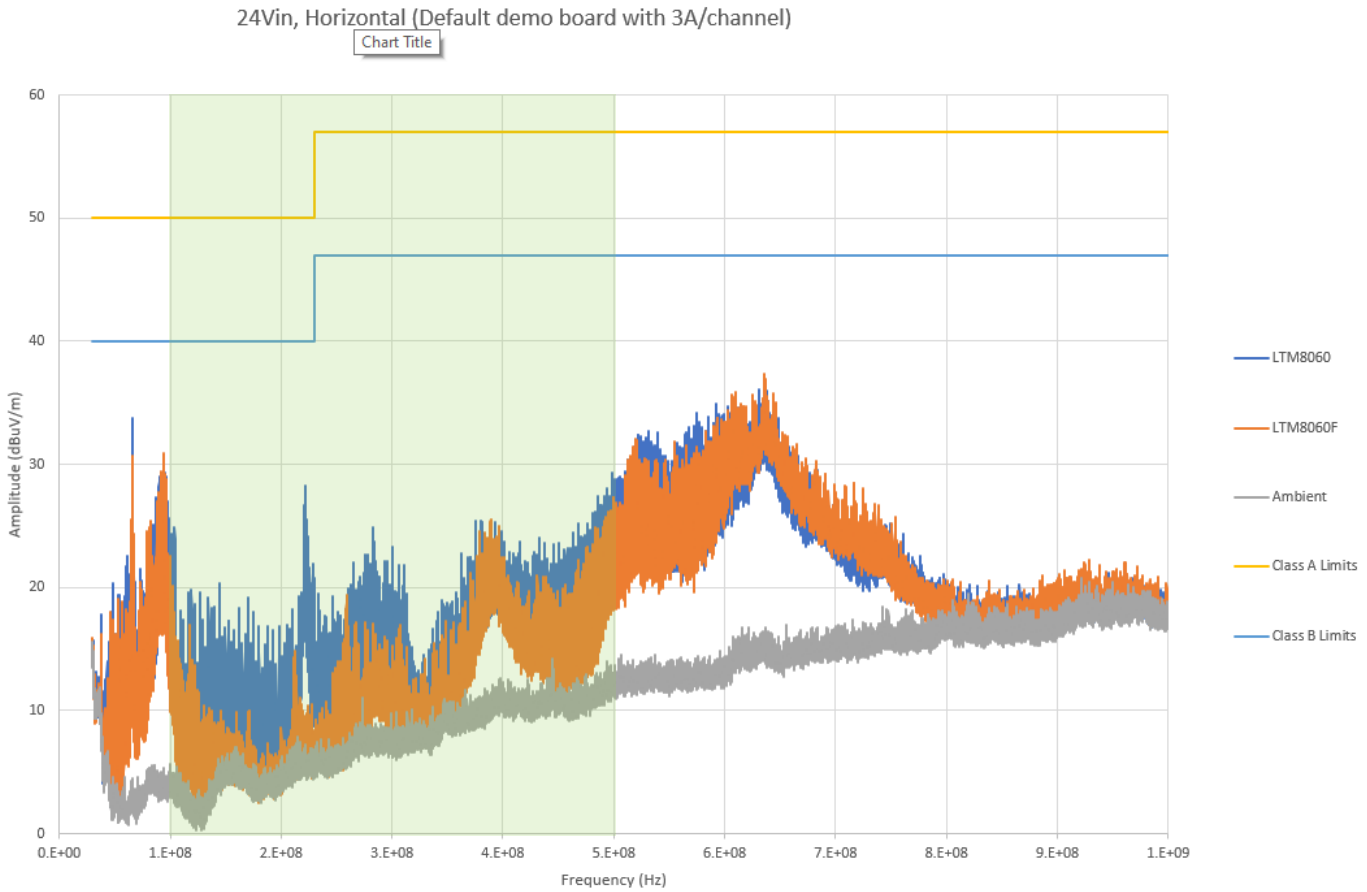
LTM8060F Near Field E Field & H Field





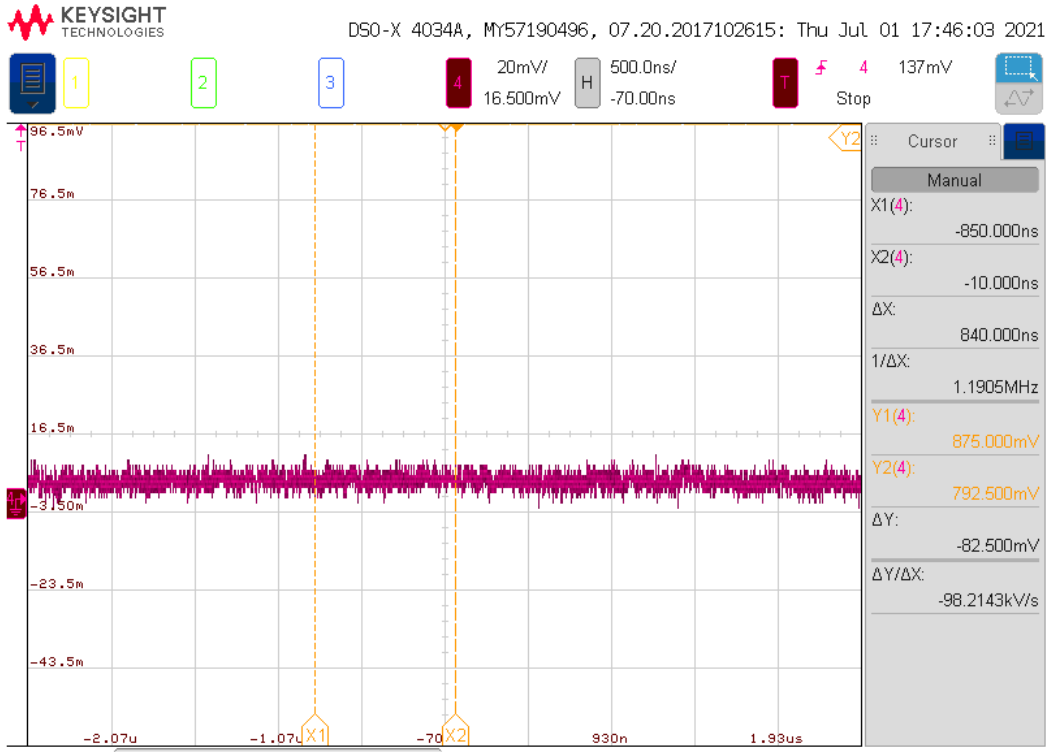
- LTM8060F는 1MHz ~ 1GHz 구간의 Near-field Electric Field 노이즈를 완전 제거
- LTM8060F는 1MHz ~ 1GHz 구간의 Near-field Magnetic Field 노이즈를 대폭 저감

LTM8060F Radiated EMI

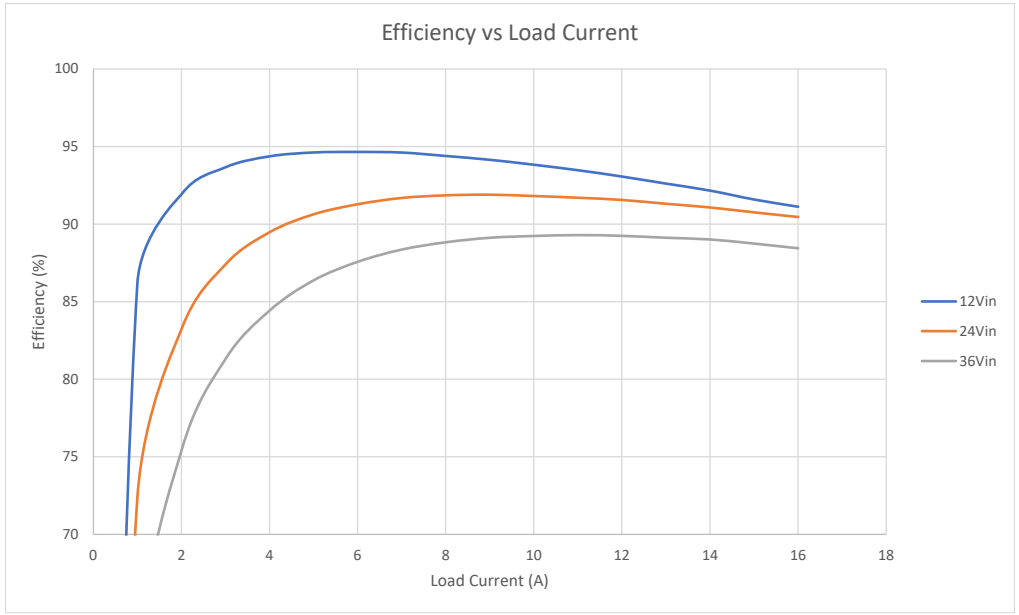


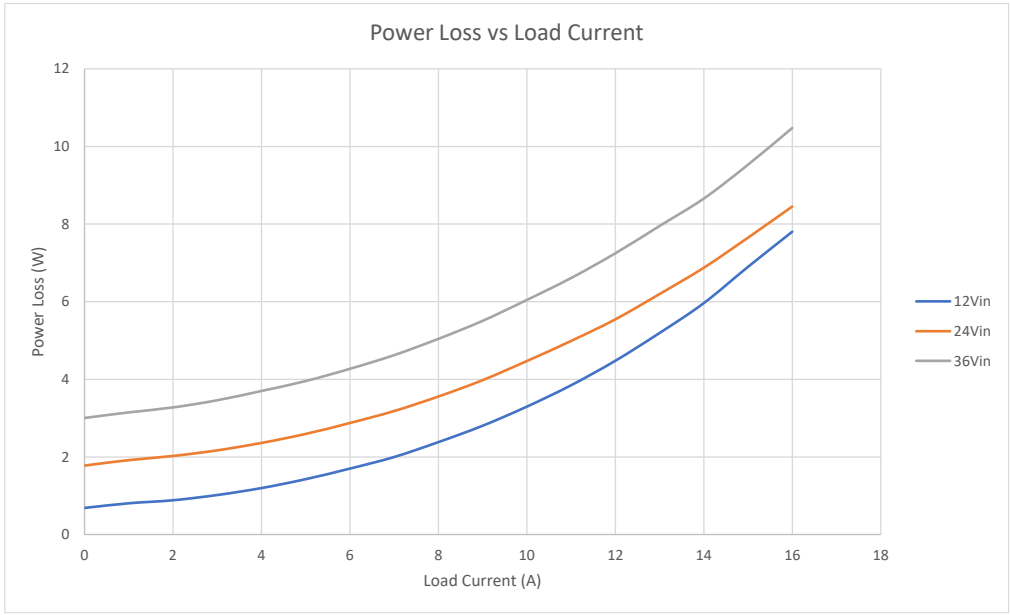
- LTM8060 대비 LTM8060F는 방사 EMI가 크게 감소하였으며, 특히 100MHz ~ 500MHz 대역에서 큰 개선 효과 확인

LTM8060F Scope Probing Noise, 100% Reduction

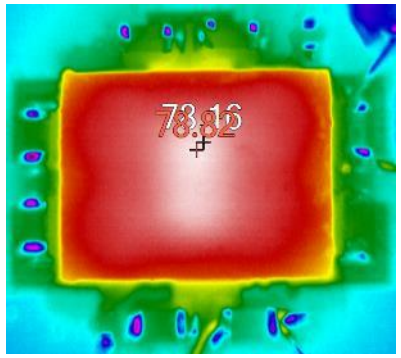


LTM8060F Efficiency, Loss, Thermal

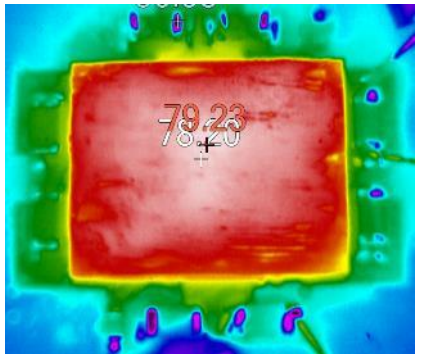




LTM8060 No Shielding



LTM8060F Shielding



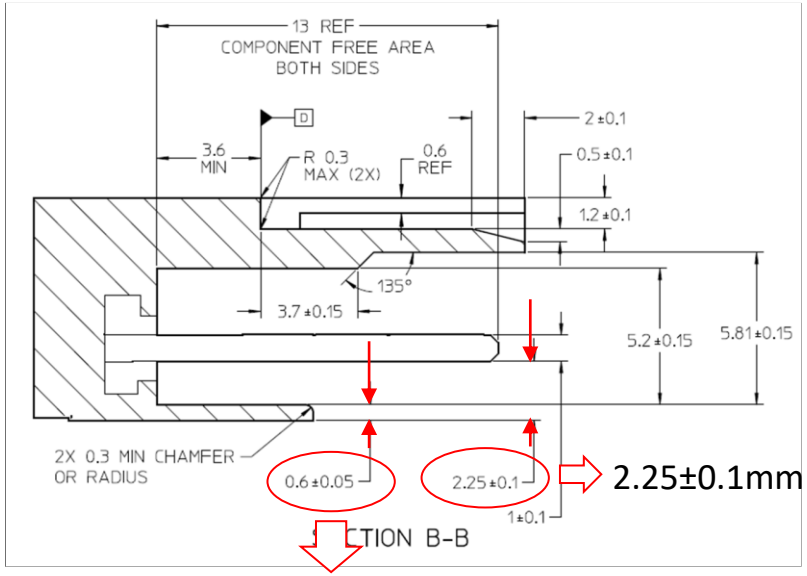
- LTM8060F는 LTM8060과 같은 효율, 전력 손실, 발열 특성을 지님

Thermal					
Vin	Vout	Iout	Vbias	Fsw	Runtime
14V	5V	12A	None	1.2MHz	~30mins

LTM8060F vs. LTM8060 Major Differences

Features	LTM8060F	LTM8060
Size	16mm × 11.9mm	16mm × 11.9mm
Height	**2.9mm**	3.3mm
Package	LGA(pre-soldered PSGA micro bump)	BGA
Electric Field Near Field Noise	**0**	Normal
Magnetic Field Near Field Noise	**10dB Lower**	Normal
External EMI Shield	**No Need**	Might Need
Efficiency, Thermal, Power Loss	Same as LTM8060	Normal

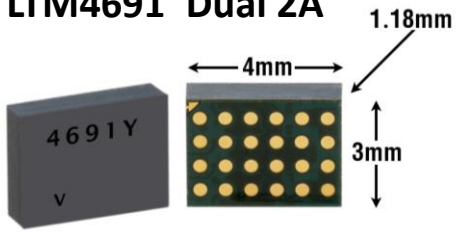
Ultra thin: 1.18mm & 1.4mm µModule for Optical Module

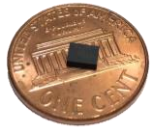


2.25±0.1mm

0.6±0.05mm

LTM4691 Dual 2A

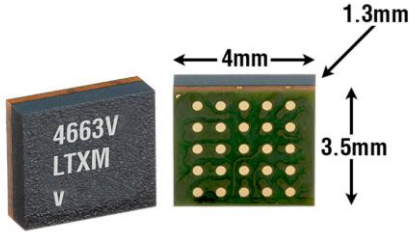




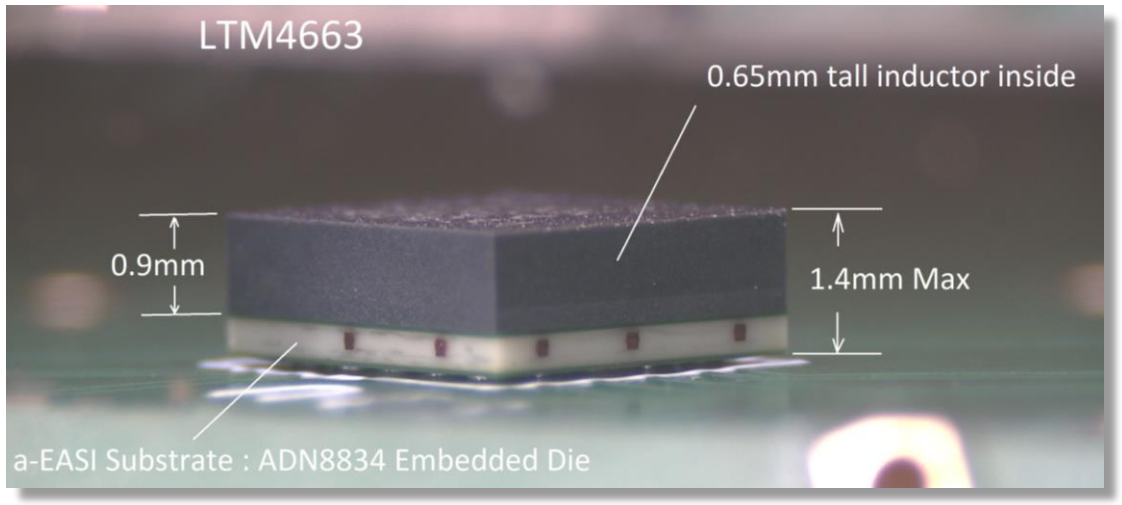
8.5mm for QSFP

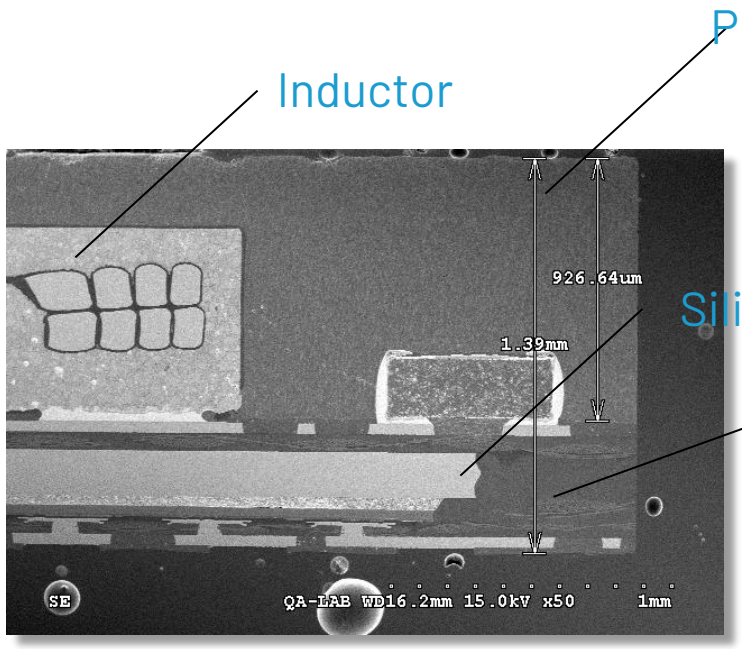
<1.4mm on back side of PC board

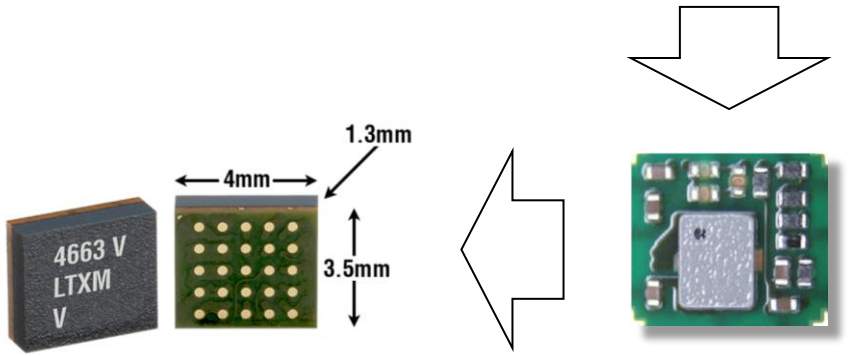
LTM4663 1.5A TEC



Thinner, Smaller: Embedded Si + Inductor on Top + Overmolded







Ultra thin Future: 1.2mm tall

ANALOG DEVICES

Data Sheet

LTM4723

Low V_{IN}, Ultrathin Dual 4A or Single 8A Step-Down DC-to-DC µModule Regulator

FEATURES

- Input voltage range: 2.25V to 5.5V
- Programmable 0.5V to 3.6V output
- Dual 4A or single 8A output current
- ±1.5% total output voltage regulation
- Current mode control, fast transient
- External CLK synchronization 1MHz to 3MHz
- 180° out-of-phase operation
- Output voltage tracking and soft start
- Burst selectable pulse-skipping/Burst Mode/forced continuous mode at light load
- Output voltage tracking

GENERAL DESCRIPTION

The *LTM4723* is a complete dual 4A output switching mode step-down dc-to-dc power supply in a tiny 4.25mm × 4.25mm × 1.35mm LGA package. Included in the package are the switching controller, power FETs, inductors, and **1.20mm** ting components. Operating over an input voltage range of 2.25V to 5.5V, the LTM4723 supports two outputs with a programmable output voltage range from 0.5V to 3.6V set by external resistors. Two outputs can be paralleled for a single 8A load. Only a few ceramic input and output capacitors are needed.

TYPICAL APPLICATION

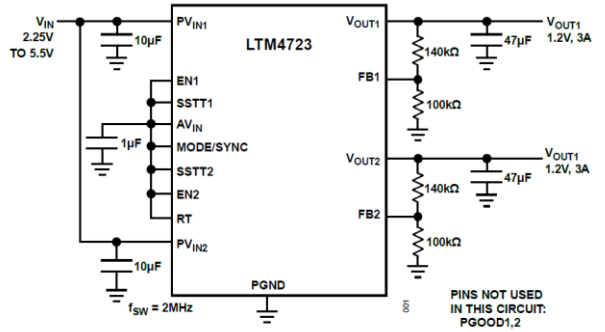
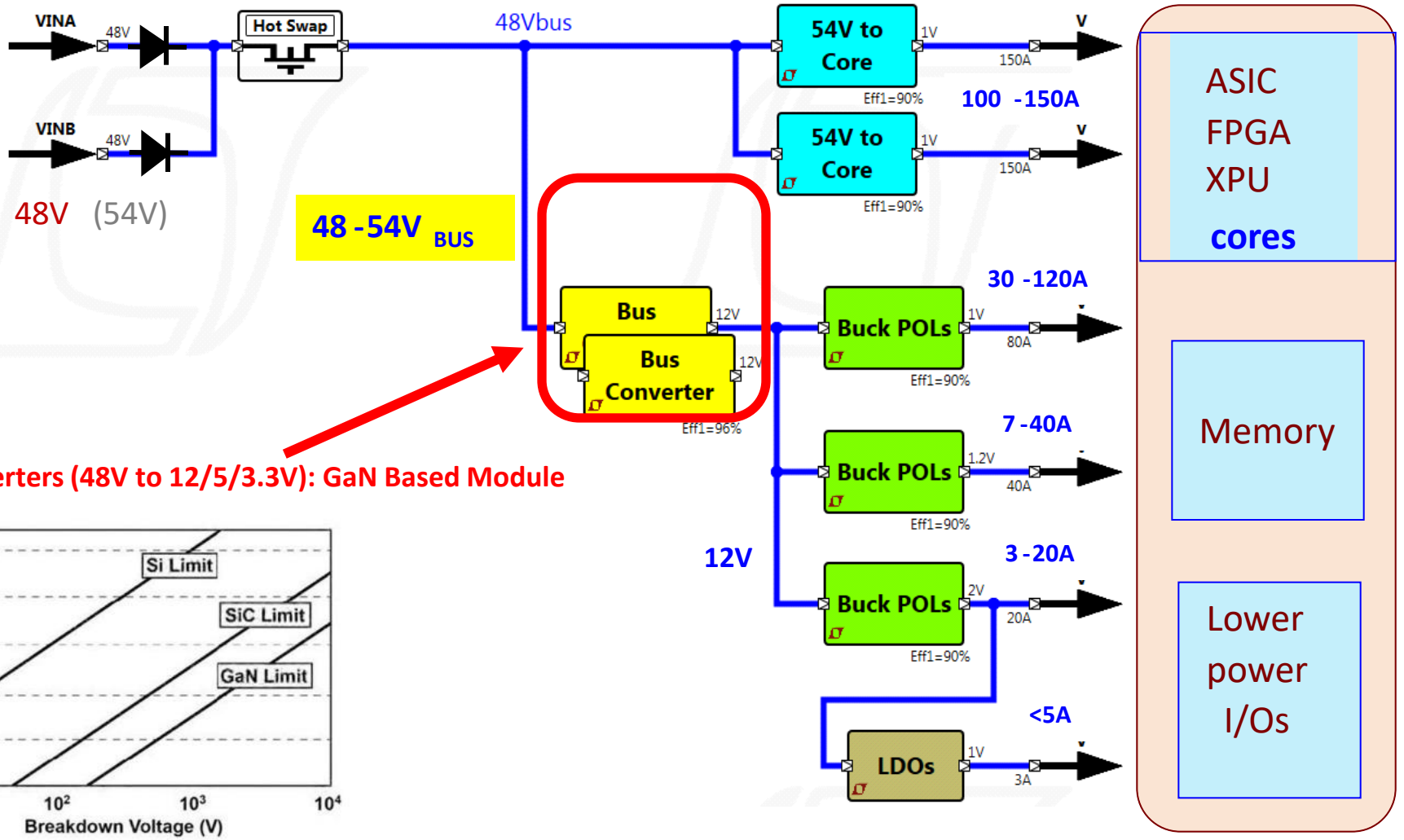


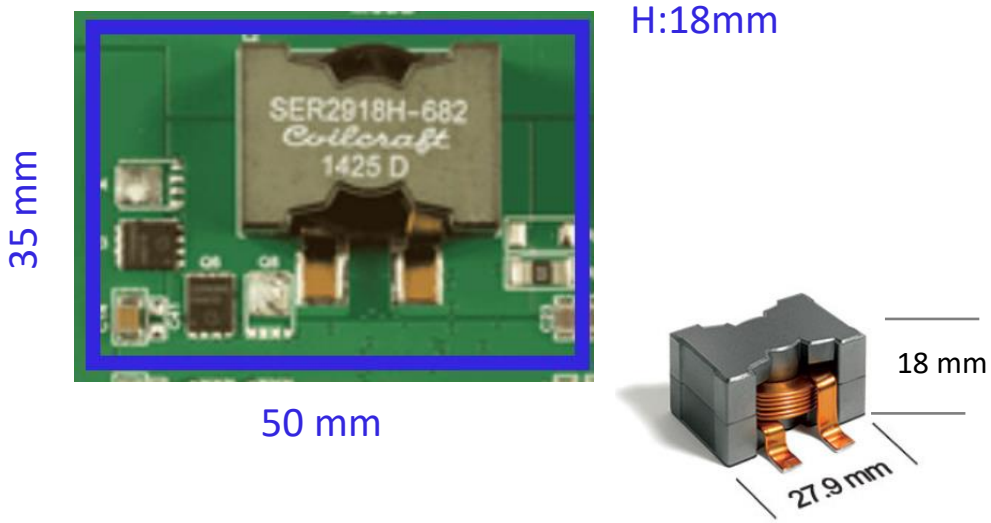
Figure 1. LTM4723 Dual 4A Step-Down µModule® Regulator

A Typical 48V System



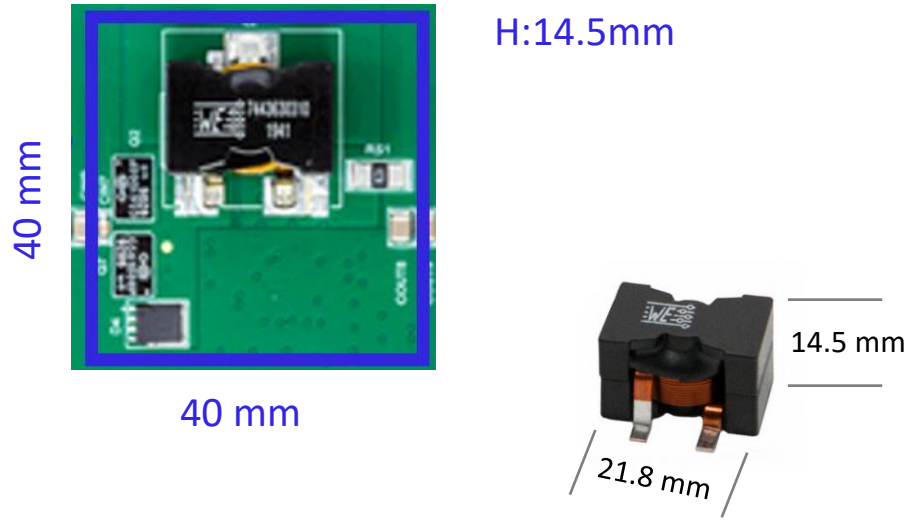
GaN Solution Power Density

LTC3892 (Si MOSFETs) demo board
(48VIN, 12Vout, 15A, 150kHz)



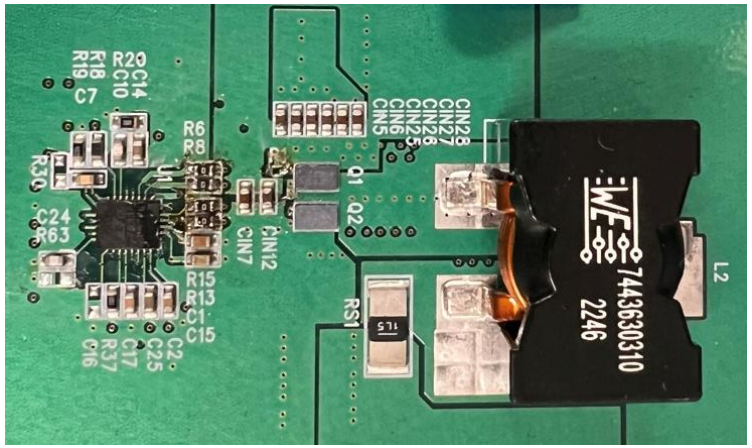
- **High switching loss**
- **Low switching frequency**
- **Bulky inductor!**

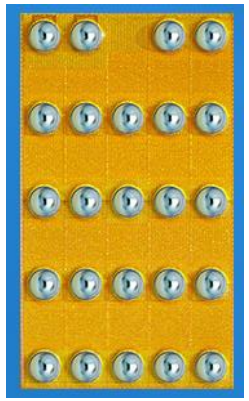
LTC7891 (GaN FETs) demo board
(48VIN, 12Vout, 20A, 400kHz)

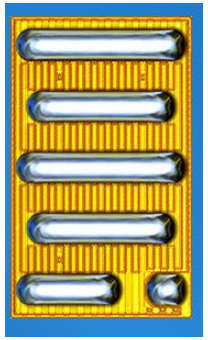


- **Lower switching loss**
- **Higher switching frequency**
- **Much smaller inductor!**

Design Challenges/Concerns with Discrete GaN





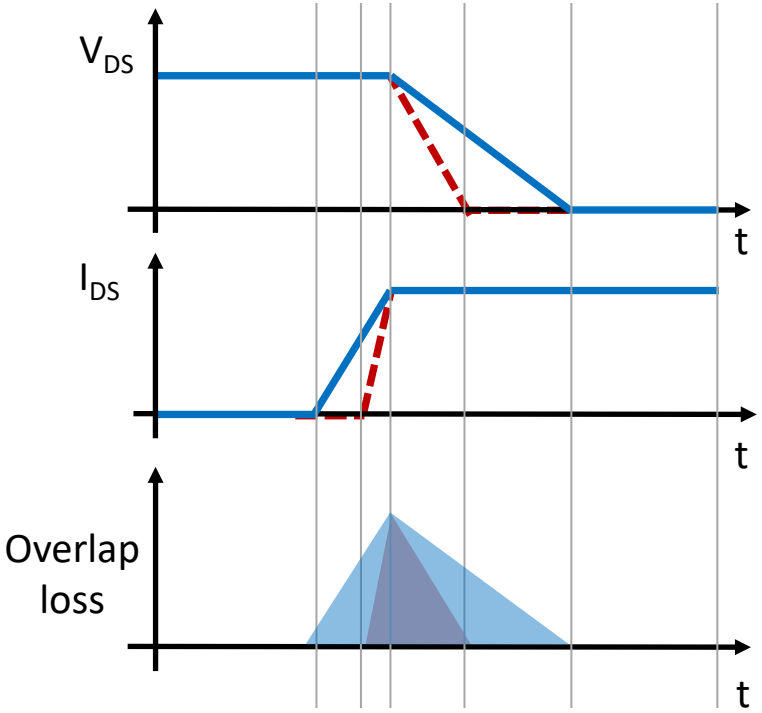


- **Assembly: Die on FR4 PCB:**
  - 기계적 신뢰성 문제 발생 가능
  - Underfill 공정 필요
  - 전류 밀도 및 열 스트레스 증가
- **PCB layout requirements:**
  - 높은 스위칭 주파수로 인한 까다로운 레이아웃 요구 조건
  - PCB 기생 임피던스에 매우 민감하게 반응
  - Hot Loop 면적을 최소화 해야 하는 숙제
- **Circuit design:**
  - 전압, 전류, 열 특성에 따른 디바이스 Derating
  - Dead Time 및 Driver 구동 최적화 필요

GaN FETs vs. Si MOSFETs in Hard Switching Buck

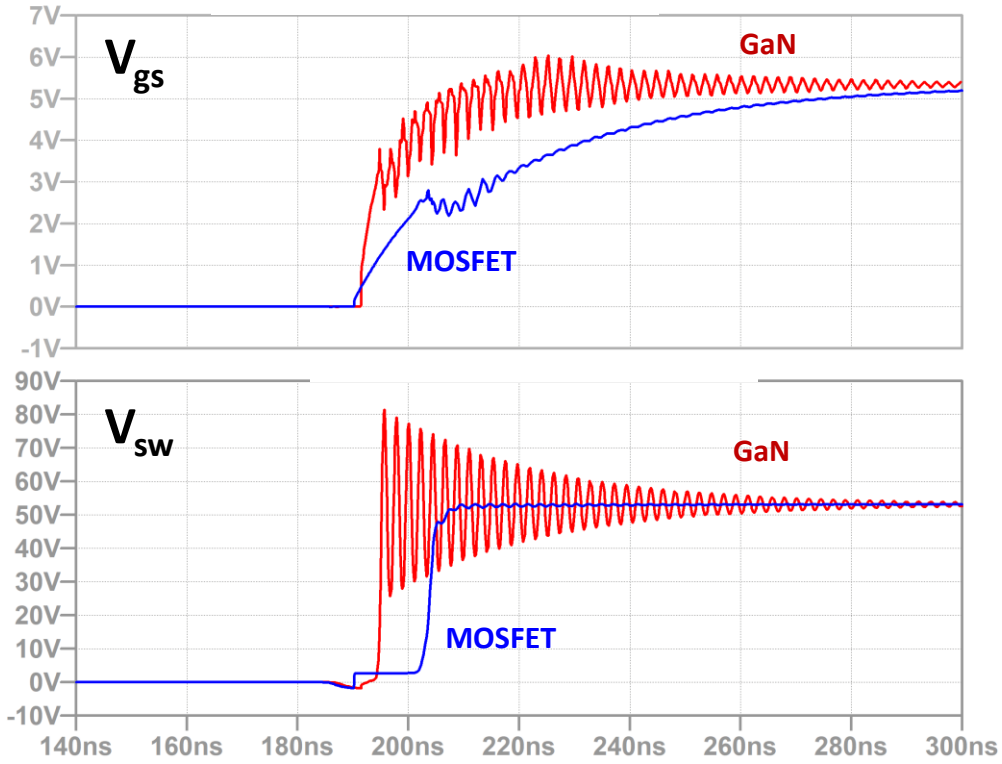
- **Lower switching loss**

GaN turn on/off faster



- **Higher risk of switching ringing**

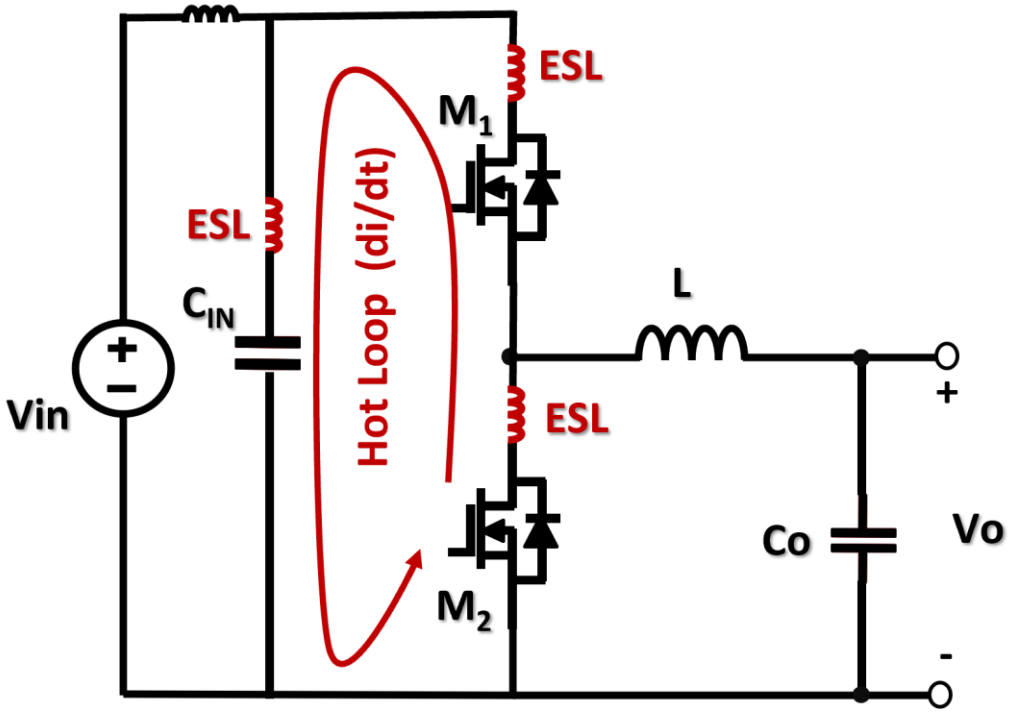
동일한 Hot Loop ESL 조건에서도 GaN 솔루션은 더 큰 Switching Ringing이 나타남

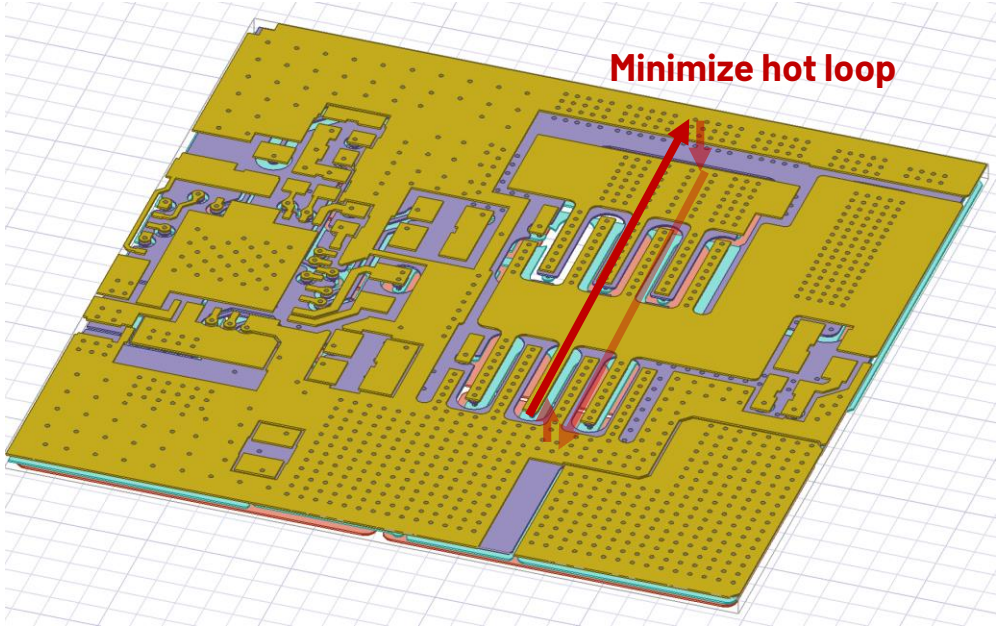


➢ **Hard Switching GaN 기반 컨버터는 레이아웃을 특히 주의 깊게 설계해야 함**

Layout Optimization: Minimize ESL in Hot Loop

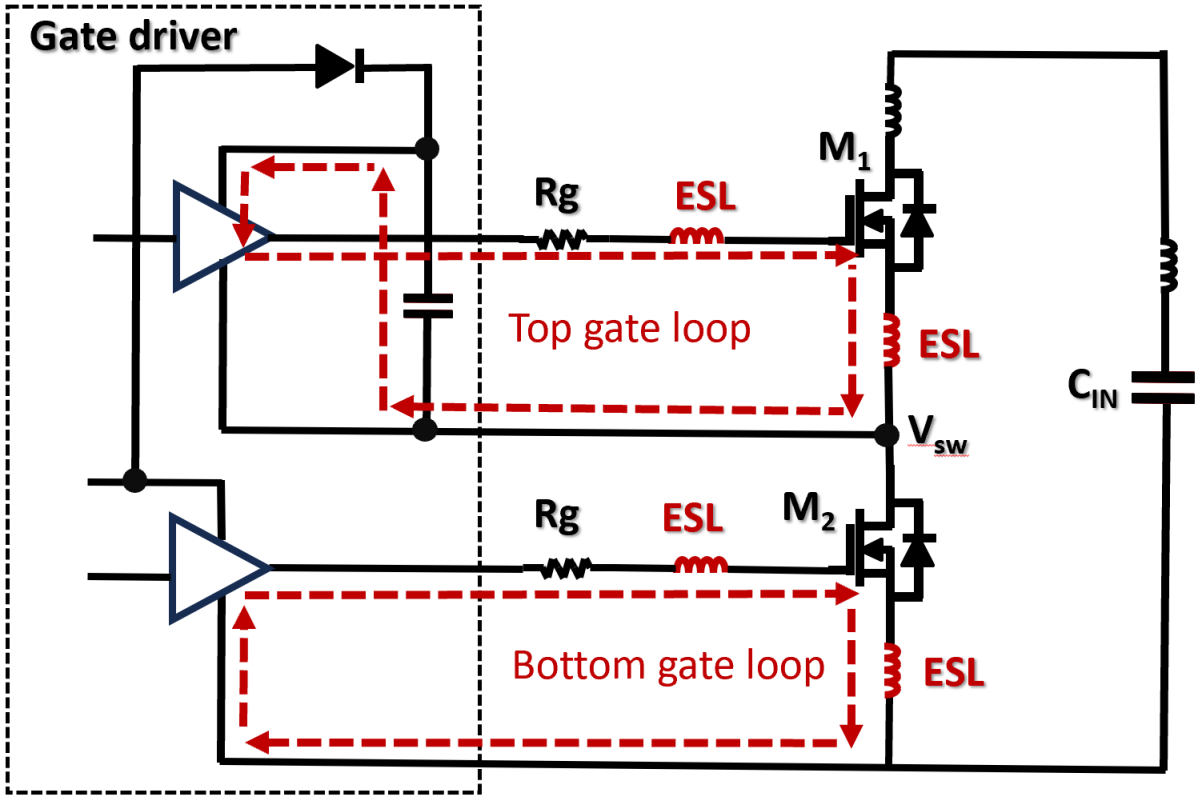
- Decoupling Capacitor를 GaN FET 바로 근처에 배치할 것.
- 전류 루프 면적을 최소화할 것.
- 충분한 개수의 Via를 사용할 것.
- Ansys Q3D를 사용해 루프 ESL을 검증할 것.

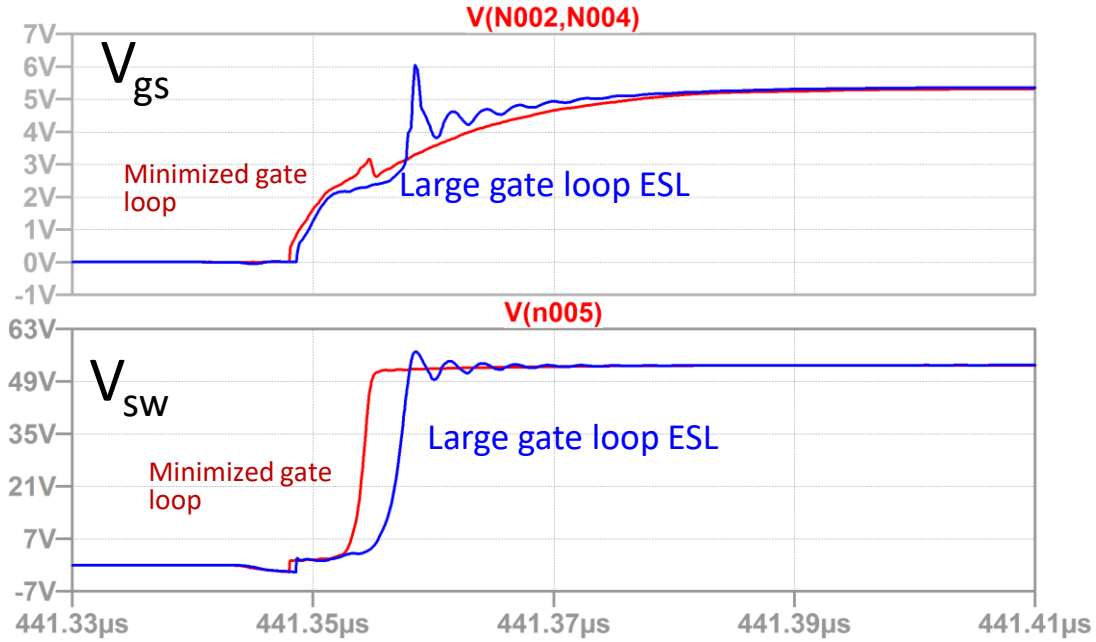


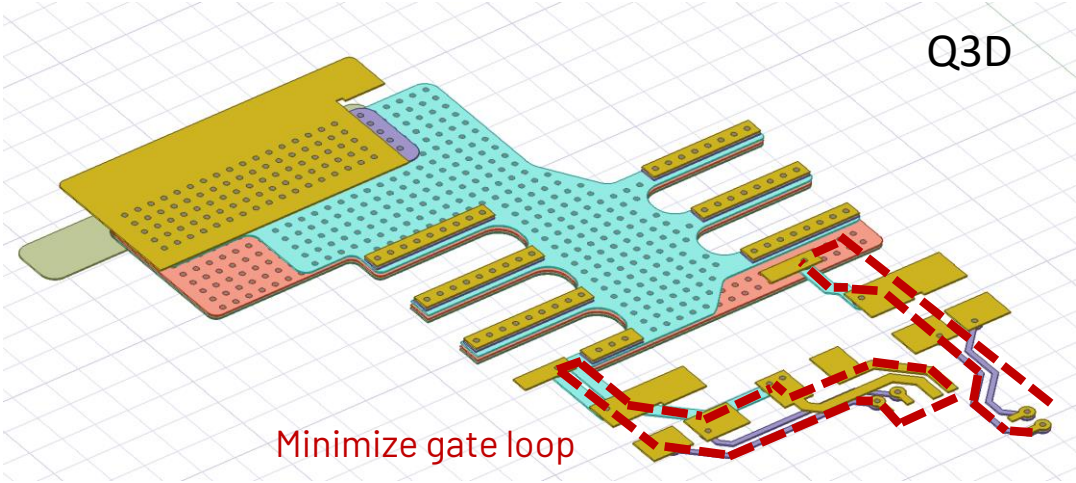


Layout Optimization: Gate Driver Loop Design

- Gate Driver 루프 면적을 최소화할 것.
- Gate Driver 경로를 파워 경로와 분리할 것.
- Ansys Q3D를 사용해 Gate Drive 루프 ESL을 검증할 것.

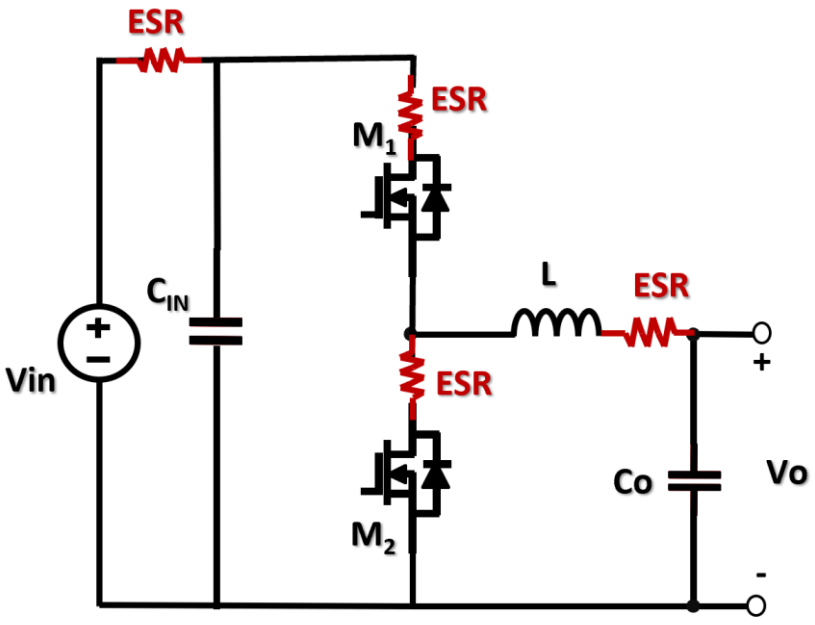


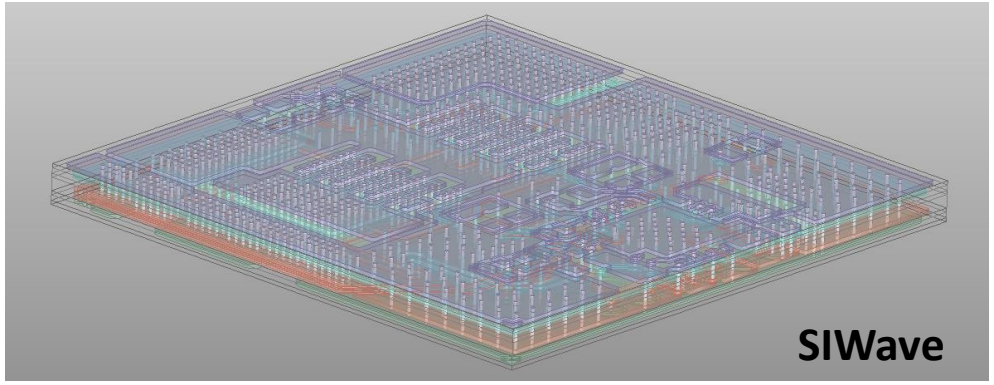


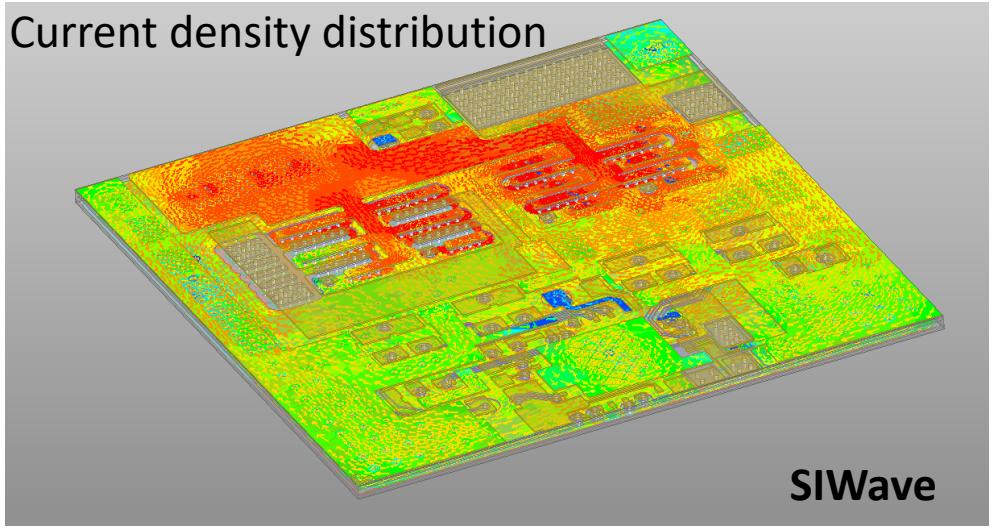


Layout Optimization: Minimize Substrate Power Loss

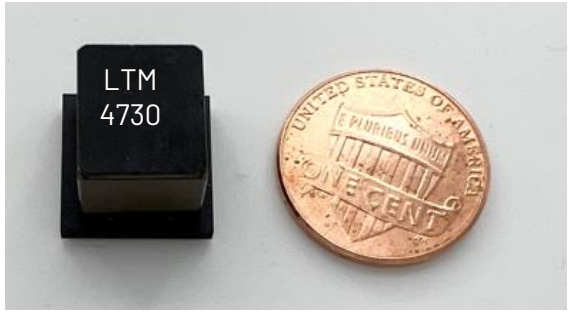
- 높은 전류 경로에 큰 ESR이 존재하면 기판(Substrate)에서 상당한 전력 손실이 발생할 수 있음.
- Ansys SIWave를 활용해 고전류 집중 구간을 찾고, 기판에서 발생하는 전력 손실을 분석할 것.

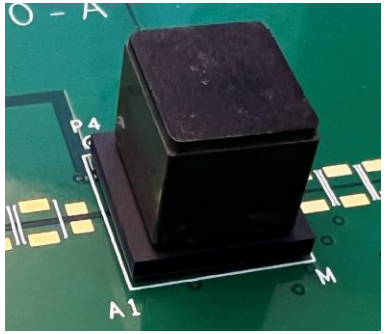


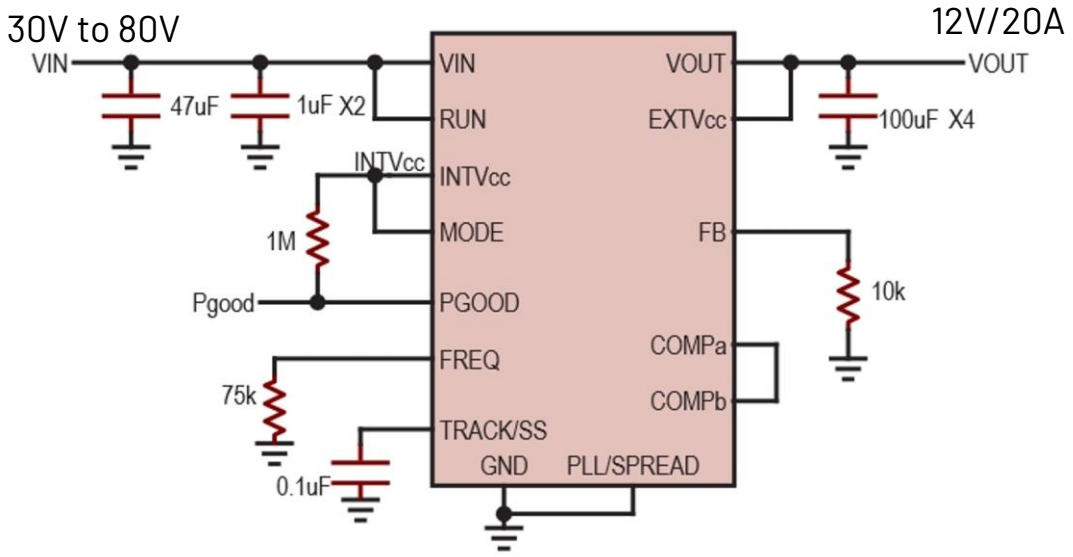




80V/20A GaN-Based µModule Regulator (LTM4730)







FEATURES

- Input Voltage Range: 30V to 80V
- Wide Output Voltage Range: 5V to 36V
- Tightly regulated and adjustable Vout
- 97% Efficiency (48VIN, 12VOUT, 20A)
- Scalable: Parallel for higher power
- Current mode control for easy current sharing
- 13mm x 13mm x 11.7mm BGA Package

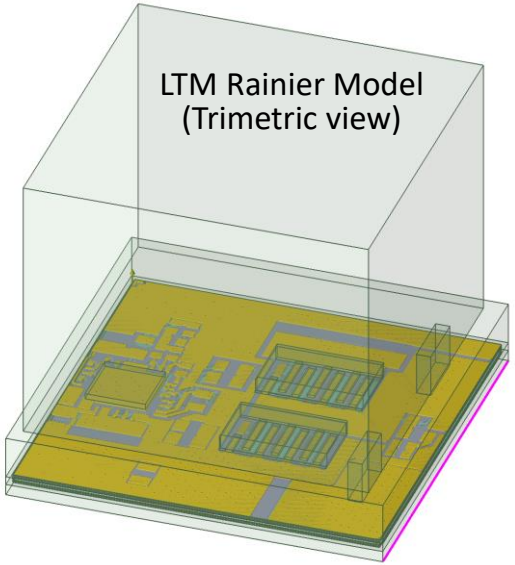
APPLICATIONS

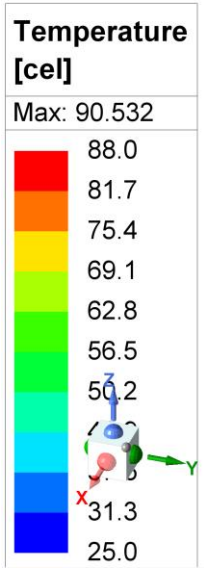
- Telecom, Datacenter, Industrial, and ATE
- High-reliability applications
- Broad markets

STATUS

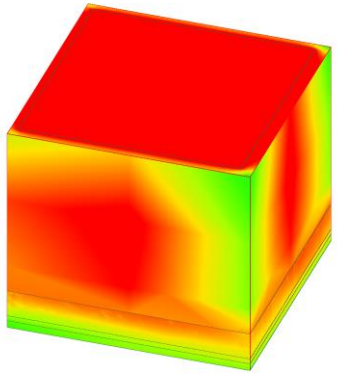
- Sample: 02/2026
- Production: 10/2026

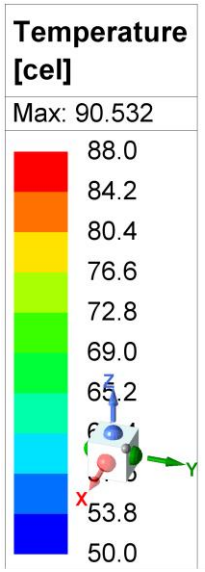
Package Thermal Verification via Icepak Simulation



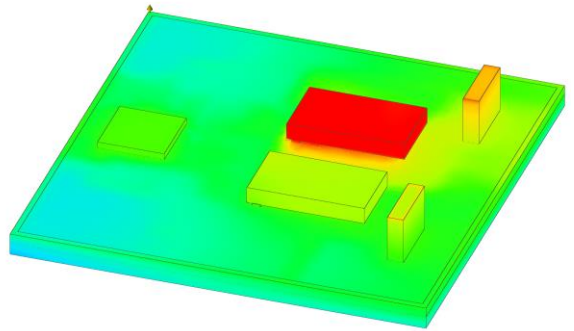


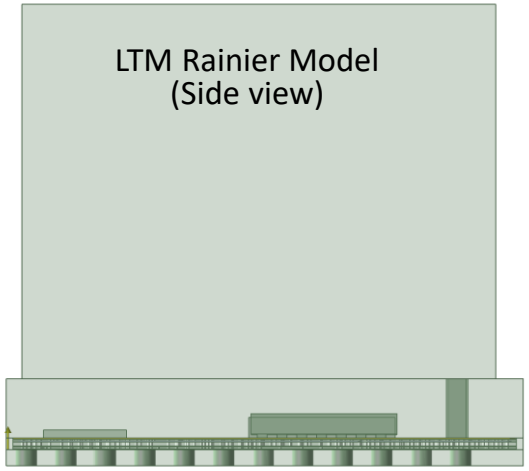
Case temperature

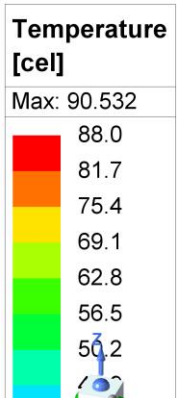




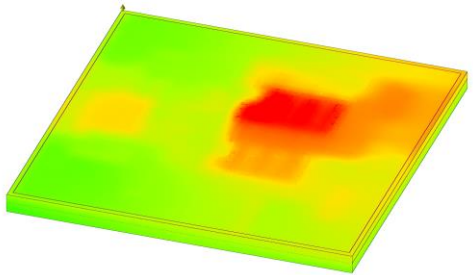
GaN FETs temperature







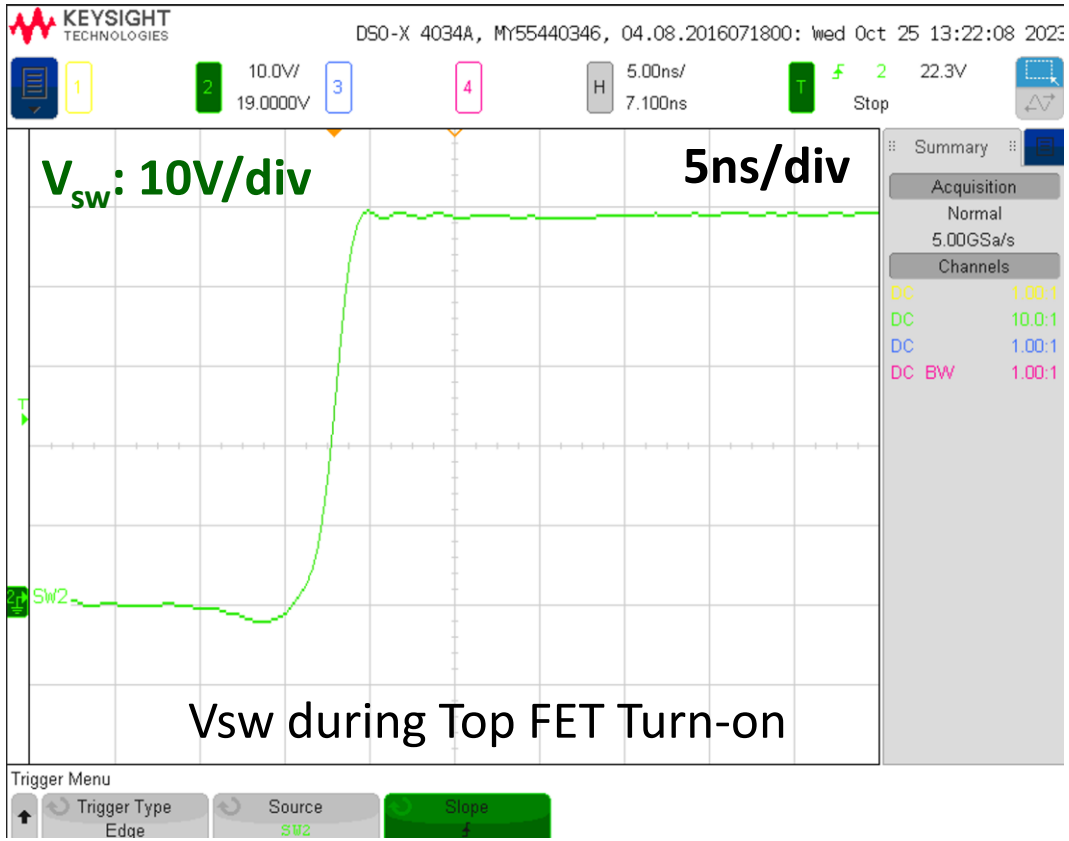
Substrate temperature

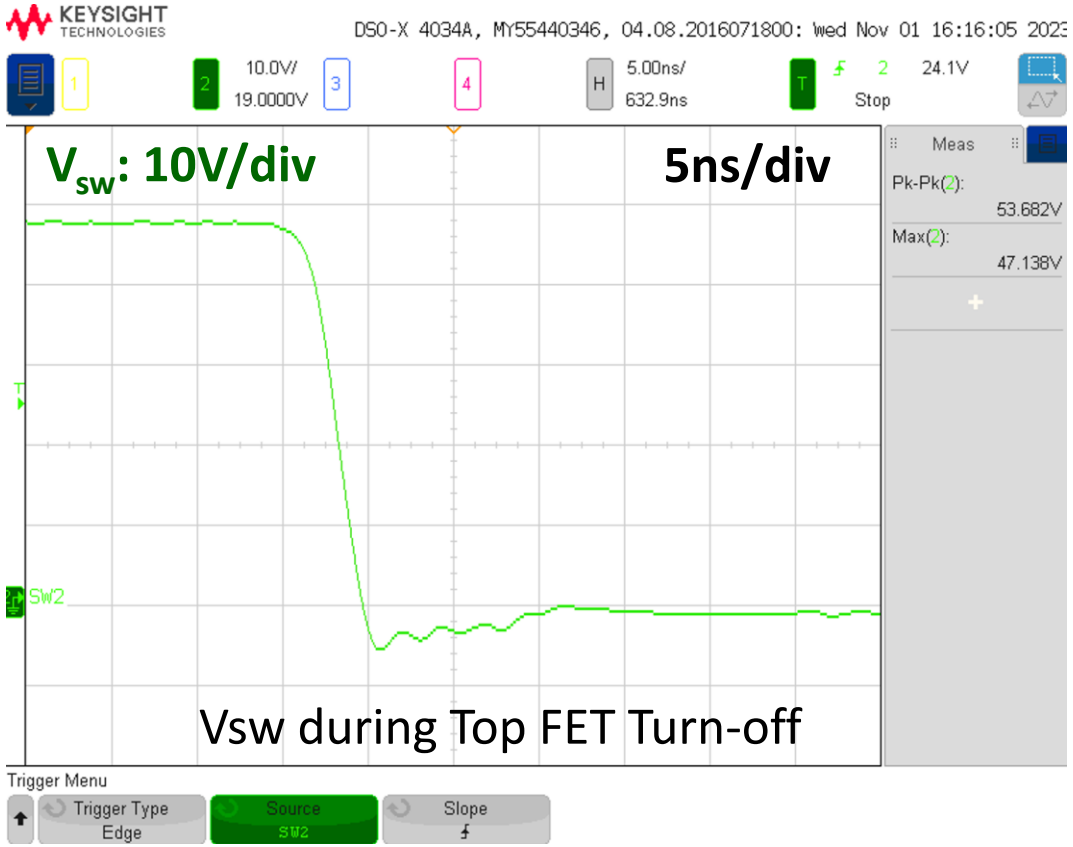


BGA ball temperature

Clean Switching Node Waveform

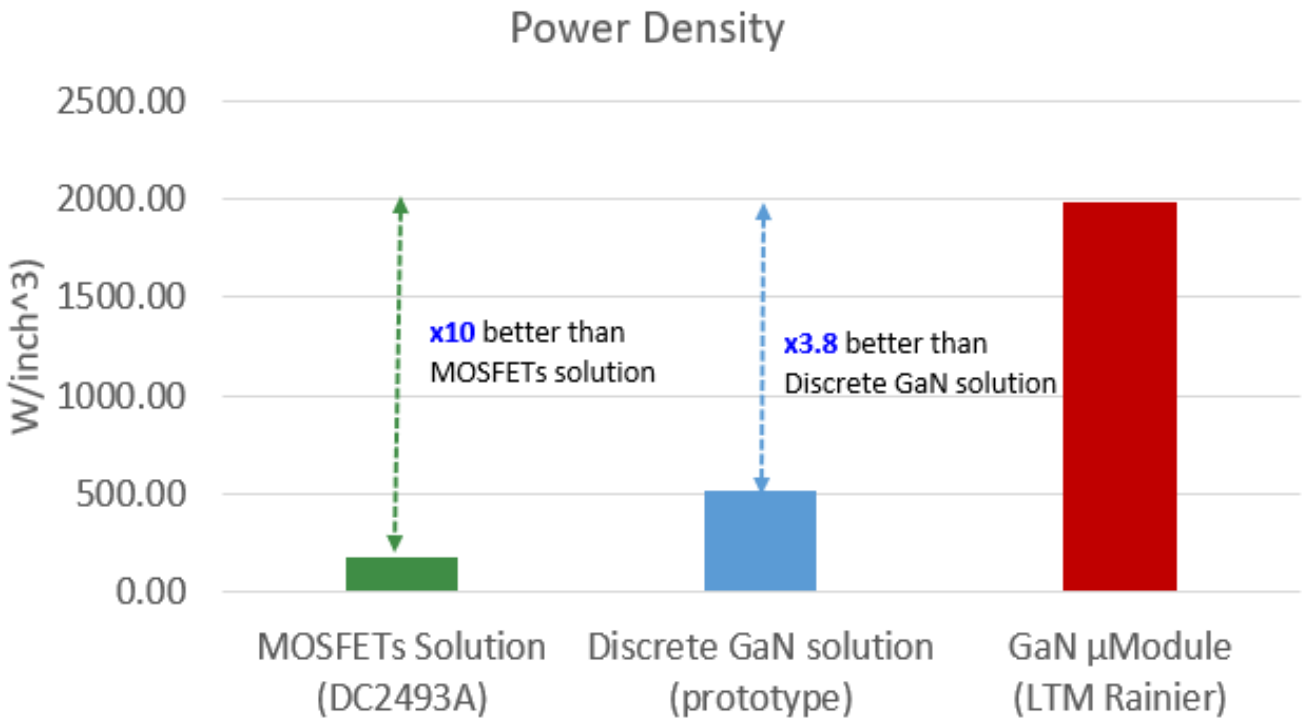
- Test under 48Vin, 12Vout@20A, fsw 400kHz

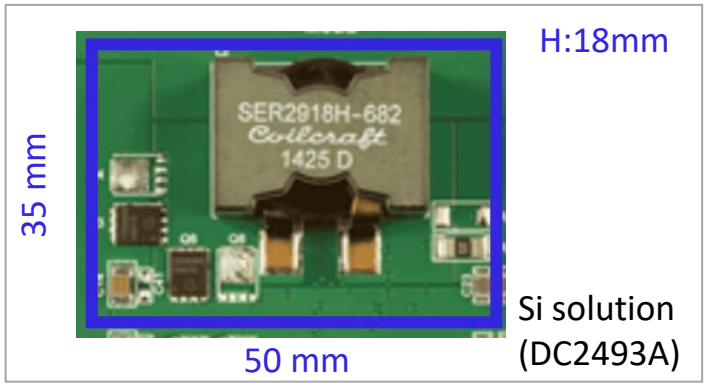


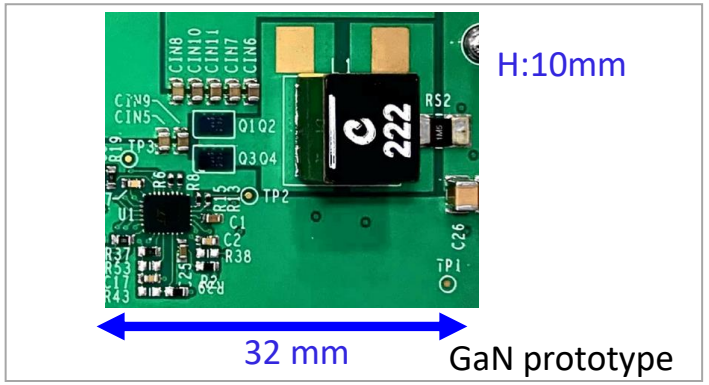


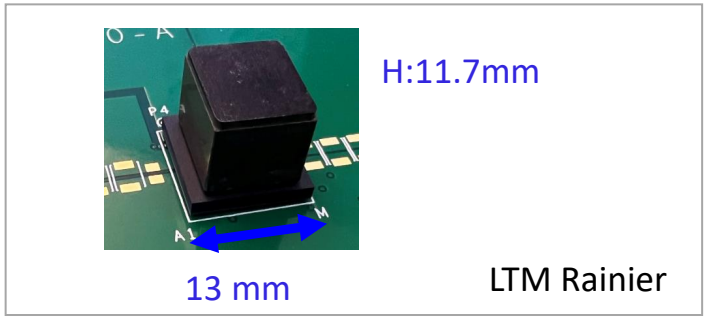
LTM4730 Gets High Power Density

- LTM4730 has **x10** power density than Si solution
- LTM4730 has **x3.8** density than discrete GaN solution

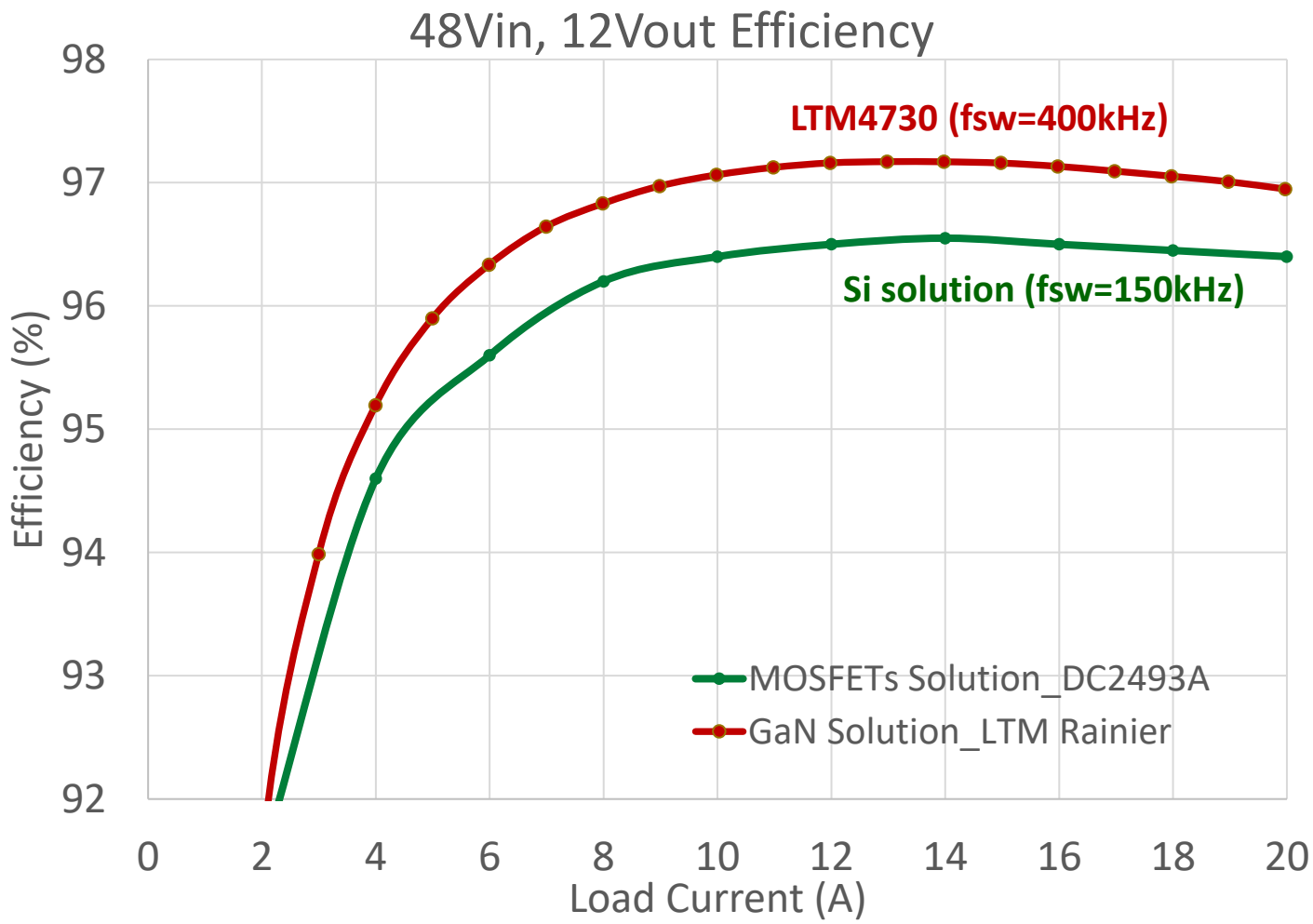




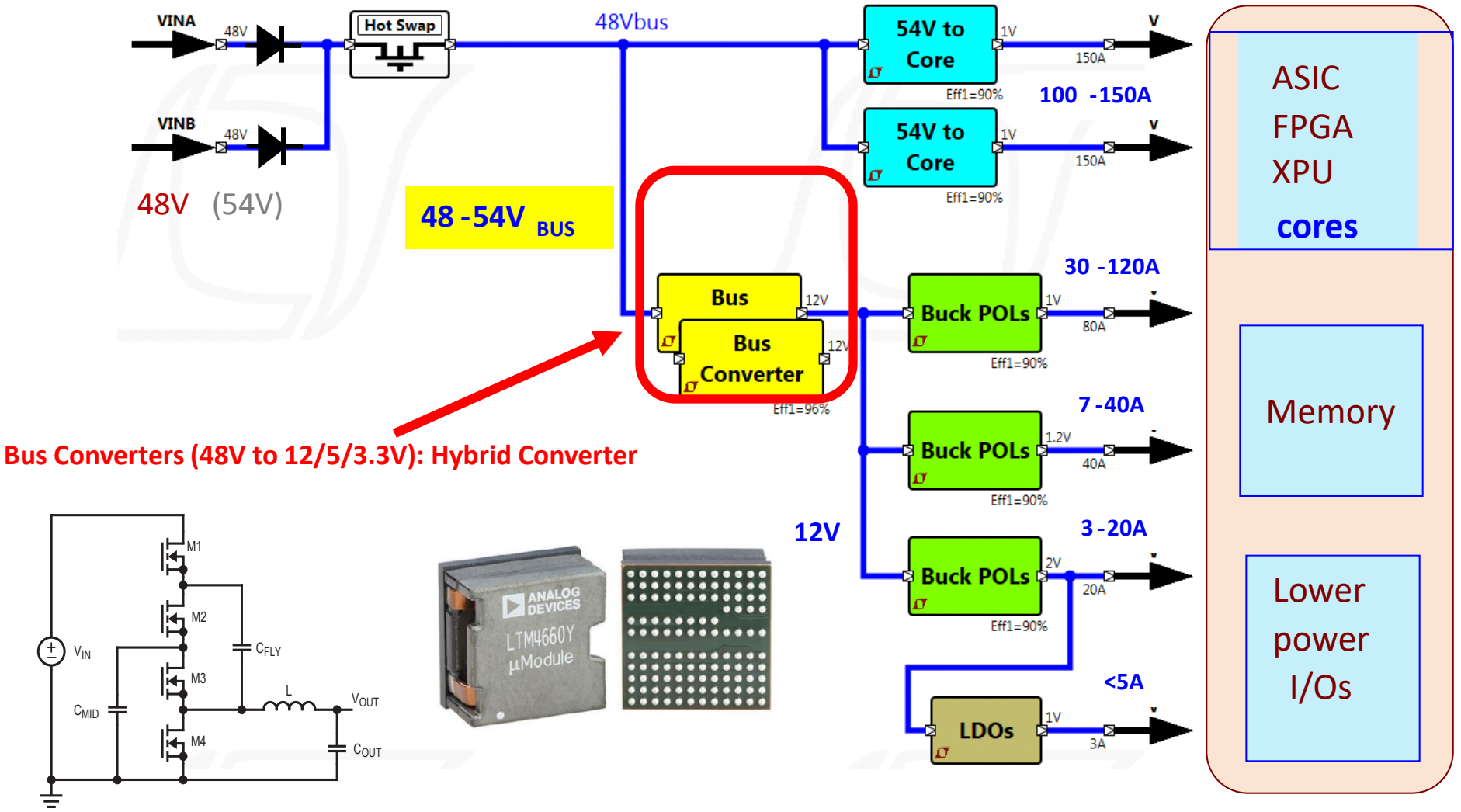




LTM4730 Gets High Power Efficiency

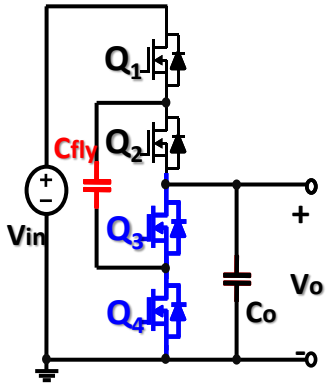


A Typical 48V System

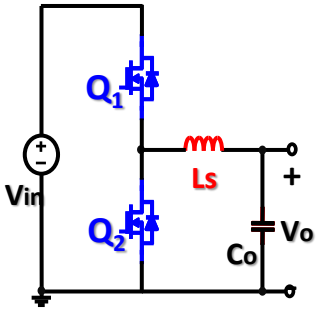


LTM4660 Hybrid Converter

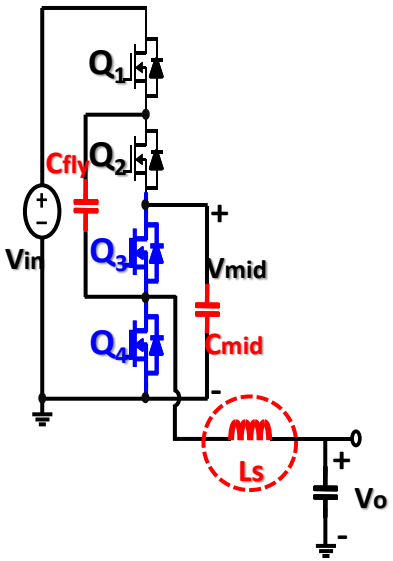
Switched Capacitor



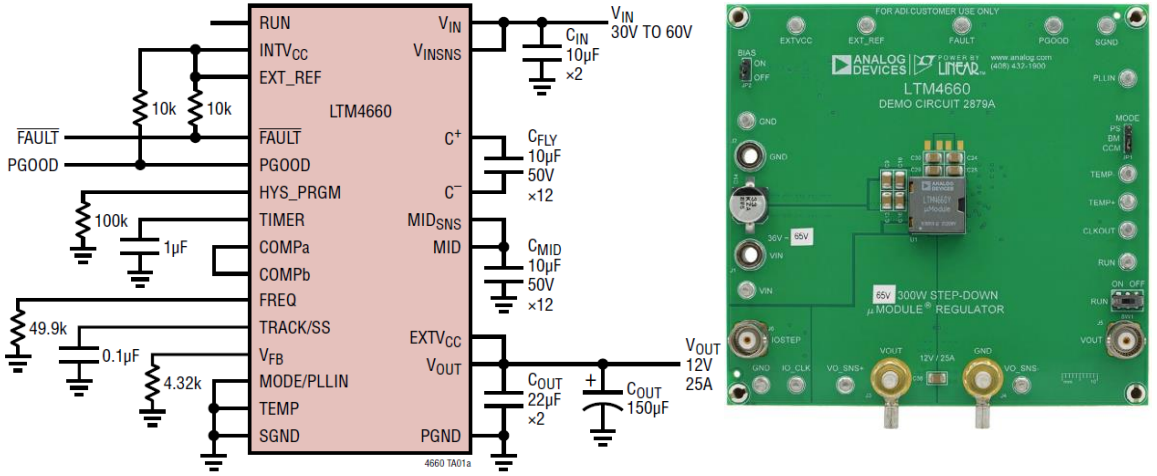
Synchronous Buck



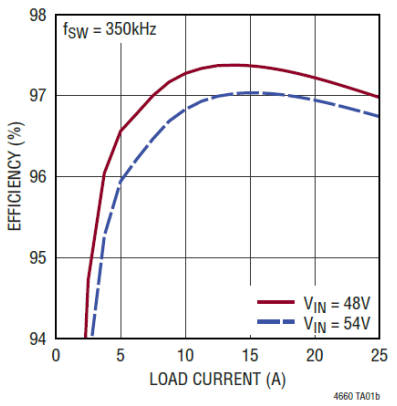
Hybrid Converter



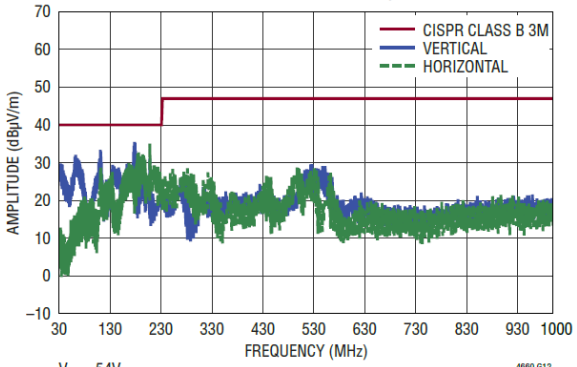
12V, 25A DC/DC µModule Nonisolated Bus Converter



Efficiency vs Load Current
V_{OUT} = 12V



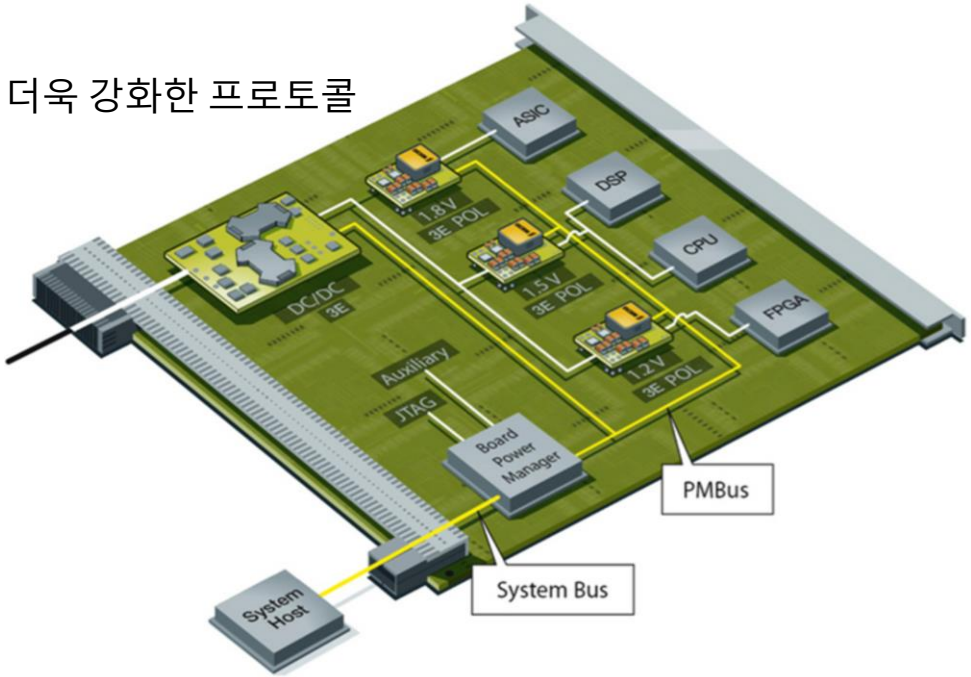
Radiated EMI Performance (CISPR22 Radiated Emission Test with Class B 3m Limits)

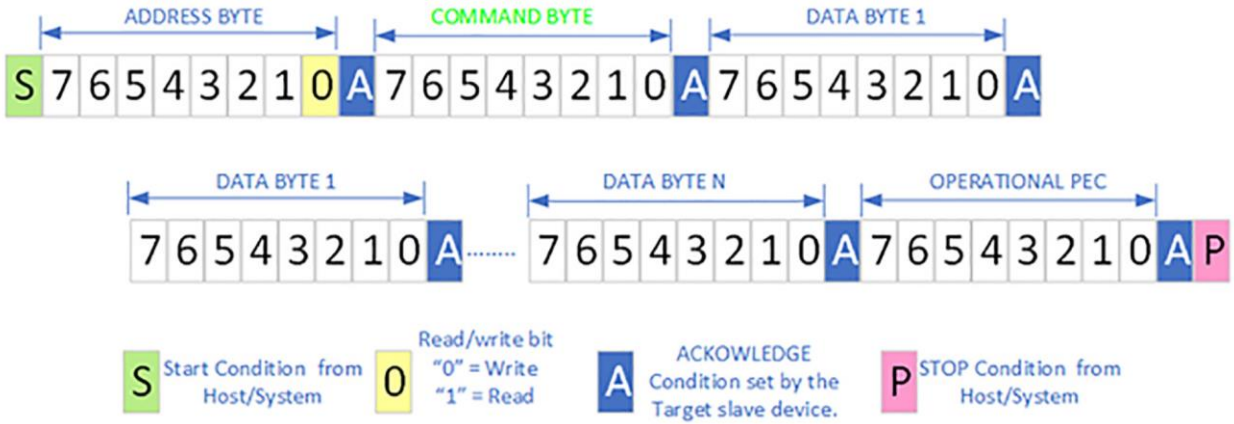


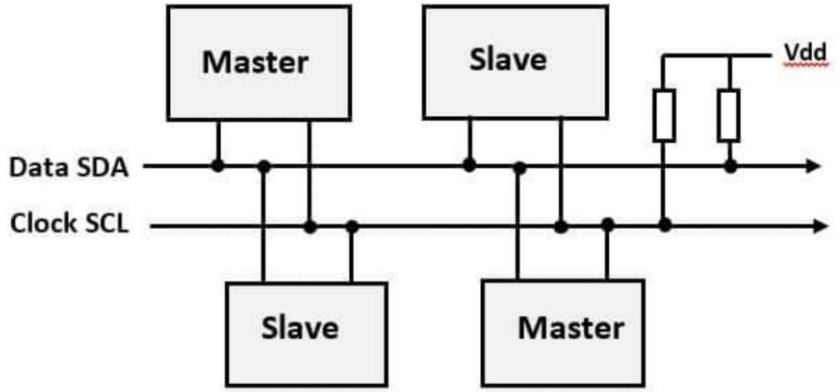
VIN = 54V
VOUT = 12V
POUT = 300W, fSW = 350kHz
DC2879A, MEASURED IN A 3m CHAMBER, PEAK DETECT METHOD

What is PMBus

- PMBus는 전원 관리(Power Management)를 위한 I2C 기반 통신 표준
- PMBus는 SMBUS(System Management BUS)를 확장한 형태로, 전원 관리에 필요한 기능을 더욱 강화한 프로토콜
- PMBus 통신은 2개의 신호선을 사용
  - SDA(Serial Data)
  - SCL(Serial Clock)
- PMBus는 최대 1MHz의 Interface 속도를 지원합니다.
- PMBus Data Packet 구조
  - 7bit address + 1bit Read/Write bit
  - 이후 8bit command Byte(명령 코드 포함)
  - 그 뒤 하나 이상의 8bit Data Byte 전송

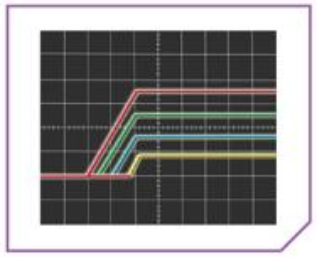






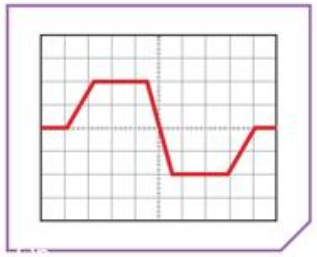
PMBus: Less Power Usage and Better Power Control

- PMBus는 설계를 단순화하고, 소프트웨어 부담을 줄이며, 실시간 진단 및 데이터 수집 기능을 제공하여 데이터 수집과 전력 사용 효율(PUE, power utilization effectiveness)을 개선하는데 도움이 됨
- PMBus는 다음과 같은 기능을 제공



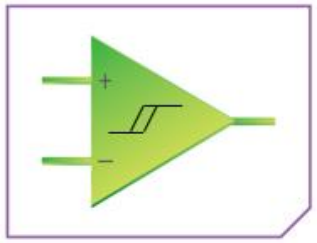
Sequence

Turn on managed power supplies in an order and with timing defined by the user.



Trim (Servo) and Margin

Servo loop digitally adjusts output voltage to a user-defined target or setpoint to tight DC accuracy. Margin-test system by adjusting output voltage.



Monitor Telemetry

Readback voltage, current, power, temperature, status.

Manage Faults

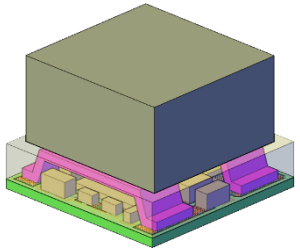
Programmable fault responses protect system, shut down in orderly fashion, restart automatically if fault is removed.

Create Fault Log

Black-box recorder, capture events leading up to fault, stored in NVM.

New PMBus POL Family Preview

Development



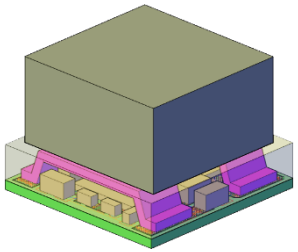
6.25x6.25mm

LTM4739

10A

90% Eff 12V to 1V/10A

Development



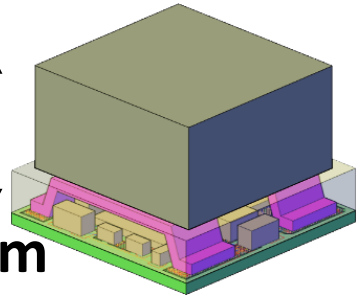
6.25x6.25mm

LTM4740

15A

87% Eff 12V to 1V/15A

Development



7.5x7.5mm

LTM4741

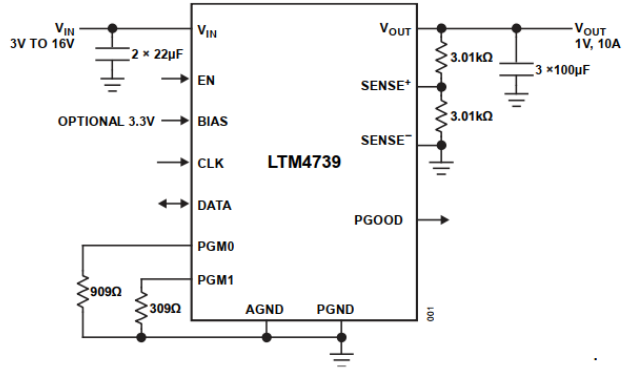
25A

86.5% Eff 12V to 1V/25A

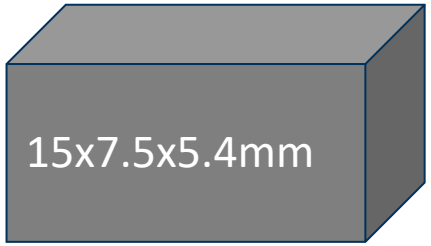
Key Benefits

- PMBus
- P90(90nm) IC
- High Efficiency (~90%)
- Compact Size (6.25x6.25mm)
- LTM4739, LTM4740 is Common Footprint

TYPICAL APPLICATION



Development



LTM4742

Dual 20A

Single 40A

86.5% Eff 12V to 1V/40A

uModule vs uSLIC

µModule

LTMxxxxx

Integration ↑

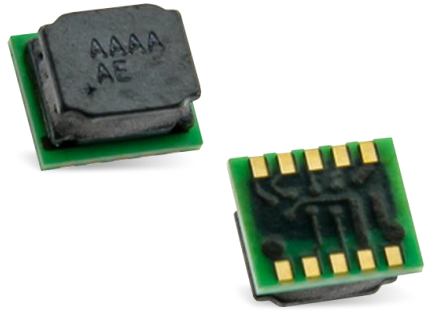
Size ↑

0.2A ~ 1000+ A

Range

µSLIC

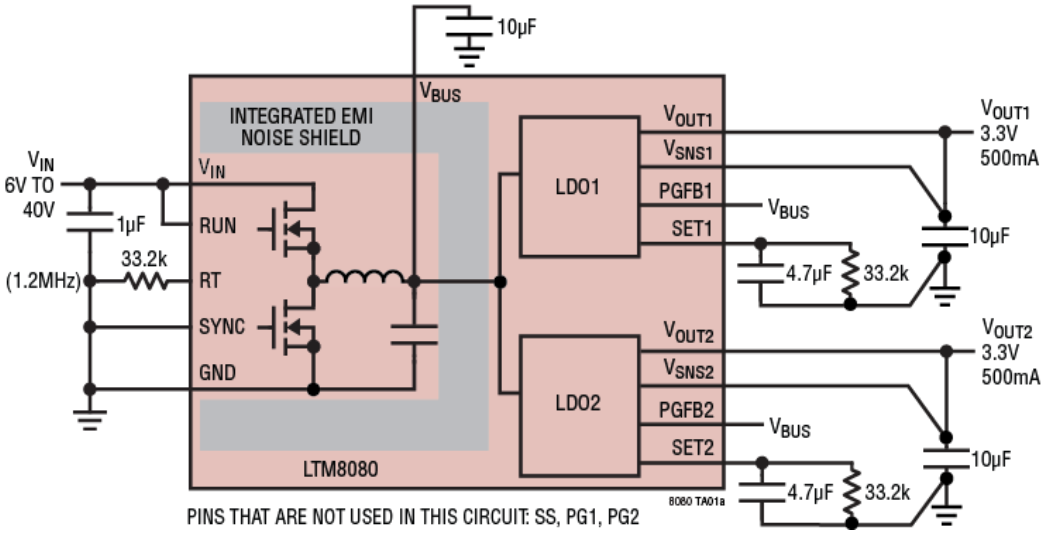
MAXMxxxxx

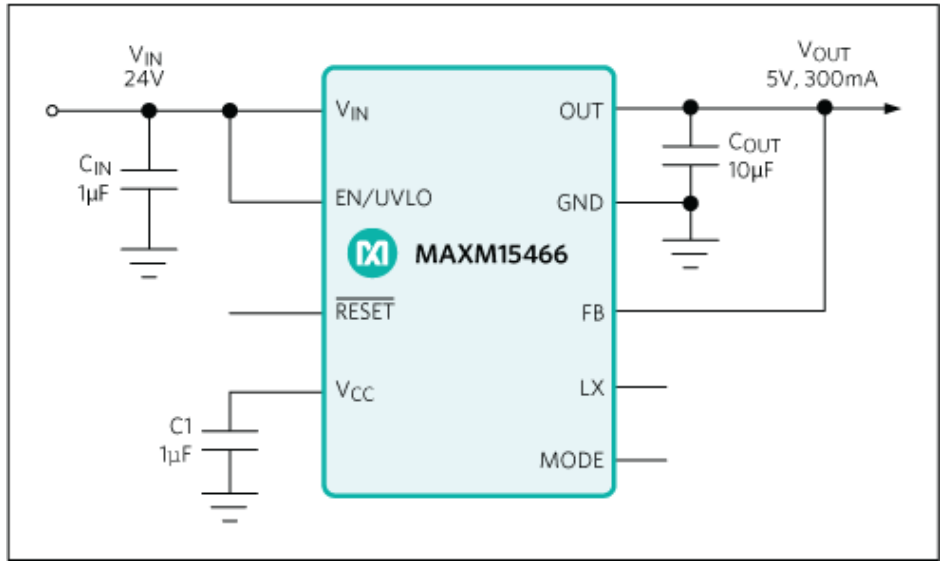


Integration ↓

Size ↓

0.1A ~ 2A

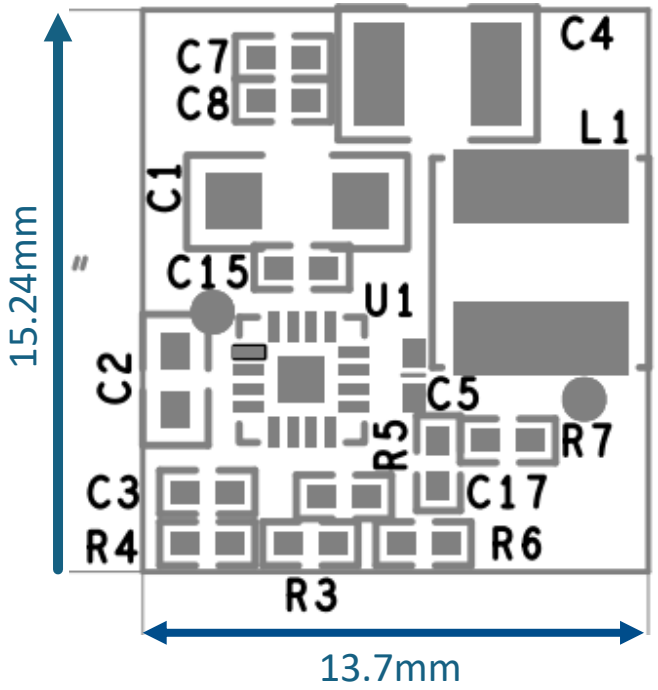




Comparison of Power Solution Size:36Vin/3.3Vout/2A

Total solution area: 209.03 mm^2

Power density: 31.57 W/mm^2



Monolithic power IC solution:

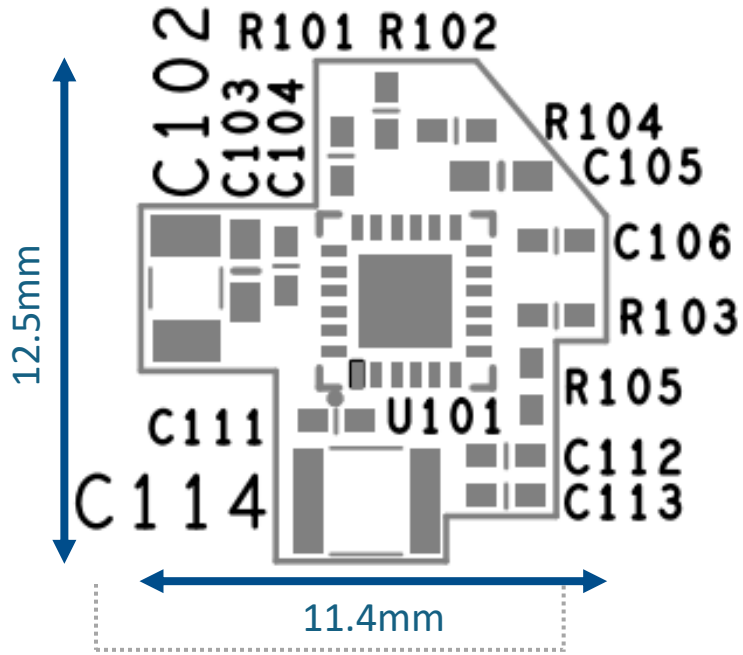
MAX17662

31.83%
total solution area reduction

46.72%
increase in power density

Total solution area: 142.5 mm^2

Power density: 46.32 W/mm^2

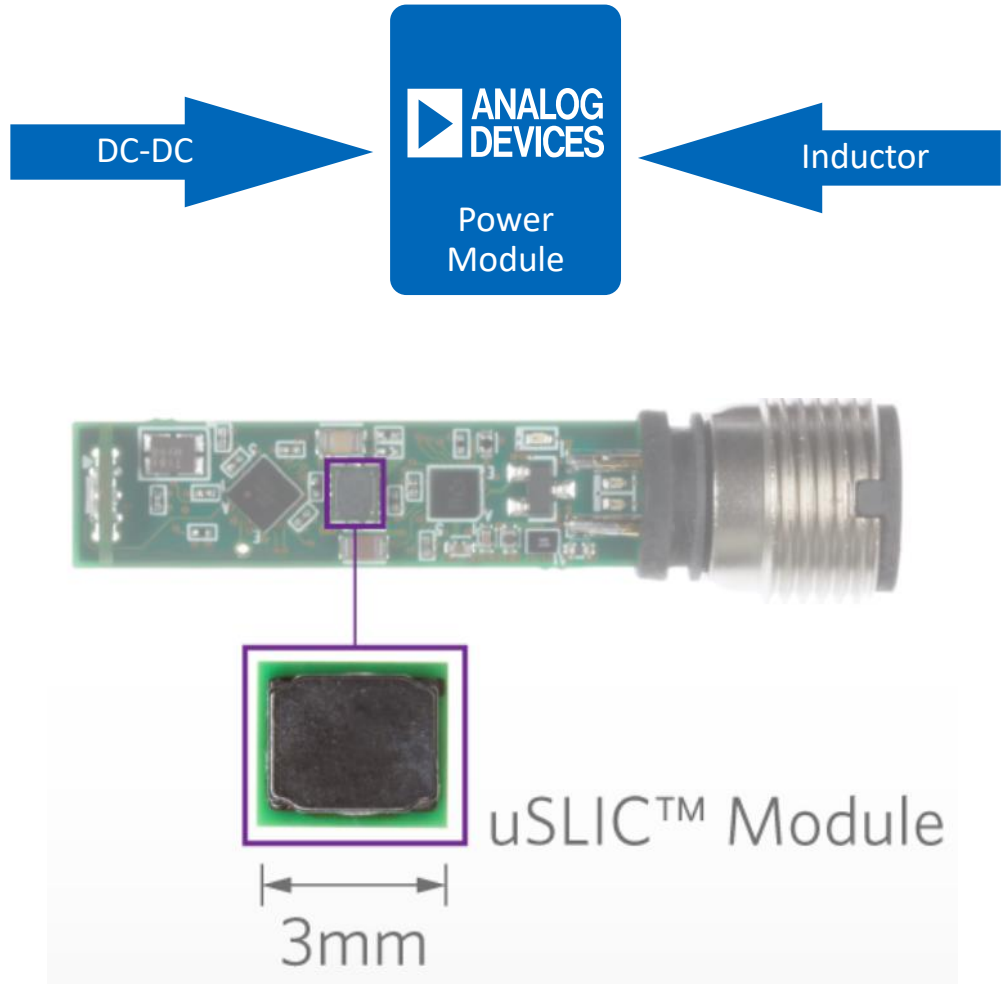


***uSLIC™** power solution:*

MAXM17633

What is a uSLIC Module?

- uSLIC : Micro System Level Integrated Circuit
  - 전력 IC와 인덕터를 하나의 패키지 안에 통합한 모듈

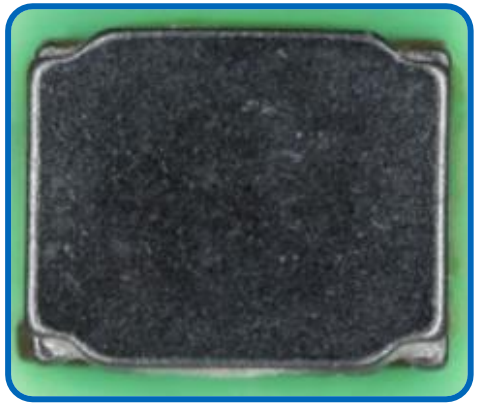


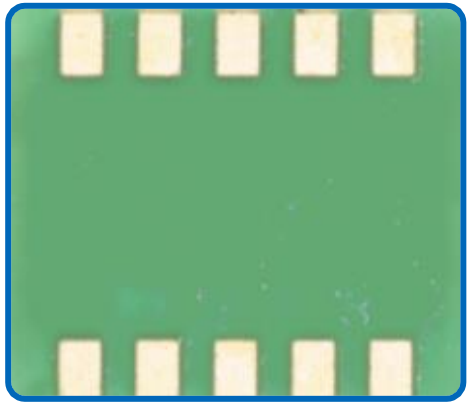
Benefits of uSLIC Modules:

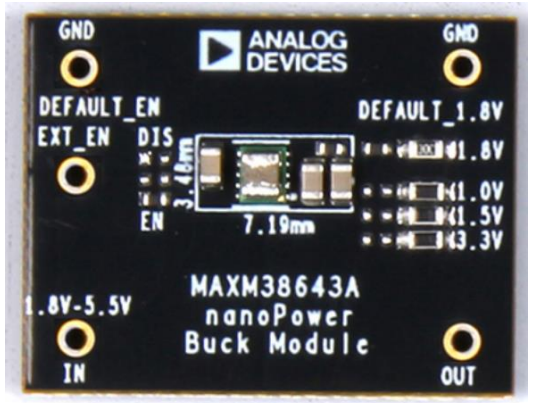
- Smal Solution size
- High Efficiency
- Quicker Time To Market
- High Power Density
- Rugged
- Reduced Eng'g Effort

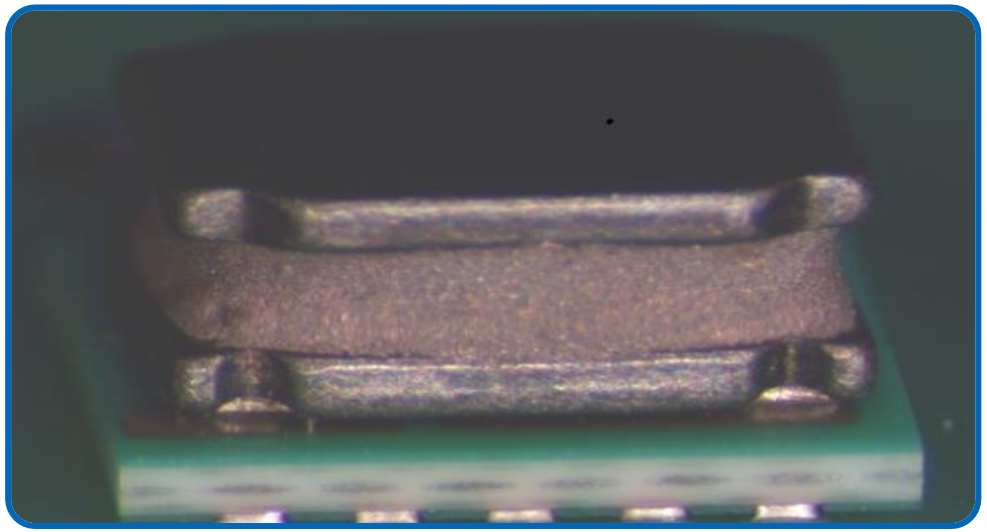
uSLIC Packaging Technology

Multiple Layer Substrate	**Better routability**
Inductor Stacking	**Smaller footprint**
Pick and Place	**Manufacturability**
Pins on Periphery	**Easier Board Layout**



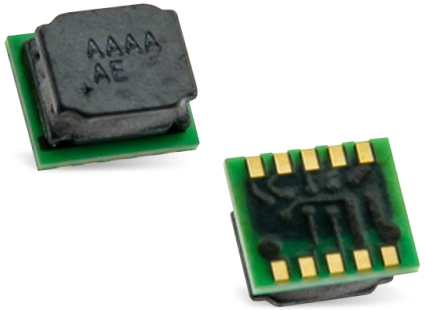






Common Design Challenges

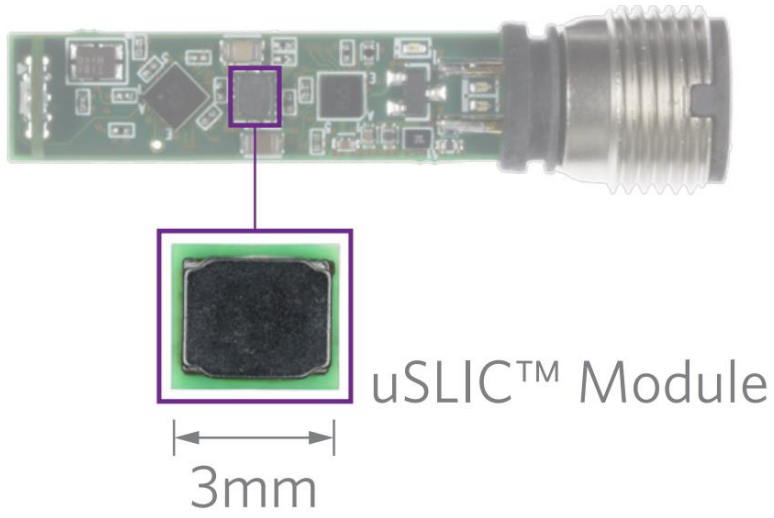
- 전자기기 소형화로 인해 설계 공간이 매우 제한적일 경우
  - ➢ Power Module을 사용하면 솔루션 크기를 크게 줄일 수 있음

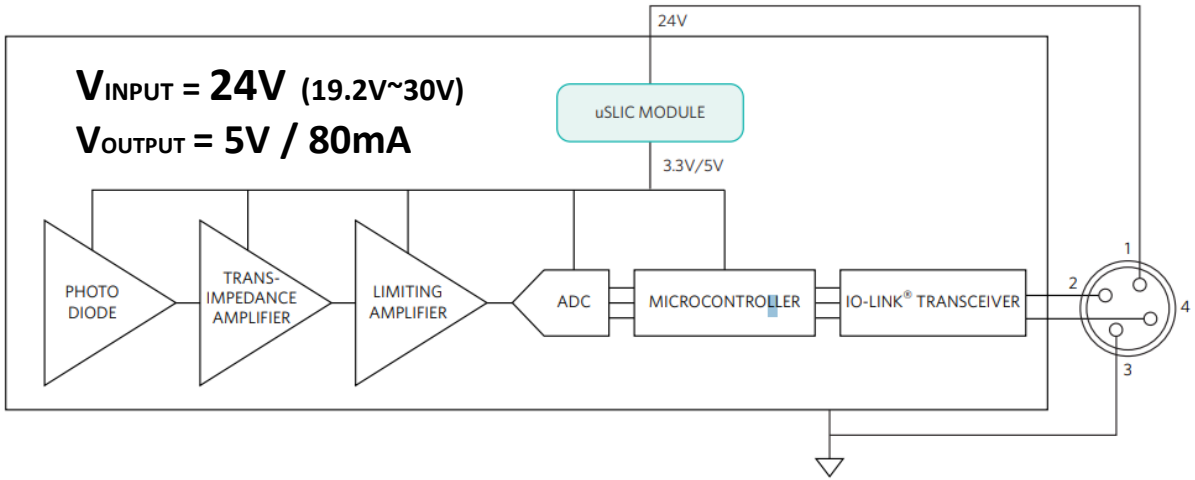


- 높은 주변 온도 또는 공기 흐름이 없는 열적으로 어려운 환경
  - ➢ 고효율 Fully Synchronous Power Module을 사용하면 온도 상승을 최소화할 수 있음
- 배터리로 동작하는 장비로써 동작 시간을 최대화해야 하는 경우
  - ➢ 높은 효율은 배터리 사용 시간을 더욱 길게 확보하는 데 도움이 됨
- 긴 케이블, 품질이 나쁜 전원 등으로 인해 예측 불가능한 Voltage Transient가 발생할 수 있는 환경
  - ➢ 넓은 입력 전압 범위를 지원하는 Power Module은 추가적인 보호 기능과 안정적인 동작을 제공함

uSLIC Usages : Optical Proximity Sensor

PCB Size = 6.5 mm x 30 mm



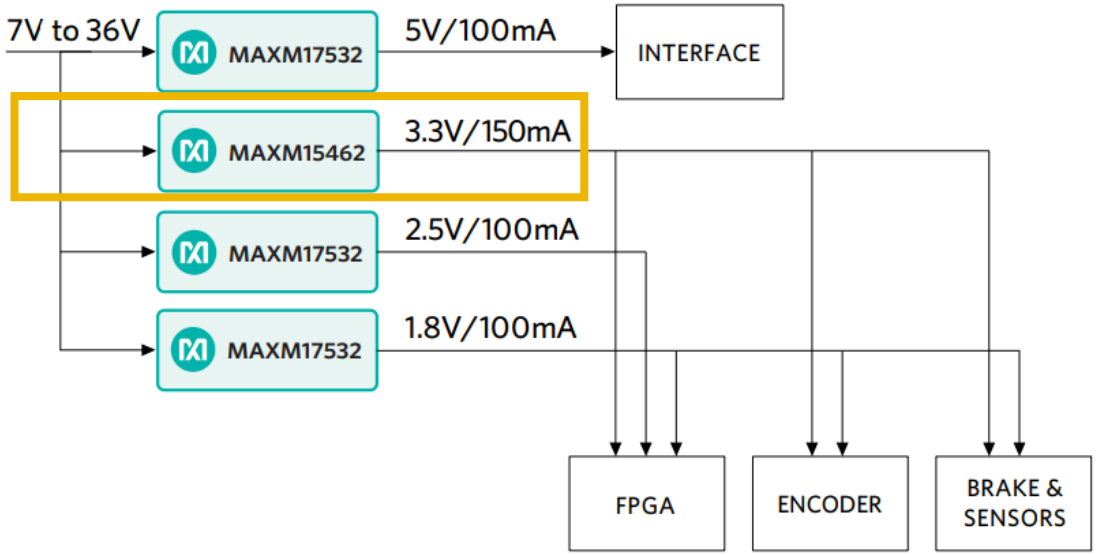


4X more efficient than the LDO

Device	Efficiency	Input Power	Power Dissipation
MAXM17532	83%	482mW	82mW
LDO	21%	1920mW	1520mW
Ratio:	**395%**	**25%**	**1/19**

uSLIC Usages : Motor Encoder

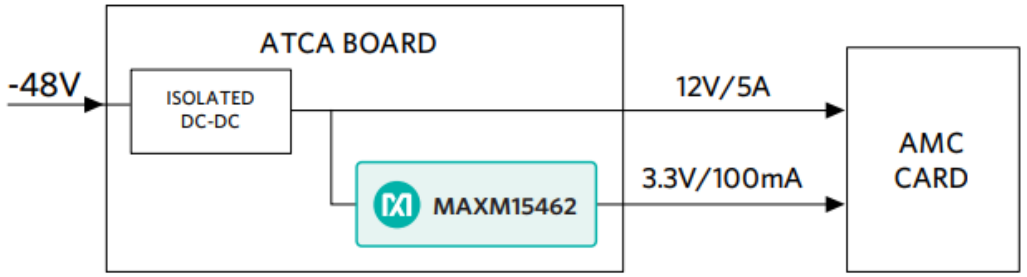
V_{INPUT} = **24V** **(19.2V~30V)**



Motor inductive ringing ads an extra guard band requirement to the **7VDC to 36VDC** operating range for the power converter.

Device	Efficiency	Input Power	Power Dissipation
MAXM15462	85%	583mW	88mW
LDO	54%	917mW	422mW
Ratio:	**158%**	**64%**	**1/4.8**

uSLIC Usages : ATCA Housekeeping

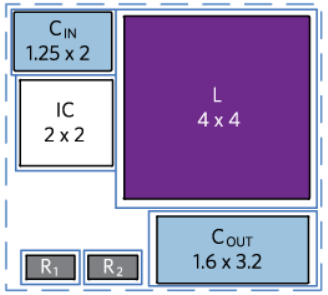


A **MAXM15462 42V/300mA uSLIC power module** would serve this +3.3V requirement very well while taking **very little space**, saving room for other circuitries.

- Easy to Use
- High Efficiency
- Flexible Design
- Robust Operation
- Rugged

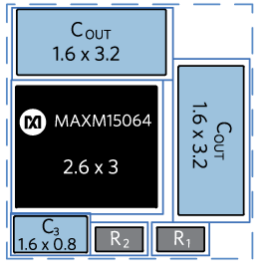
uSLIC Usages : Harsh Industrial Environment

Typical 300 mA Buck



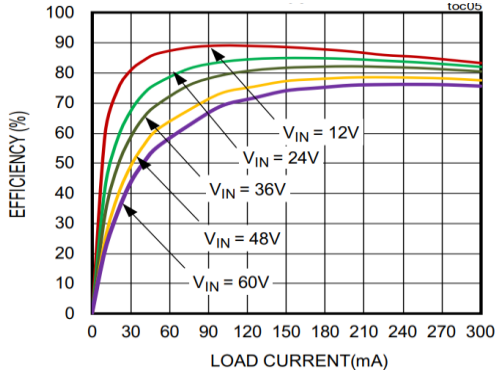
29.3mm² net area

MAXM15064
60V,300mA uSLIC

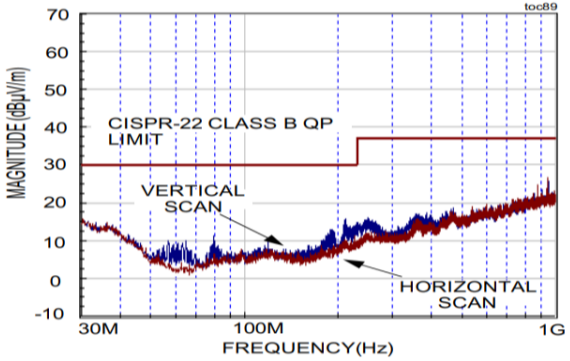


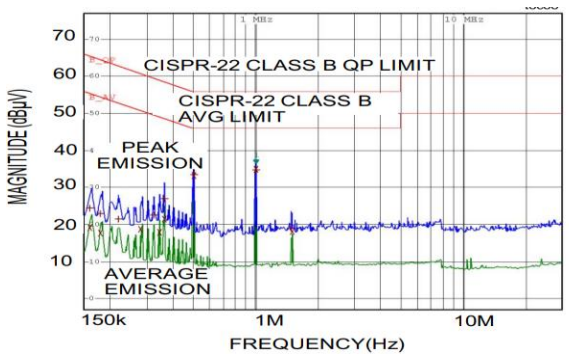
21mm² net area

28% smaller



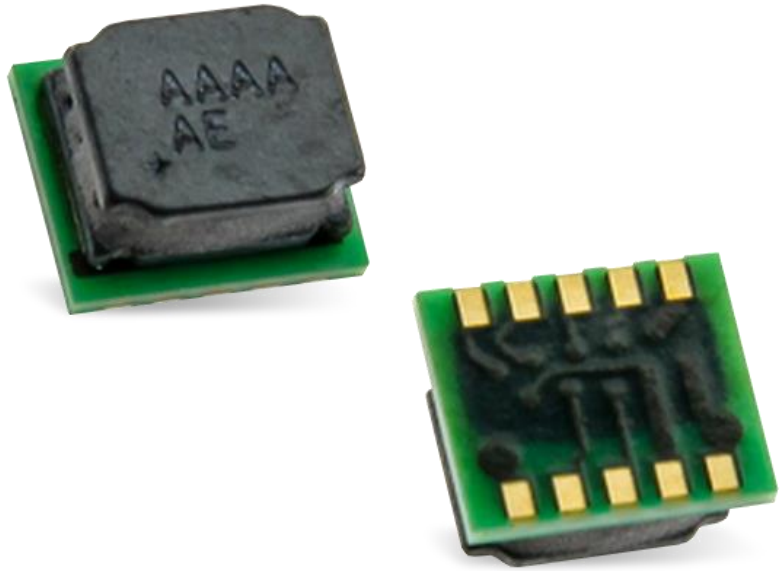
High efficiency ensuring minimal heat output





Low Conducted and Radiated EMI

uModule & uSLIC Conclusion



AHEAD OF WHAT'S POSSIBLE

analog.com