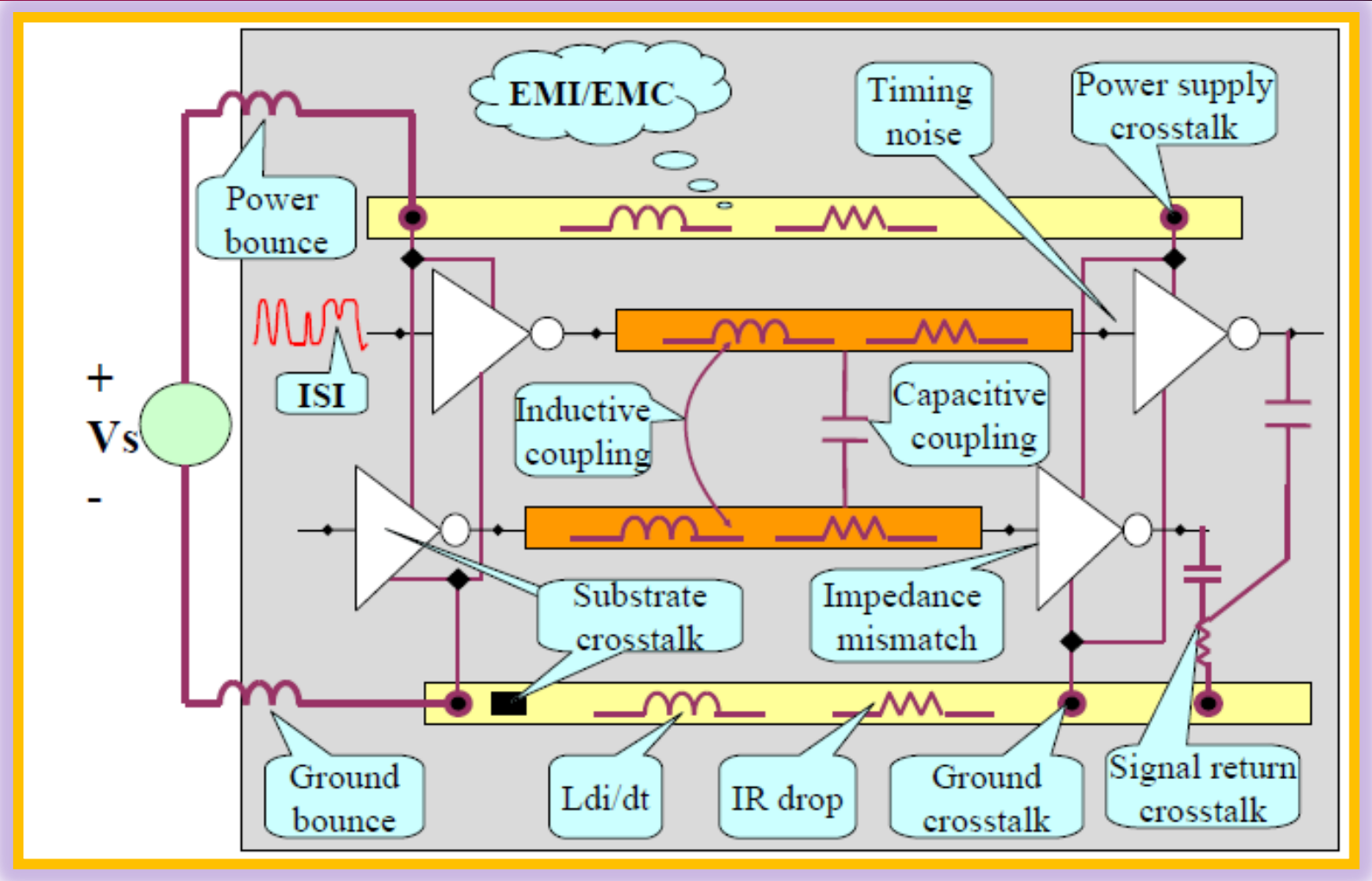
PollEx DFE/SI 를 활용한, SI/PI/EMC 대응 설계

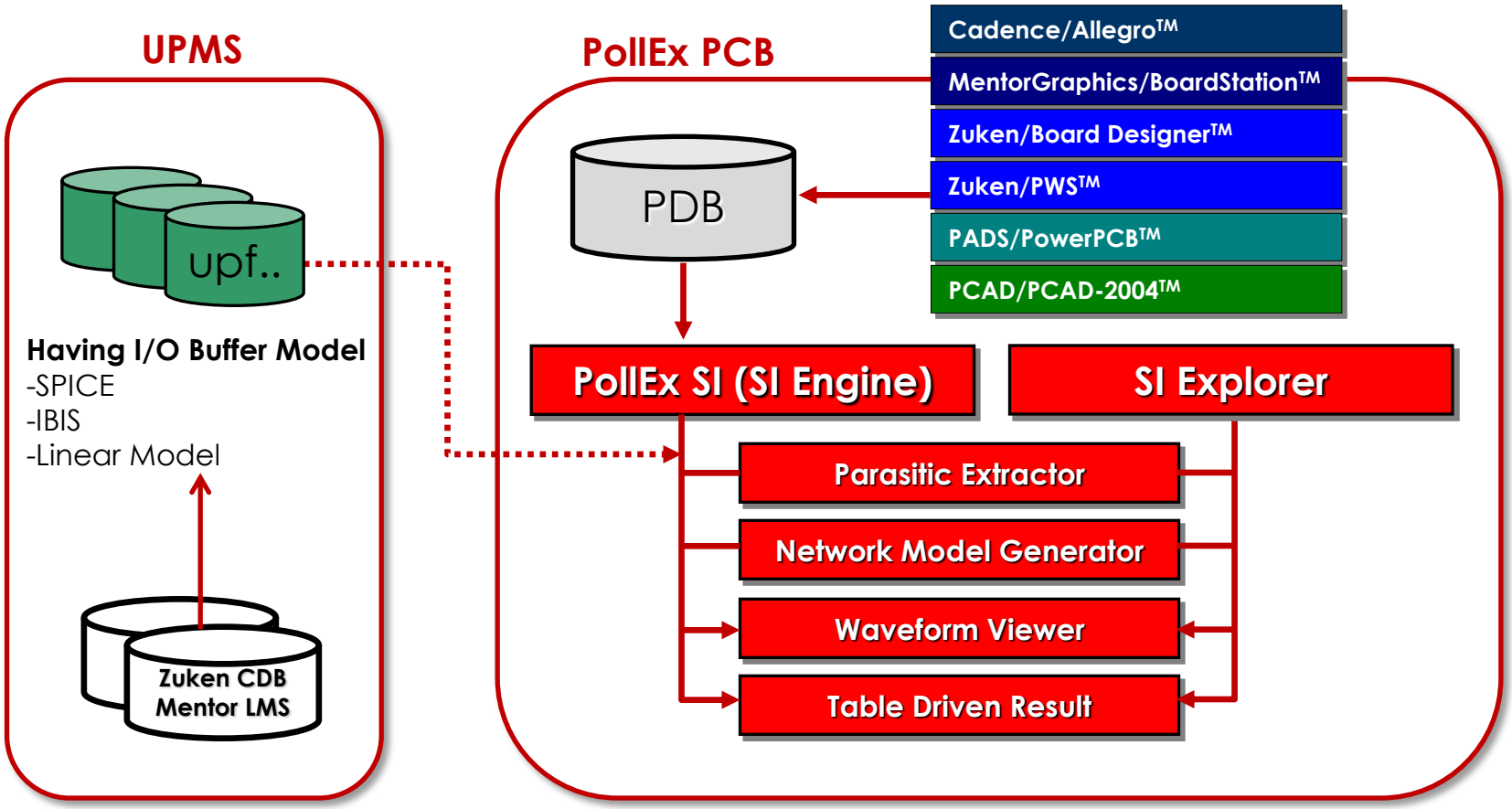
- POLLIWOG Corporation.

2014.11.18
Polliwog Corporation
DaiHo Ham, Director

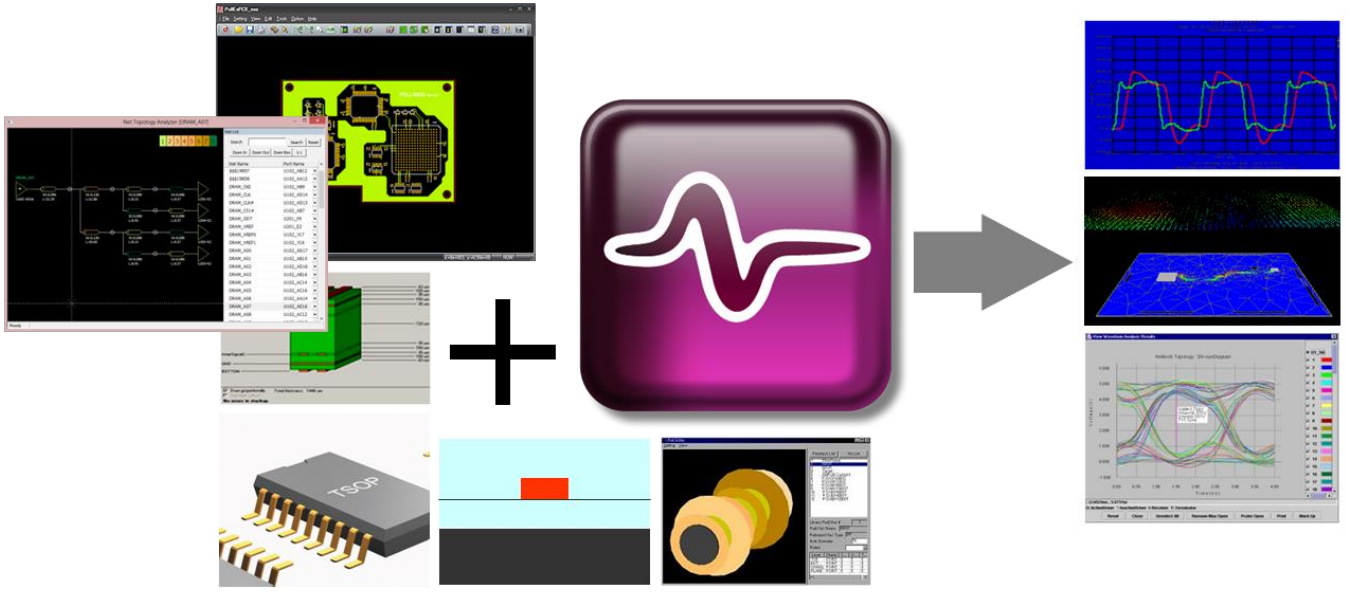
SI/PI/EMI Issue in PCB



PollEx Signal Integrity



PollEx SI



- **Transmission Line Analysis**: Routed Net Impedance, Delay 분석, TLM Model 생성/관리
- **Network Analysis**: 신호 Eye Diagram, Setup/Hold Margin 및 Noise Analysis
- **Data Line Analysis**: DDR Data Line의 Byte별 Analysis 일괄 수행
- **ADD/CMD/CNTR Line Analysis**: DDR ADD/CMD/CNTR Line의 Byte별 Analysis 일괄 수행
- **Crosstalk Analysis**: Routed Net Coupling 분석, Odd/Even Mode Crosstalk 분석
- **Net Topology Analysis**: Net Topology 분석 및 수정/해석 기능

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◆ Transmission Line Analysis

- Analysis PCB trace etching effect
- Analysis GND guard effect

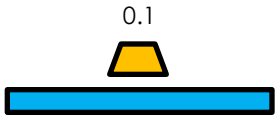
$$Z0 = \sqrt{\frac{(R + j\omega L)}{(G + j\omega C)}}$$

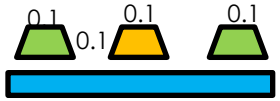
Z0 = L/C ∝ W, h, t

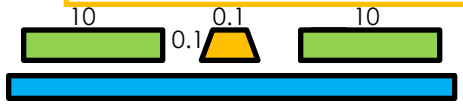
$$Zo = \frac{60}{\sqrt{\varepsilon r}} \ln \frac{4b}{0.67\pi(0.8w + t)}$$

$$tf = 1.017 \sqrt{\varepsilon r} \quad (ns/ft)$$

* w/(b-t)<0.35, t/b<0.25







Transmission Line Analysis-Display Results

Model / Item

ITEM
- Resistance (Ohm/cm)
  - R11
- Inductance (nH/cm)
  - L11
- Capacitance (pF/cm)
  - C11
- Conductance (mS/cm)
  - G11
- DC Resistance (Ohm/cm)
  - R01
- Skin Depth (m)
  - SD1
- Char-Impedance (Ohm)
  - Z01
- Delay (sec/m)
  - TD1
- Velocity (m/sec)
  - V1
- Attenuation (dB/m)
  - A1

Frequency (MHz)	1_0.09
100	52.691, -1.789
111.1	52.597, -1.686
144.4	52.36, -1.467
200	52.11, -1.23
277.8	51.902, -1.019
377.8	51.735, -0.857
500	51.587, -0.728
644.4	51.482, -0.629
811.1	51.394, -0.548
1000	51.326, -0.484

Display Network Parameters | Display Chart | Close

Frequency (MHz)	Z01
100	49.023, -0.364
111.1	48.998, -0.34
144.4	48.94, -0.289
200	48.874, -0.232
277.8	48.822, -0.181
377.8	48.778, -0.141
500	48.741, -0.11
644.4	48.713, -0.085
811.1	48.691, -0.065
1000	48.674, -0.049

Display Chart | Close

Frequency (MHz)	Z01
100	42.747, -0.61
111.1	42.656, -0.52
144.4	42.431, -0.33
200	42.195, -0.123
277.8	41.997, 0.063
377.8	41.837, 0.207
500	41.697, 0.32
644.4	41.598, 0.409
811.1	41.51, 0.48
1000	41.444, 0.539

Display Chart | Close

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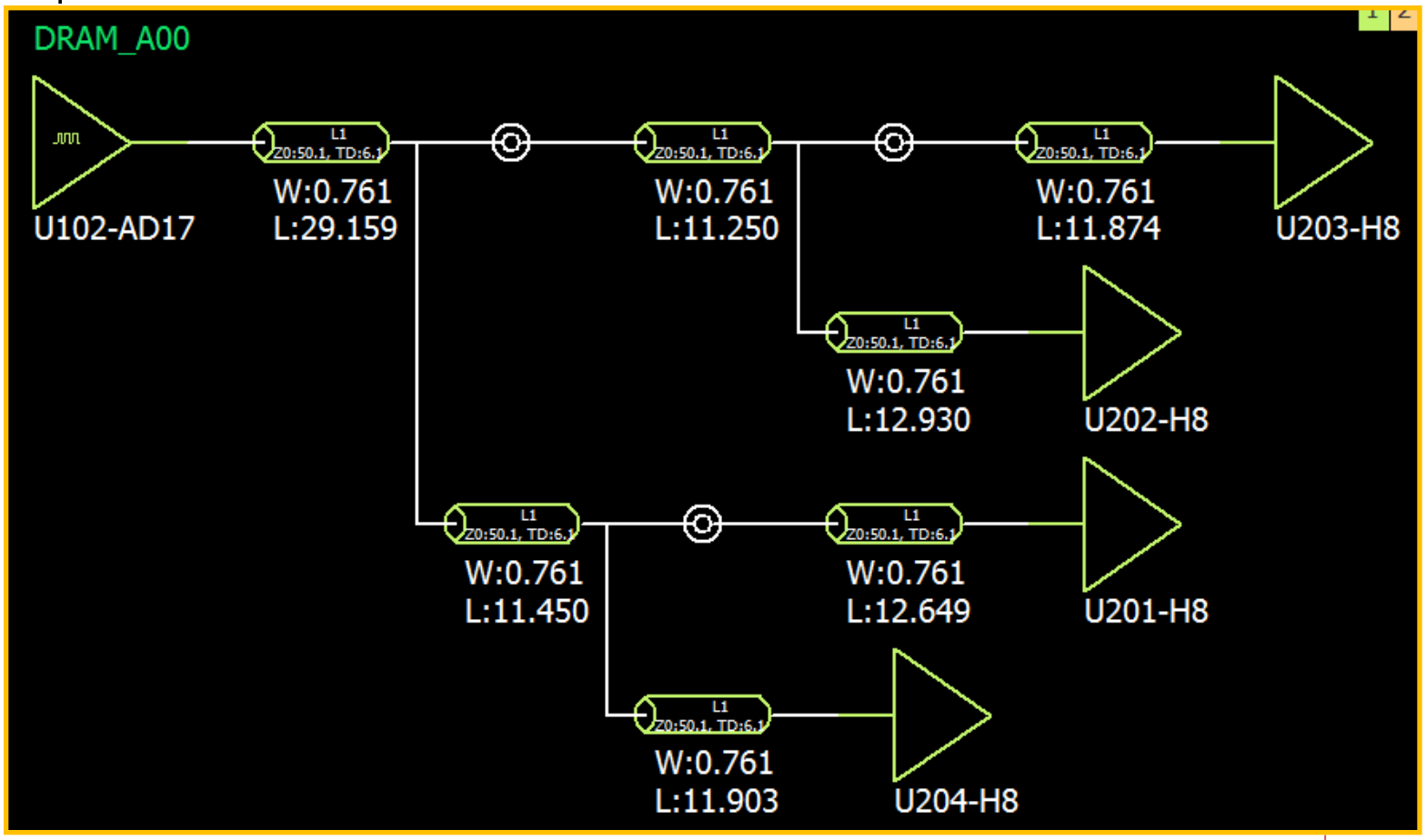
◆ Transmission Line Analysis

- Impedance Mismatch



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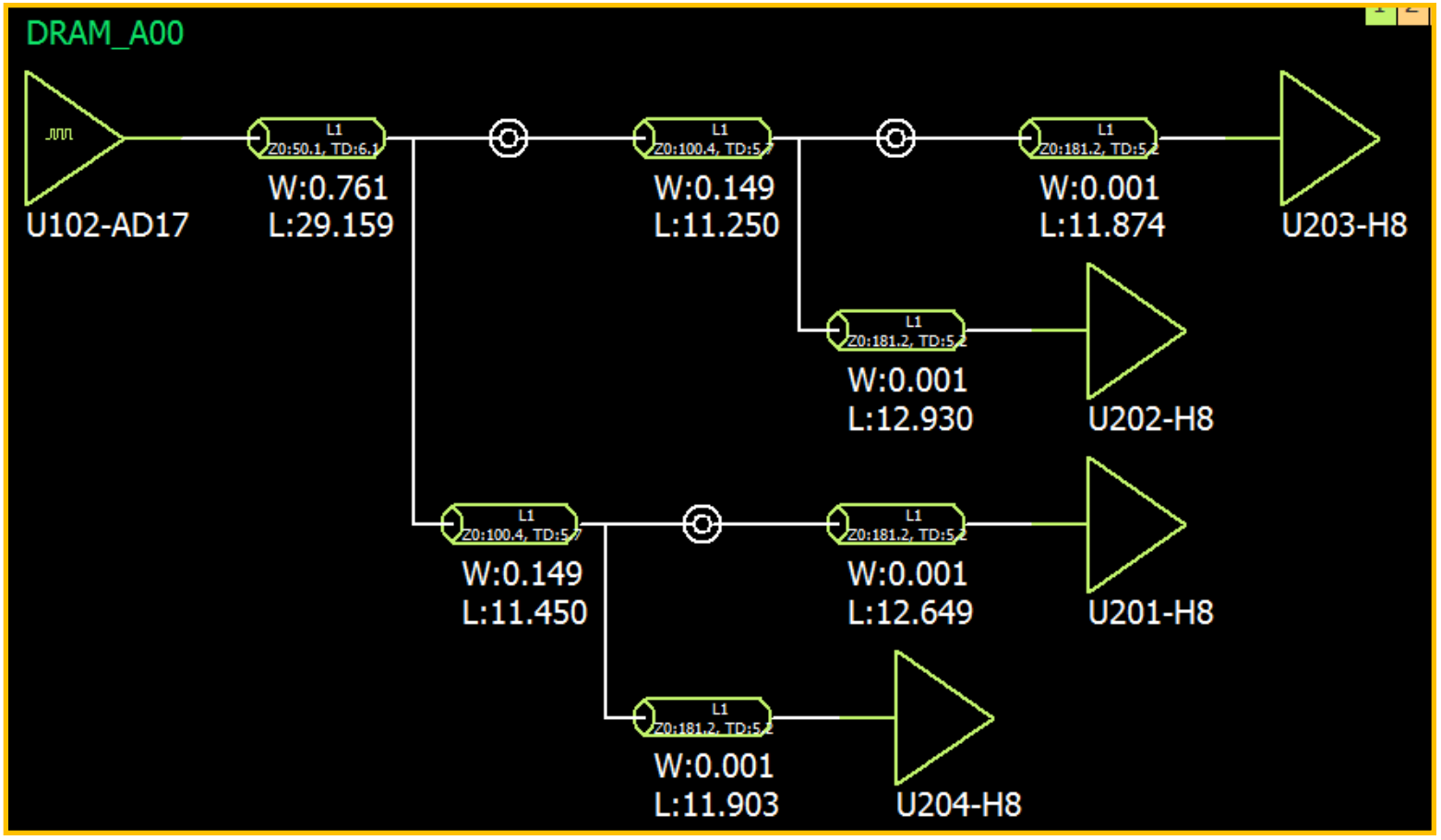
◆ Transmission Line Analysis

- Impedance Match



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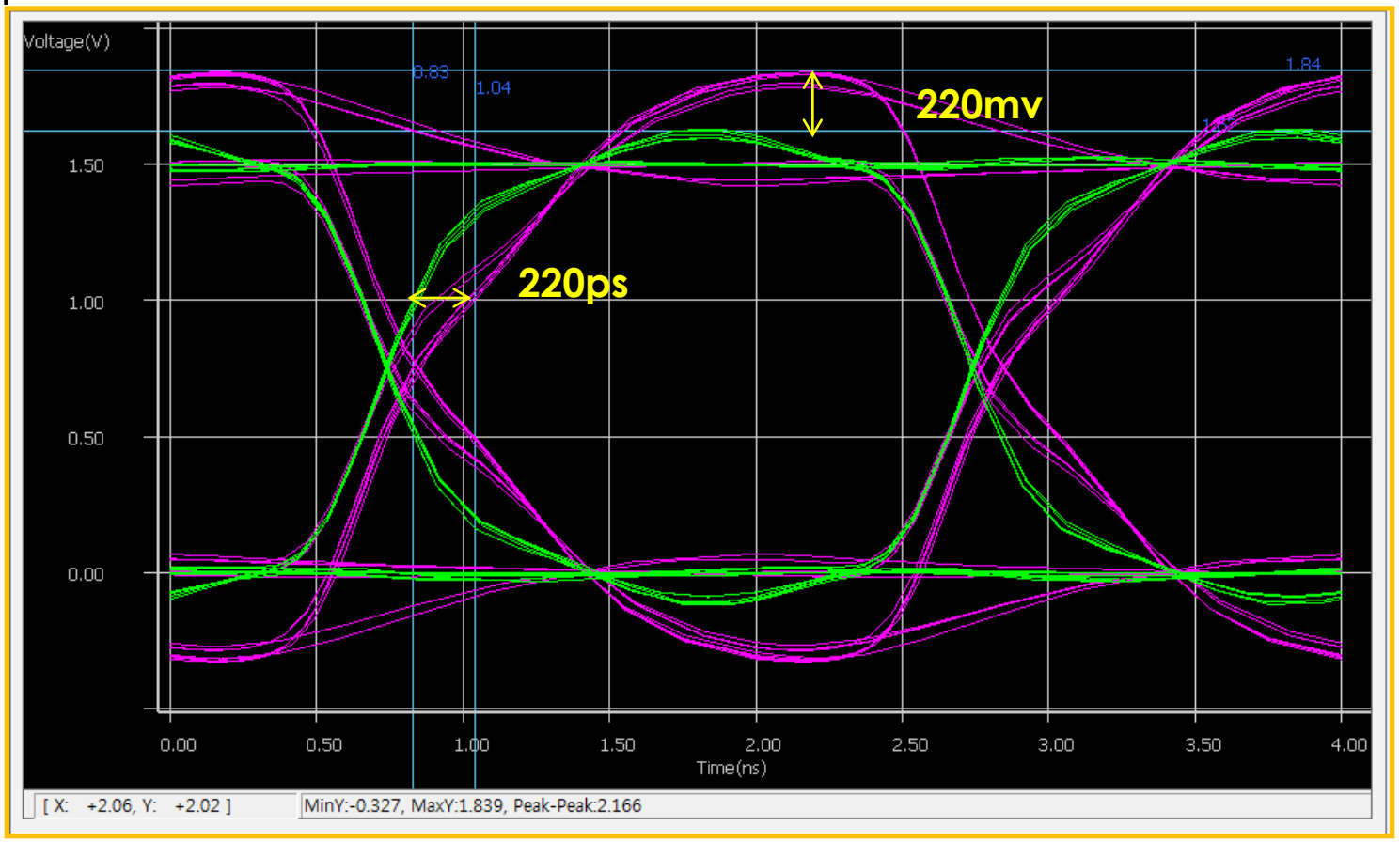
◆ Transmission Line Analysis

- Impedance Mismatch



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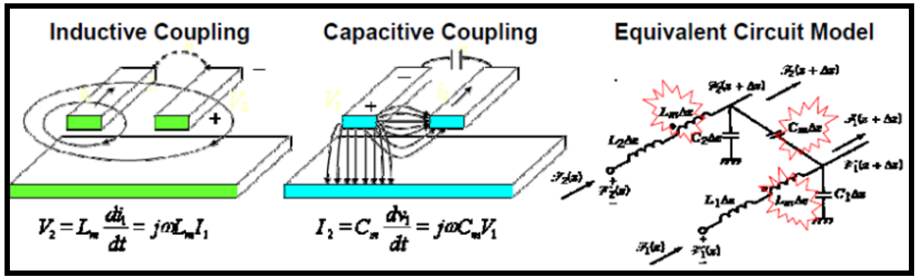
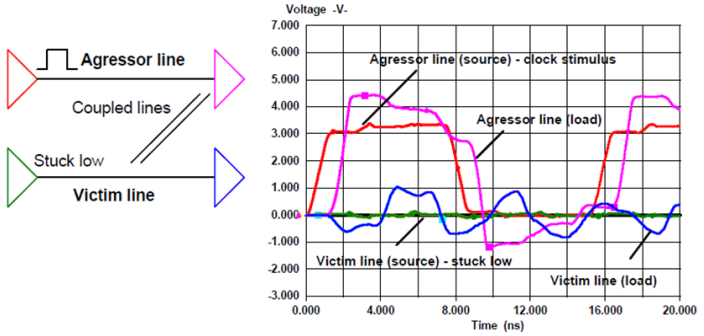
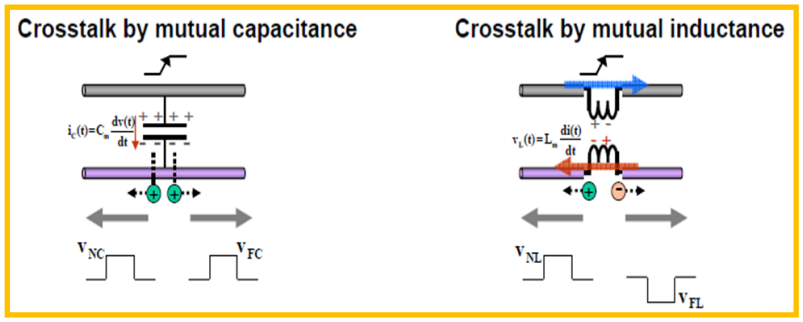
◆ Crosstalk Analysis

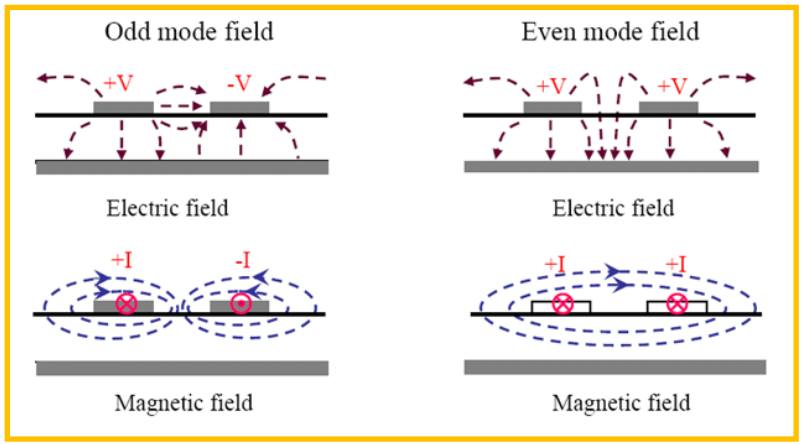
- 주변 신호선과의 Noise Coupling 현상 해석



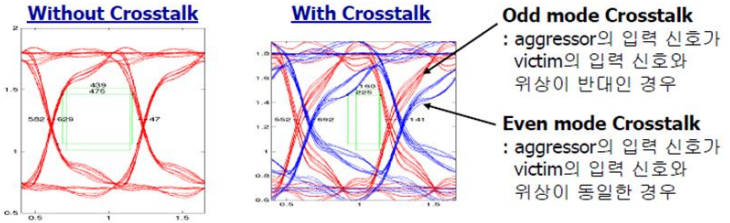
Noise Margin Issue







Timing/Noise Margin Issue



Odd mode Crosstalk
: aggressor의 입력 신호가 victim의 입력 신호와 위상이 반대인 경우

Even mode Crosstalk
: aggressor의 입력 신호가 victim의 입력 신호와 위상이 동일한 경우

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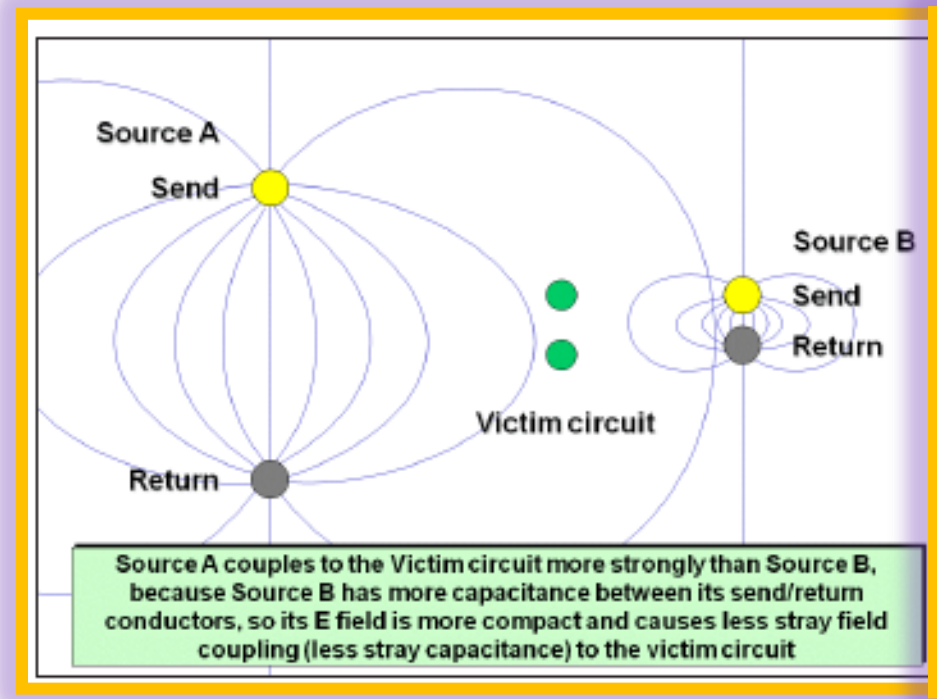
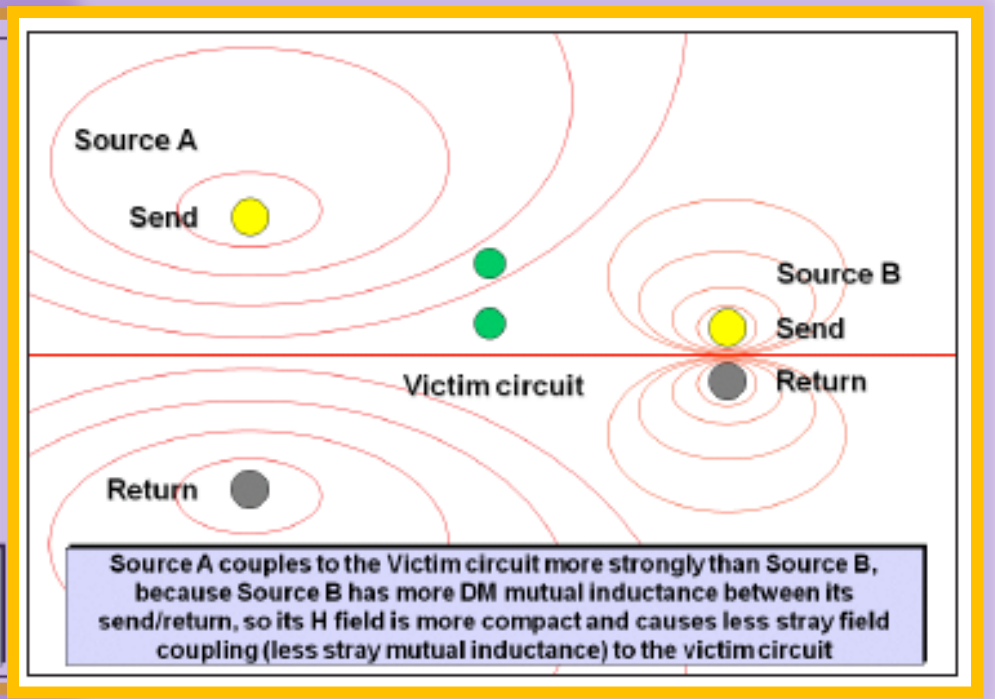
◆ Crosstalk Analysis

- 3W





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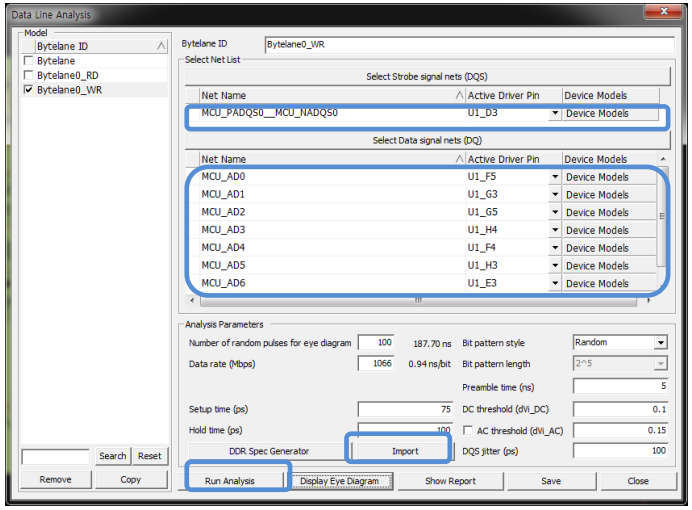
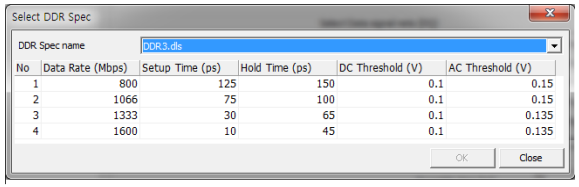
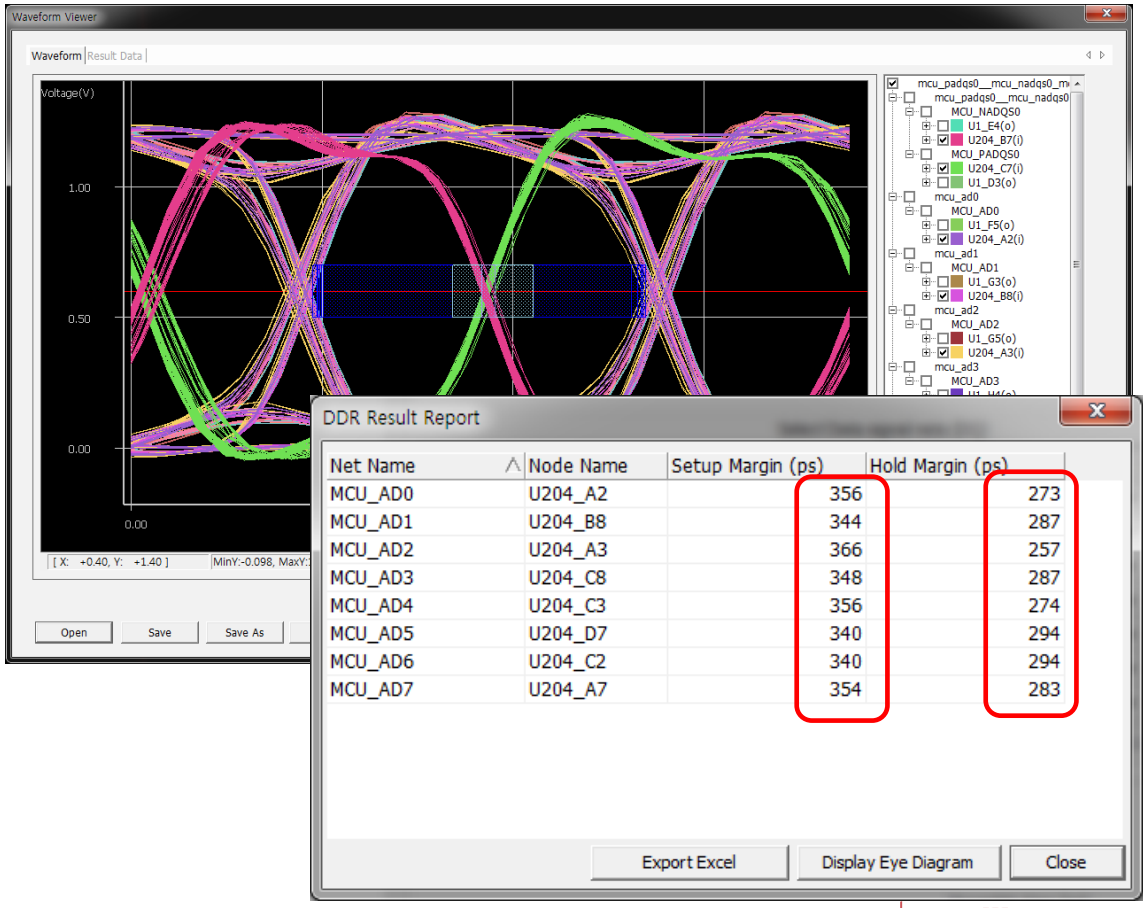
◆ Data Line Analysis

- DDR Data Line의 Byte별 Analysis 일괄 수행.







Centering을 통한 Margin 확보

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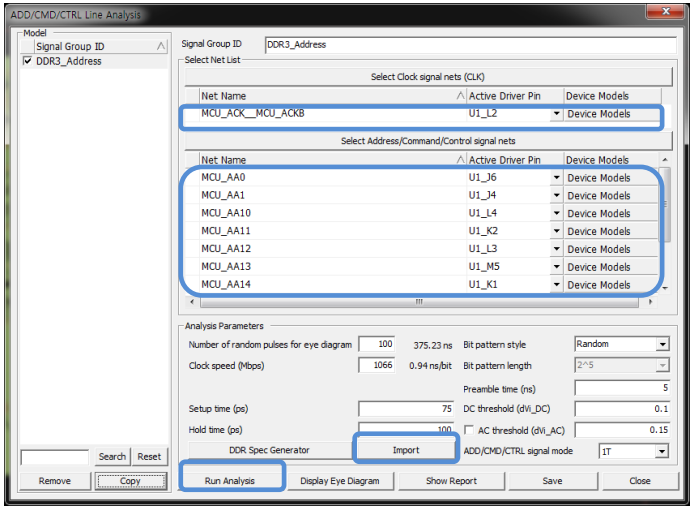
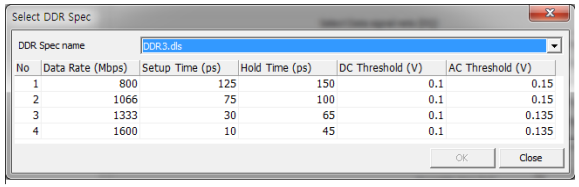
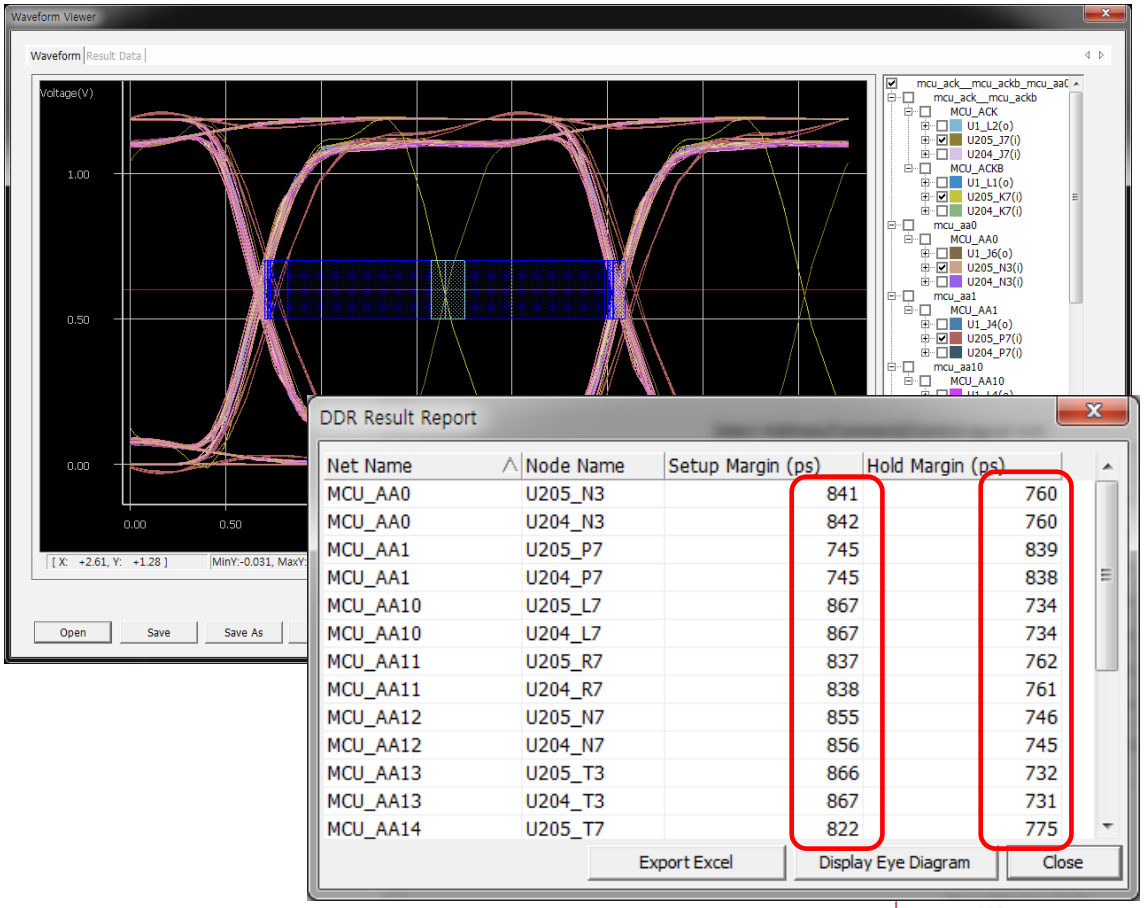
◆ ADD/CMD/CNTR Line Analysis

- DDR Control Line의 Byte별 Analysis 일괄 수행.







Centering을 통한 Margin 확보

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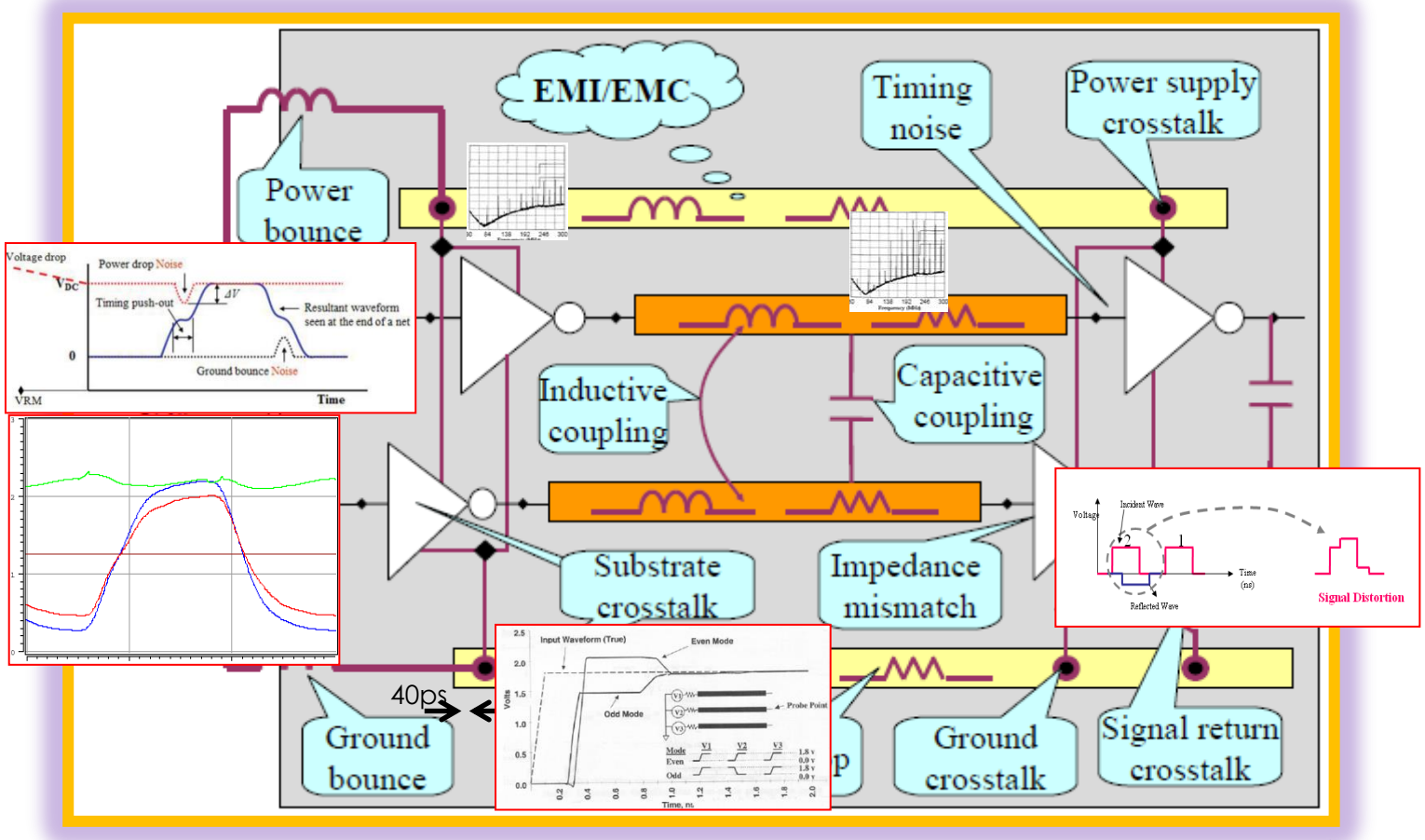
◆ Timing/Noise Margin Analysis

- Margin = Reflection + SSN + Crosstalk + Jitter



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◆ Read Timing Budget 예 (DDR2-667 사례)

PCB/Interconnect Skew Component	Setup	Hold	Units	Comments
Crosstalk	40	40	ps	-
Data Group Trace Mismatch	15	15	ps	- M/S: 7.1ps/mm, S/L:5.5ps/mm
SSN	80	80	ps	- Power Trace 구조
Termination Mismatch(VOH/VOL)	15	15	ps	Termination mismatch error that reduces the input eye. (OCD calibration 필수)
Eye Reduction	50	50	ps	V_{REF} mismatch error, termination error, and eye reduction due to slew rate differences between DQS and DQ
Jitter	100	100	ps	온도, 전압, Corner Chip
Total Board Skew	300	300	ps	-
DRAM output skew(tDQSQmax)	240	240	ps	From DDR2-400/533/667/800 data sheet (350/300/240/200)
DDR controller input skew requirement(tDISKEW)	550	550	ps	Controller Spec.
Read Timing Margin	10	10	ps	Margin = Controller Requirement – DRAM – Board Skew (DRAM out + Board Skew < Controller Requirement)

◆ Write Timing Budget 예 (DDR2-667 사례)

PCB/Interconnect Skew Component	Setup	Hold	Units	Comments
Crosstalk	40	40	ps	-
Data Group Trace Mismatch	15	15	ps	- M/S: 7.1ps/mm, S/L:5.5ps/mm
SSN	80	80	ps	- Power Trace 구조
Termination Mismatch(VOH/VOL)	15	15	ps	Termination Mismatch Error that reduces the input eye. (OCD calibration 필수)
Eye Reduction	50	50	ps	V_{REF} mismatch error, termination error, and eye reduction due to slew rate differences between DQS and DQ
Jitter	100	100	ps	온도, 전압, Corner Chip
Total Board Skew	300	300	ps	-
DDR Controller output skew(tDQSQmax)	290	290	ps	DDR Controller Spec.
DDR controller Output setup/hold	750	750	ps	Assumes Center Align
DRAM Input setup/hold (tDS/tDH) Requirement	100	175	ps	From DDR2 data sheet(400/533/667/800) (150-275/100-225/100-175/50-125)
Write Timing Margin	60	-15	ps	Margin = DDR controller – DRAM Requirement – DDR controller skew - Board Skew (Controller Output - Board Skew > DRAM Requirement)

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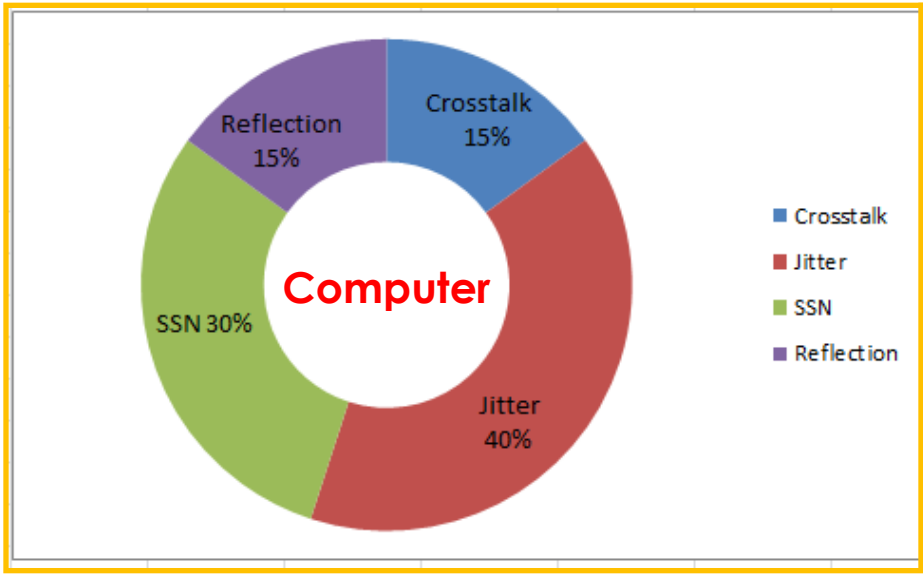
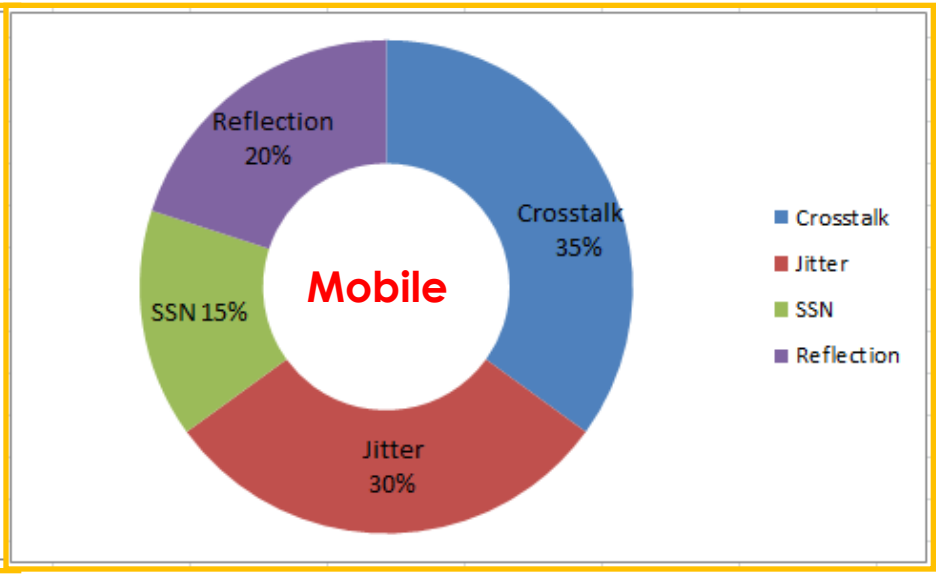
◆ Margin distribution policy

- Do not have blind faith in a Design Guide from Vendor.





- Termination required
- Net spacing: 3W
- Appropriate Decoupling Capacitor

- No termination(Except Clock)
- Net spacing: 2W
- Tight length matching

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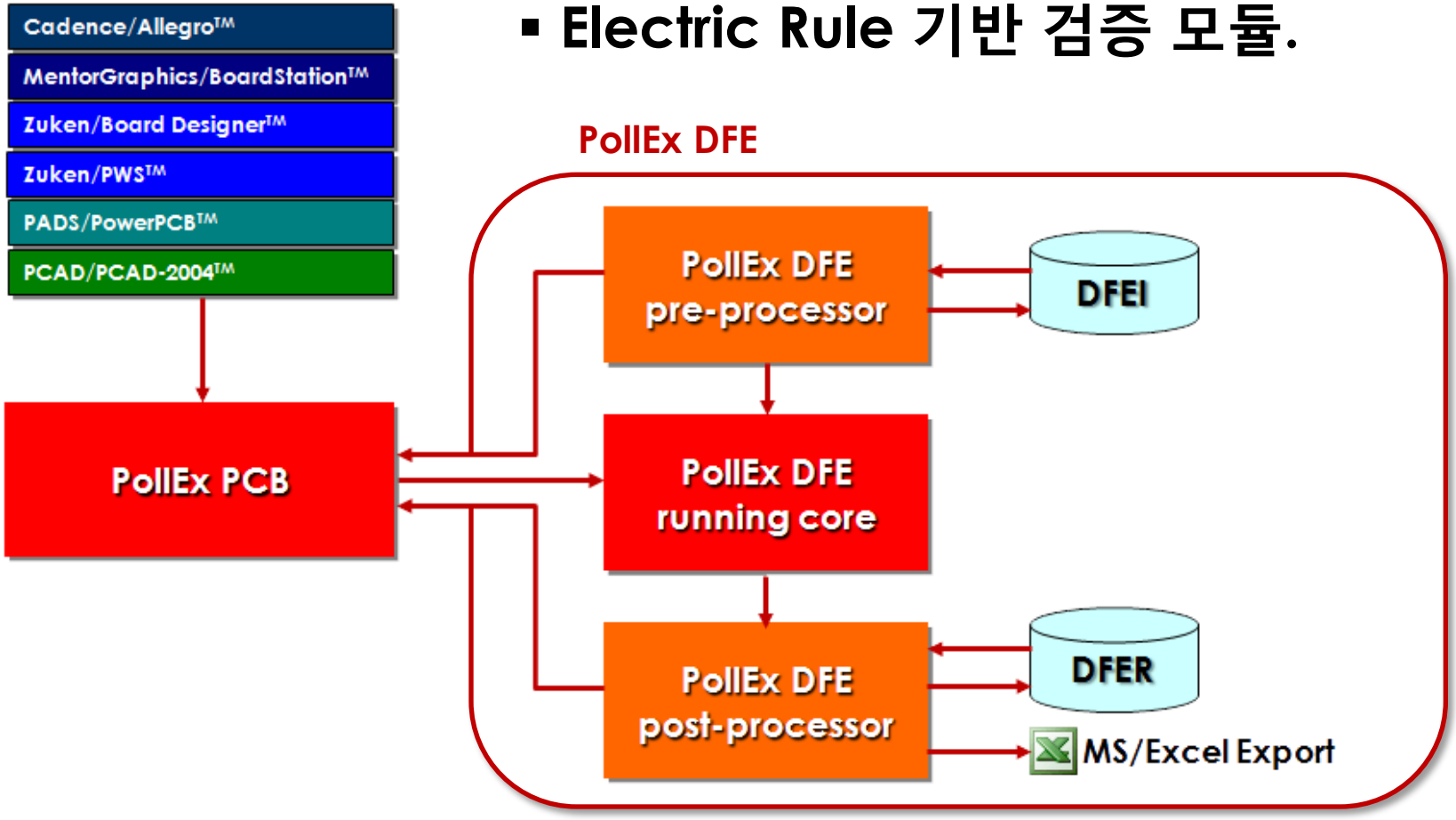
- Electric Rule 기반 검증 모듈.



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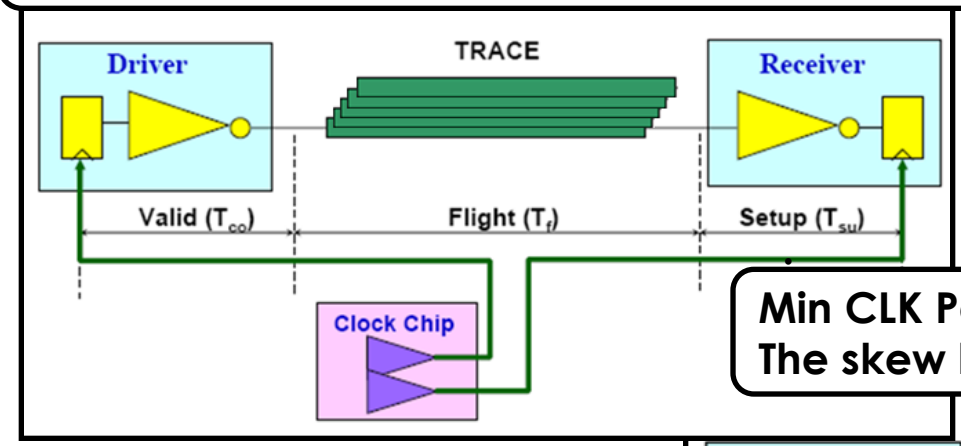
◆ Data Transfer Method

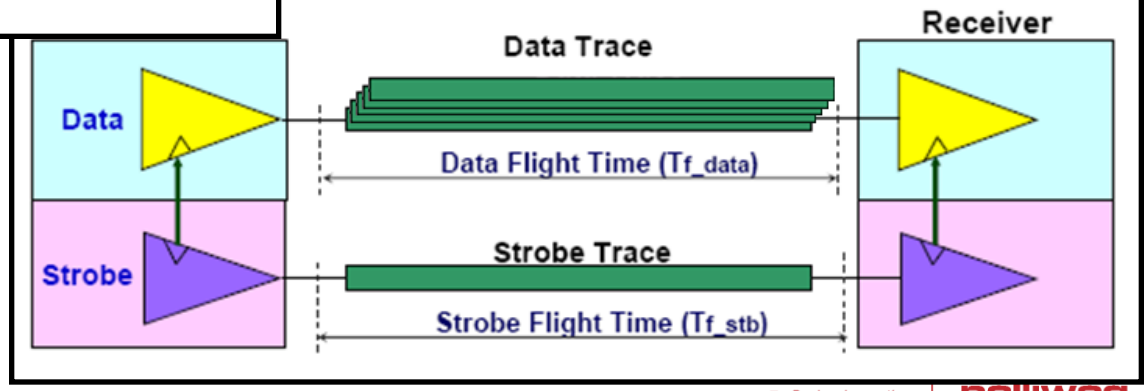
Common Clock Method

Min CLK Period = Valid + Flight + Setup + Jitter + Skew
Flight Time restricts Frequency of operation



Source Sync Method

Min CLK Period = No limitation theoretically
The skew between Tf_data and Tf_stb is important



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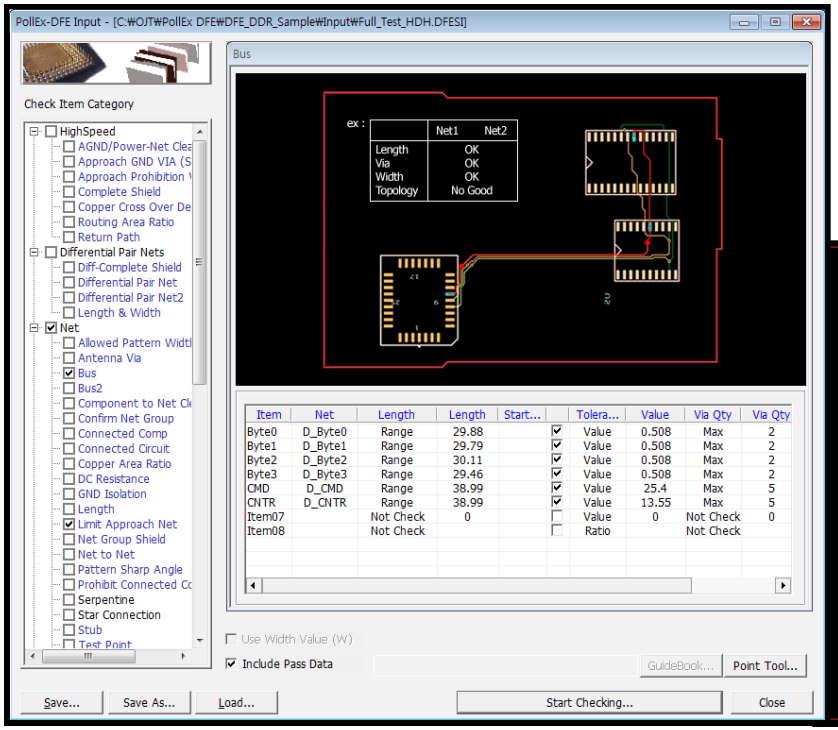
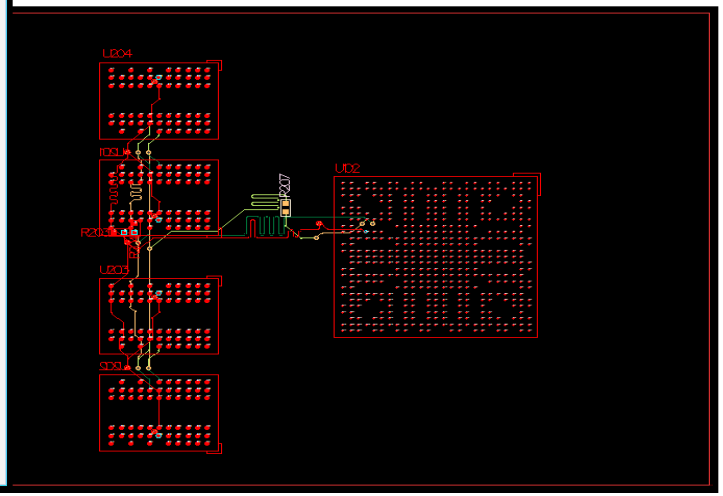
◆ BUS



Check Items:

- Trace length matching with tolerance.
- Via quantity.
- Trace width.



Item	Net	Length	Length	Start Component		Tolerance	Value	Via Qty	Via Qty	Width
Item01		Not Check				Ratio		Not Check		Not Check

- Not Check
- Min
- Max
- Range
- Longest Length
- Combination Length

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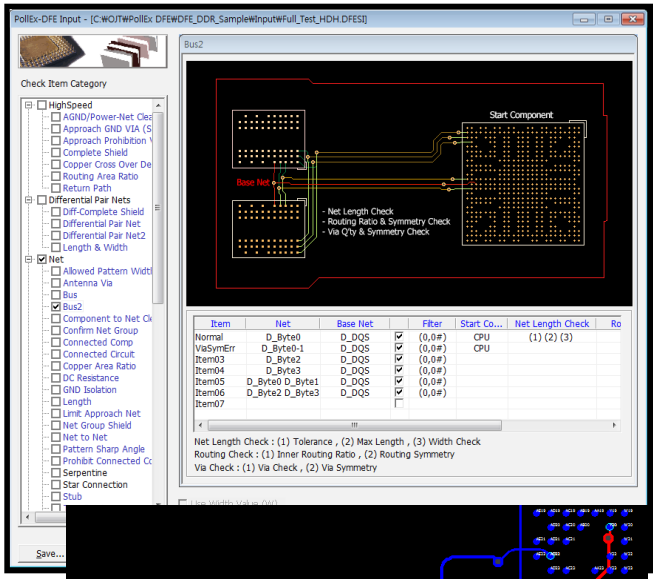
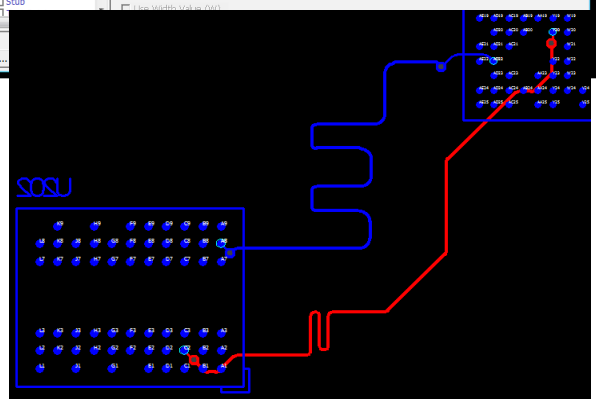
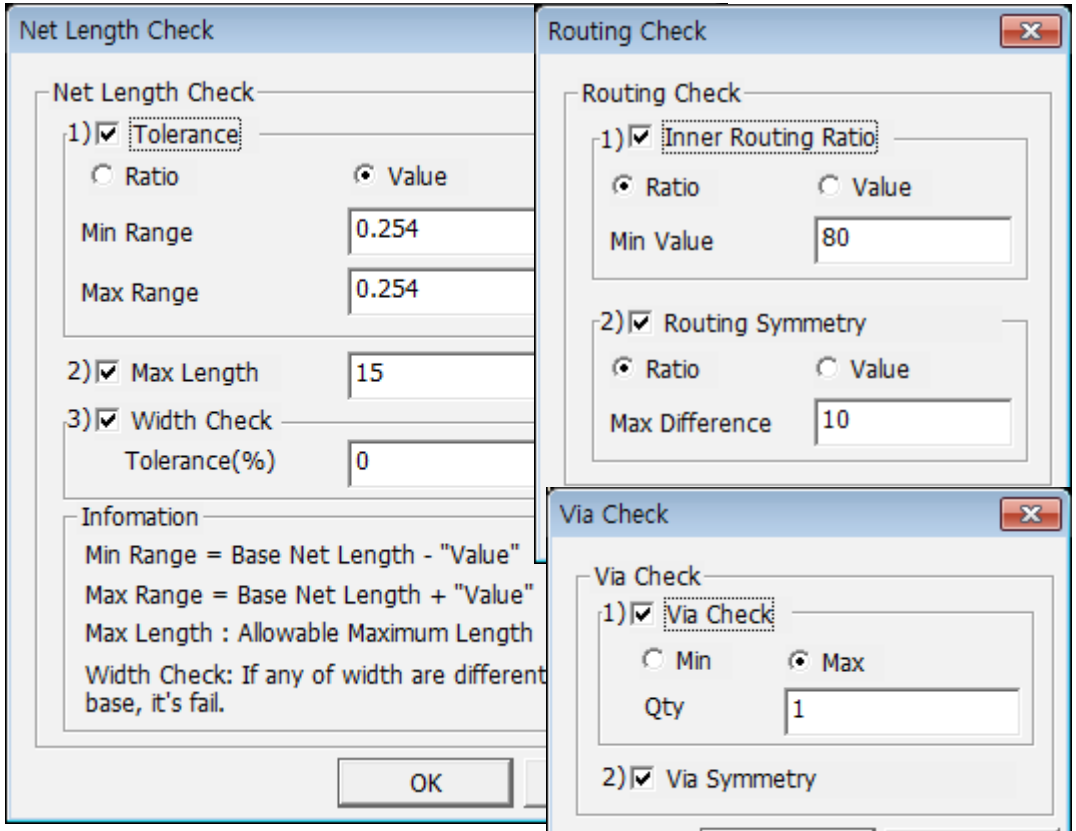
◆ BUS2

- Routing symmetry between strobe and data is Key.







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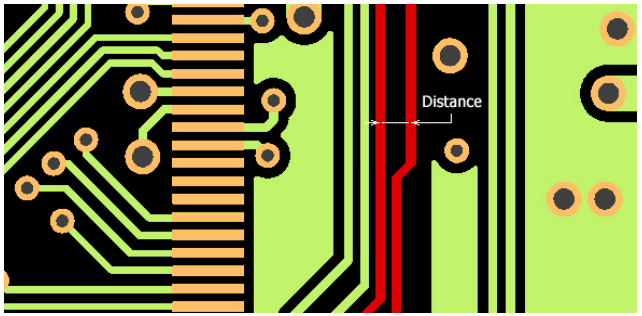
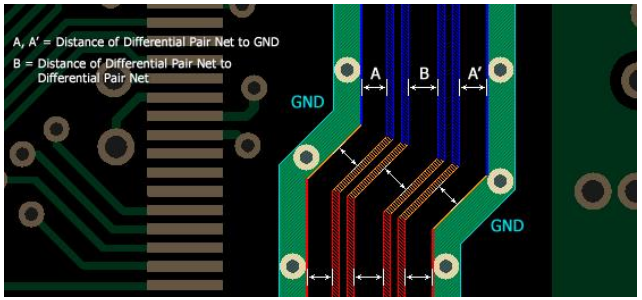
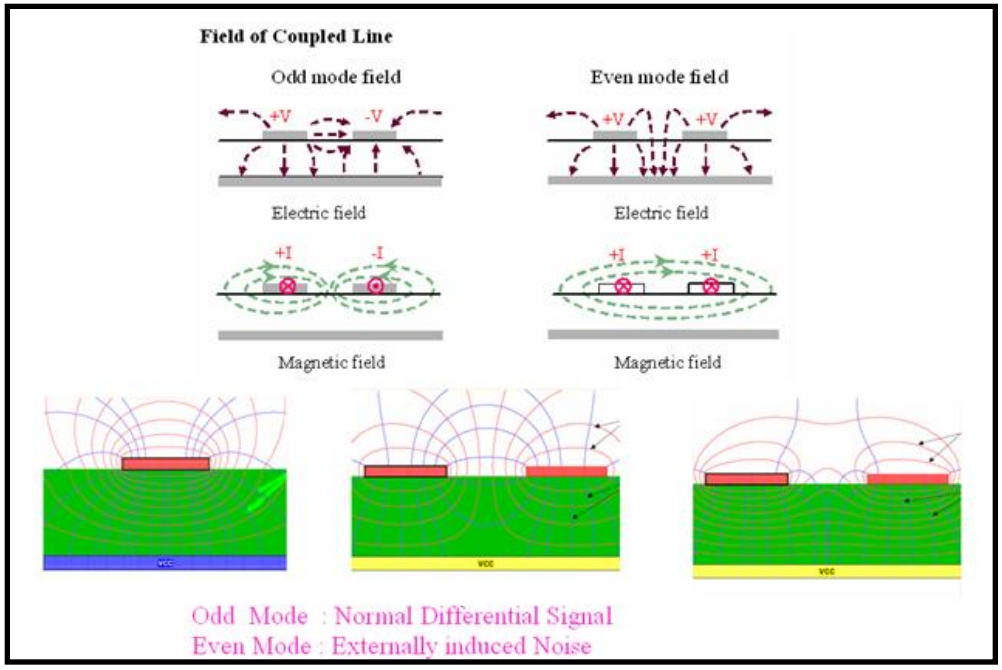
◆ Differential Signalling

- Length matching between P/N signals.







Item	Net	Start Comp	End Comp	Filter		Toleran...	Ratio(%)		Segment Distance	Pin Escape		TP	TP Distance	Nut Shape Anti-Pad	Except Layer
Item01					☐		80	☐	Minimum Distance	0	☐			Not Check	

Item	Net Group	Filter	GND Net Group	Pin Escape	Via Escape	Net Clearance	Shield Distance	Tolerance(%)	Show Segment .
Item01									☐

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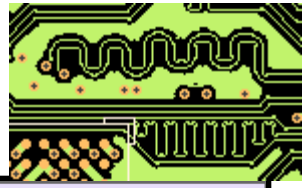
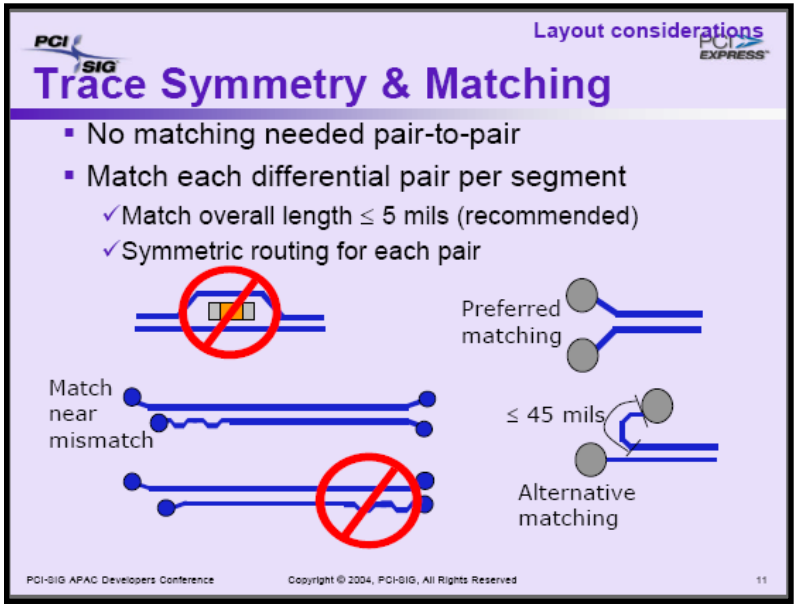
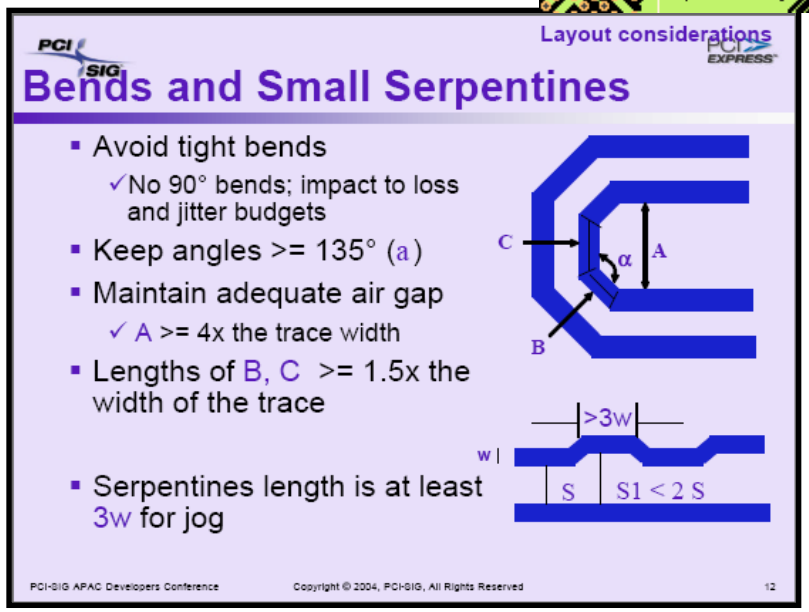
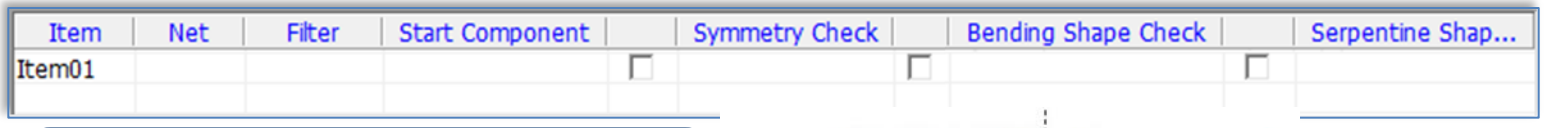
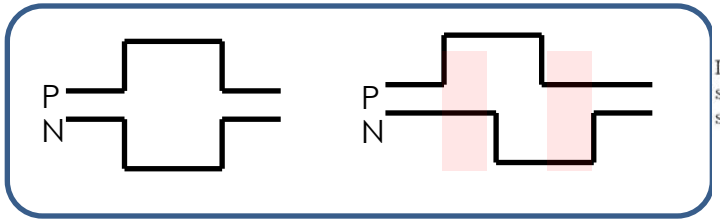
- **Serpentine**
  - Routing symmetry between strobe and data is Key.



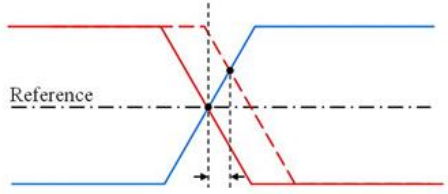








Differential signaling scheme



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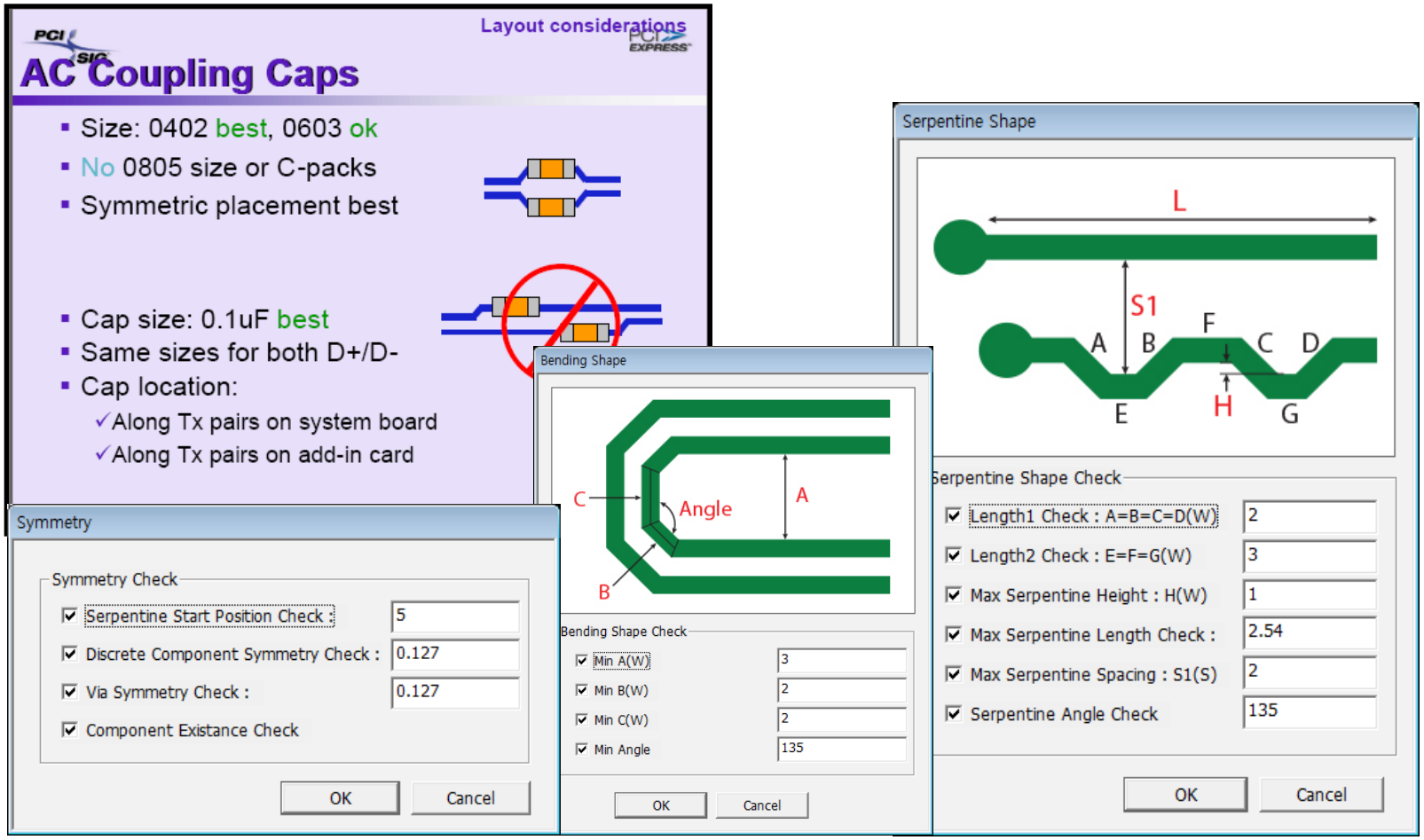
◆ Serpentine



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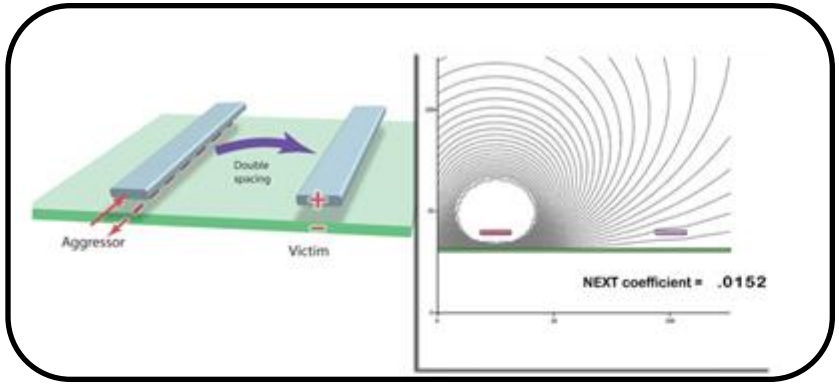
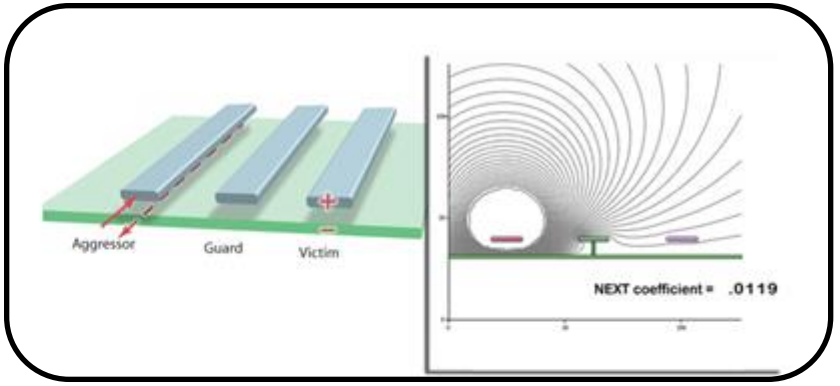
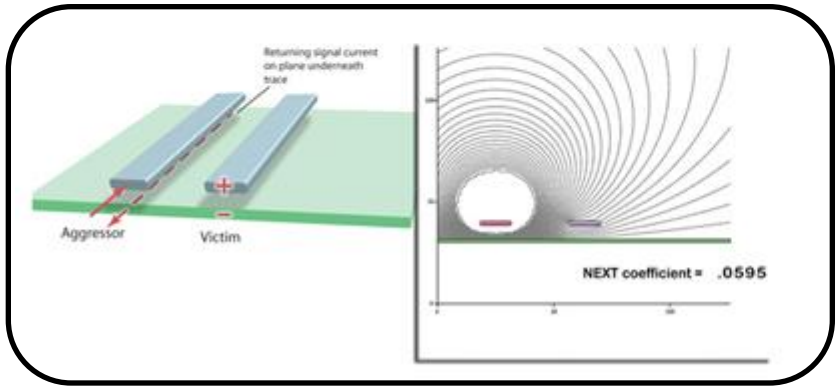
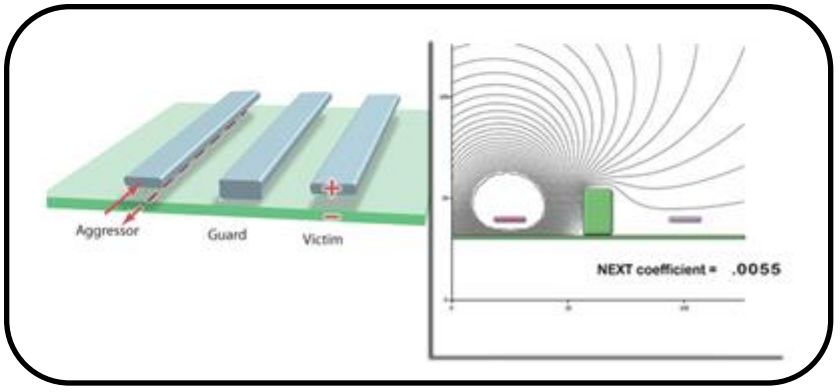
◆ Ground Barrier Effect

- Audio signal needs ground barrier in order to prevent noise coupling









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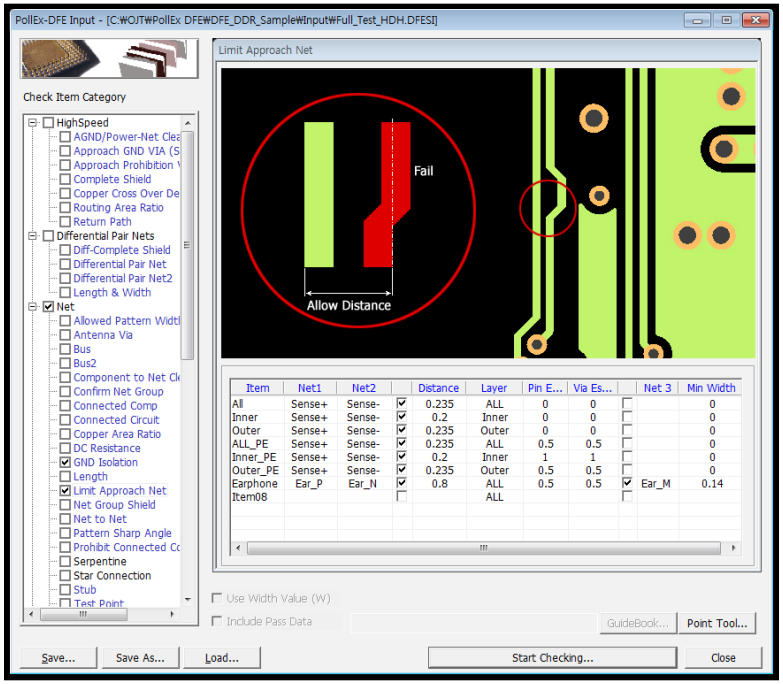
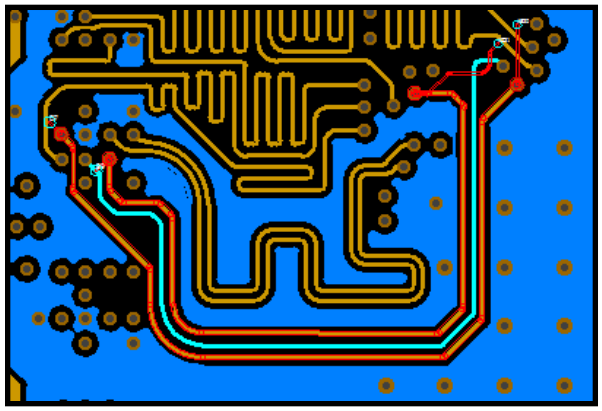
◆ Limit Approach Net



Check Items:

- Separation between Net1 and Net2.
- Ground barrier existence.
- Ground barrier minimum width.

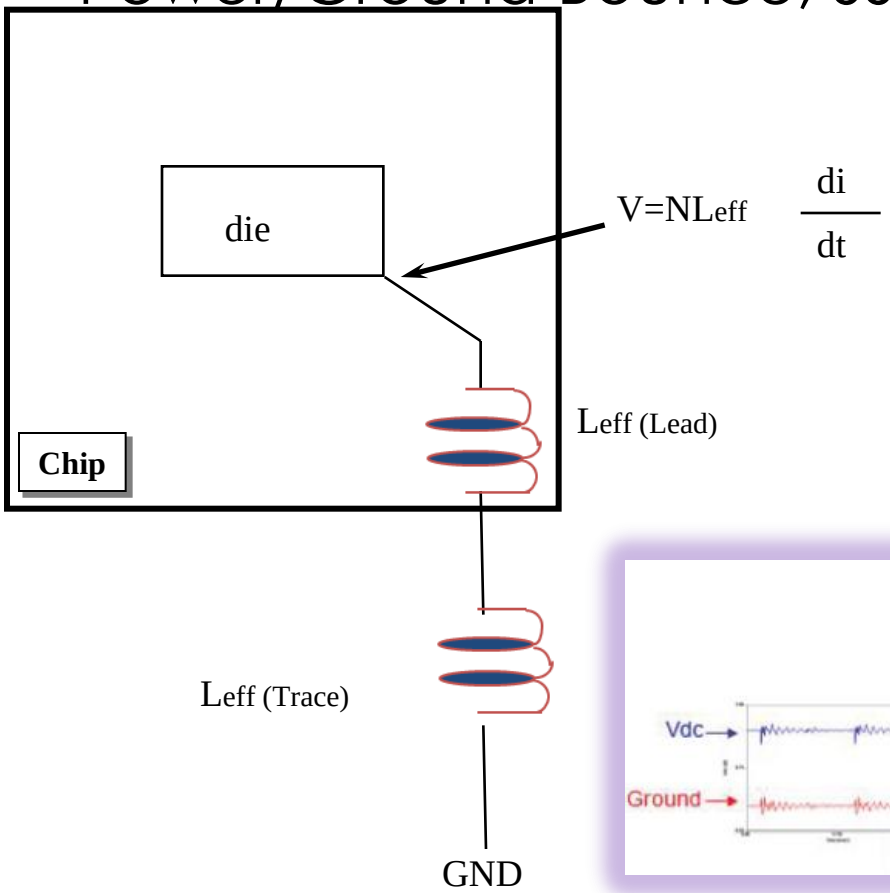


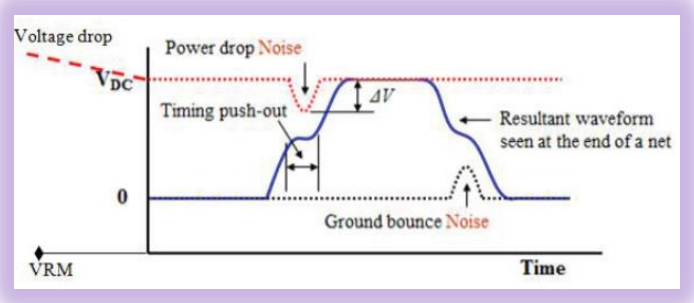
Item	Net1	Net2		Distance	Layer	Pin Escape	Via Escape		Net 3	Min Width
Item01			☐		ALL			☐		

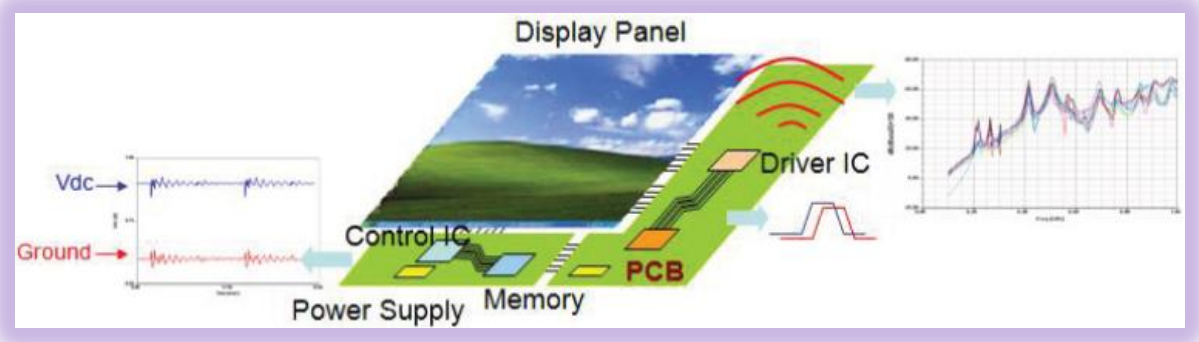
PollEx DFE

◆ Power Integrity

- Power/Ground Bounce, SSN/SSO







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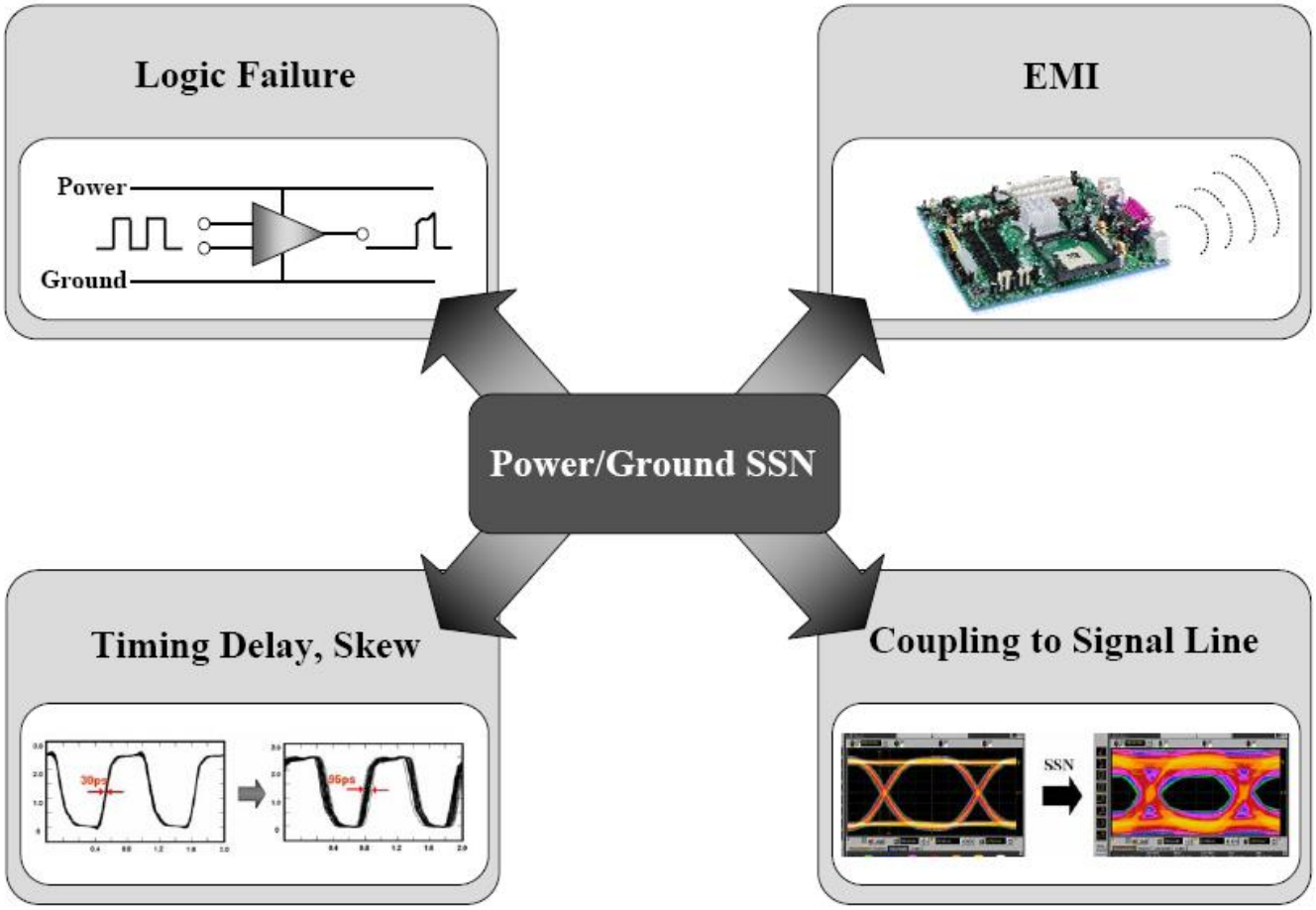
◆ Problems by Power/Ground SSN



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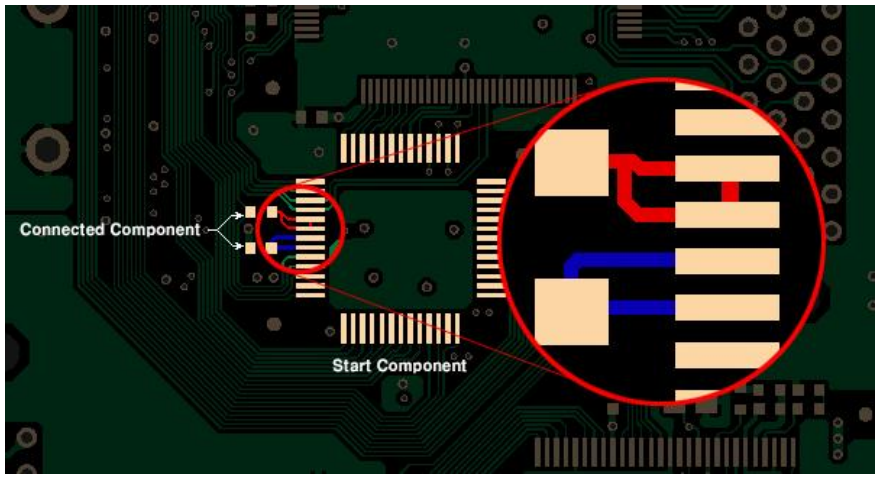
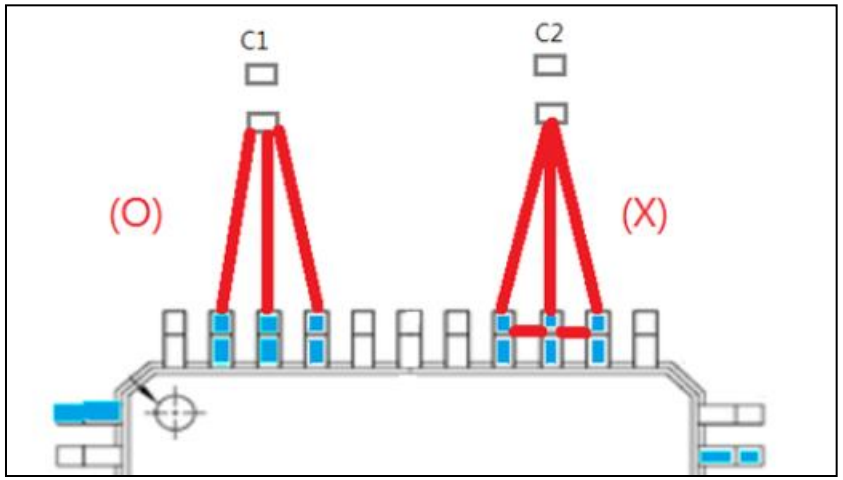
◆ Star Connection

- In case of sharing one capacitor, connection should be isolated .





Item	Star Component	Connected Component	Check Net
Item01			

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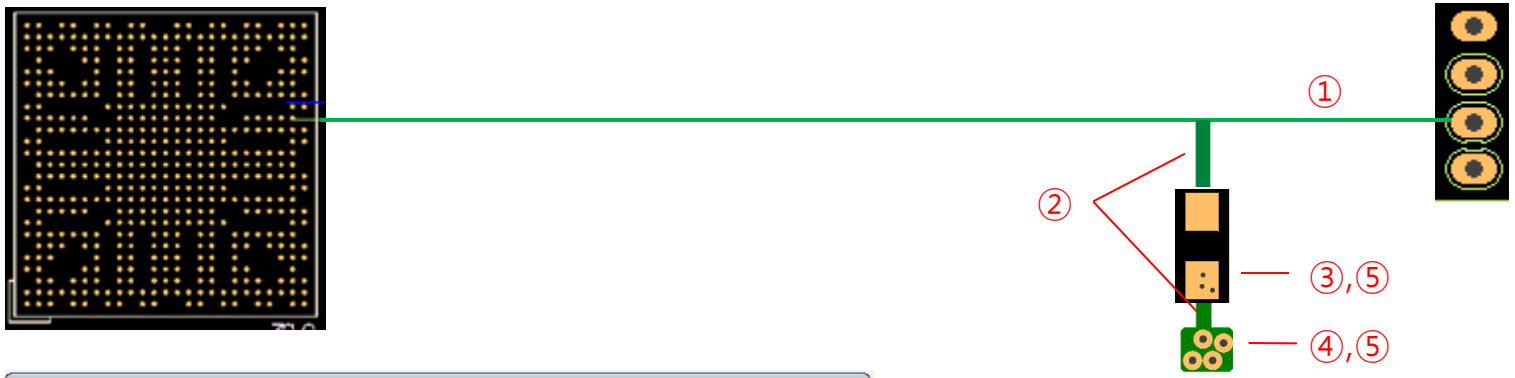
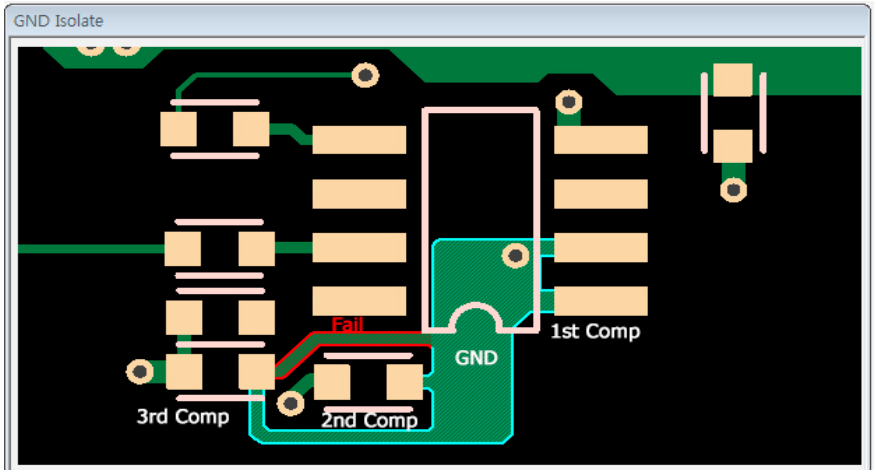
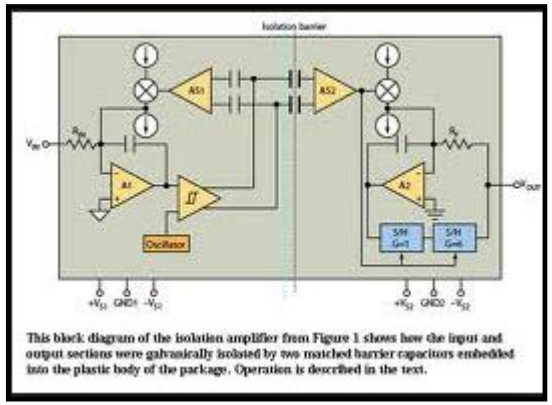
◆ GND Isolation

- ESD discharge path should be isolated and direct connect to main ground.





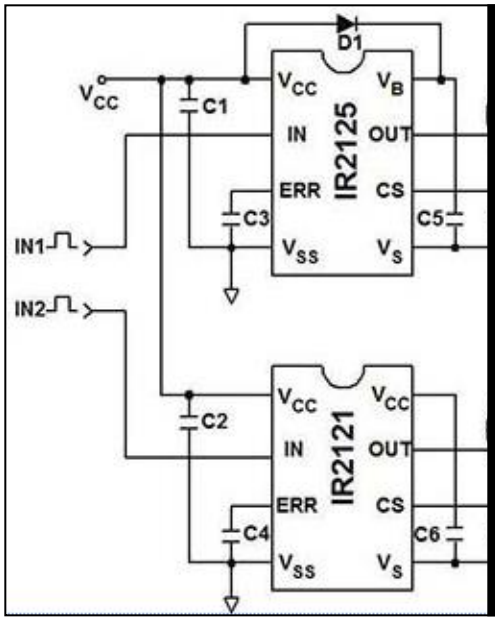


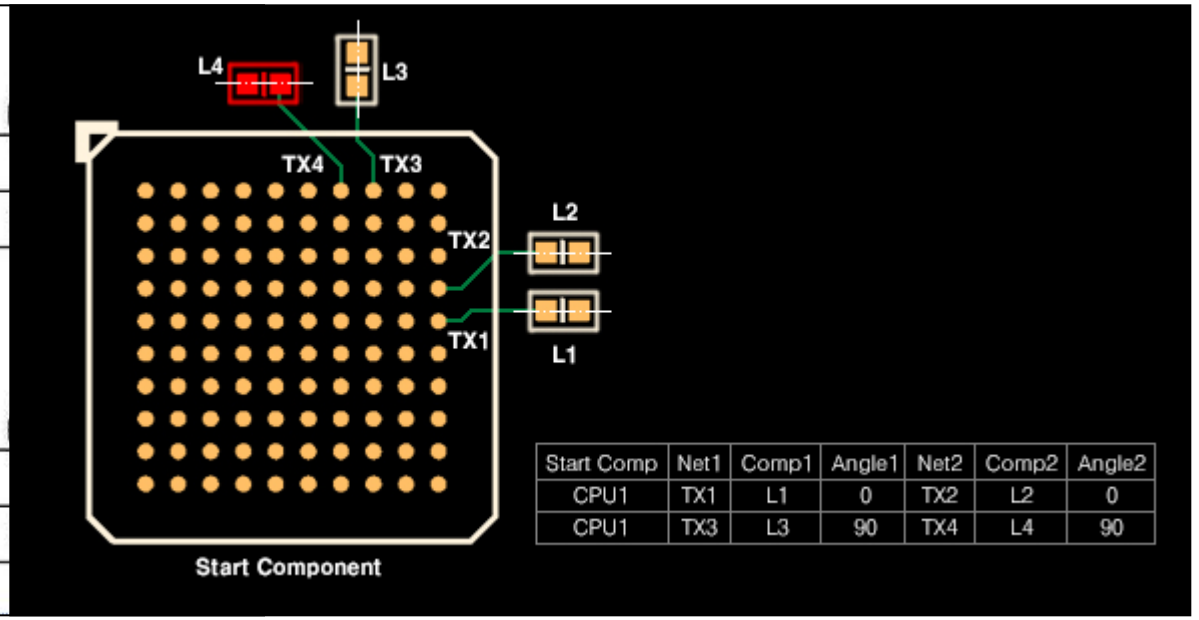
Item	Check Pins	MGND-Count	GND Isolation		Via Location	Distance
Item01			☐	☐		

PollEx DFE

◆ Component Direction

- Check passive devices' placement angles.



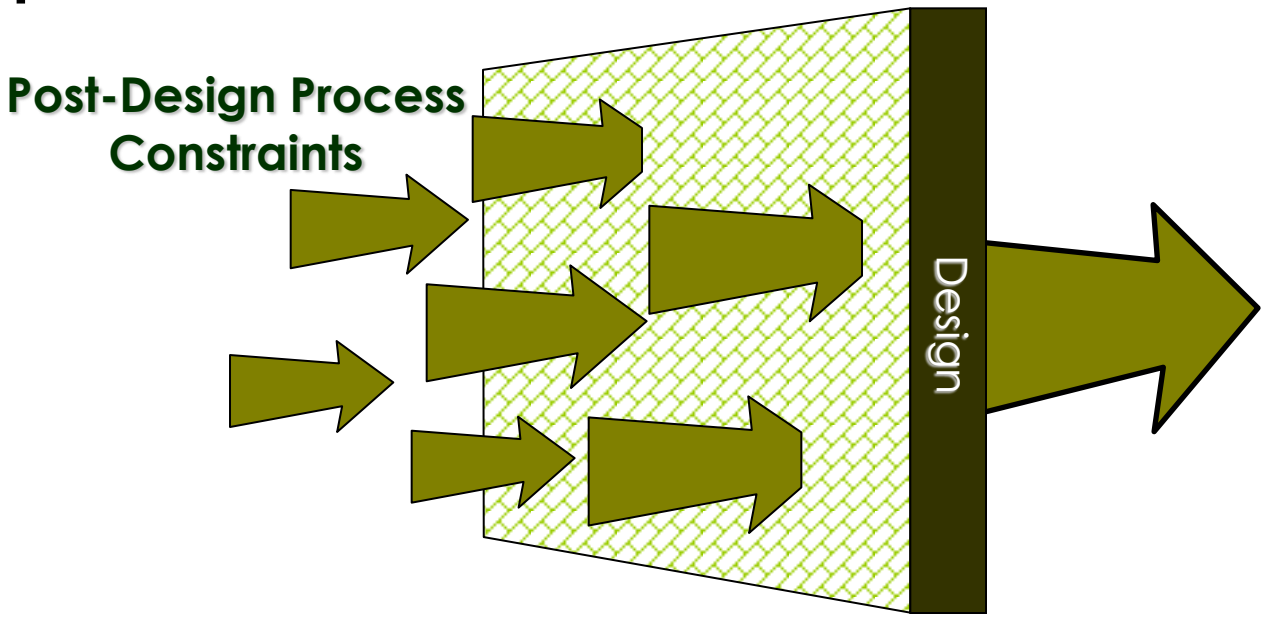


Start Comp	Net1	Comp1	Angle1	Net2	Comp2	Angle2
CPU1	TX1	L1	0	TX2	L2	0
CPU1	TX3	L3	90	TX4	L4	90

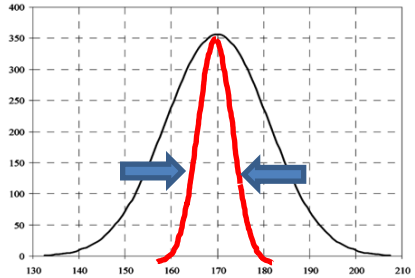
Item	Start Component	Angle	Net1	Comp1	Net2	Comp2
Item01						

PollEx DFE

◆ Expectation for PollEx DFE



Minimize Design Iterations



Consider engineering faults in early design stages.
→ Accumulate Knowledge for Engineering.
→ Save Time-Consuming Cost. (Time to Market)
→ Get Superior Competitive Power to Competitors.

Thank You !

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