# ST MCU is the leading Cortex-M based platform

STMicroelectronics

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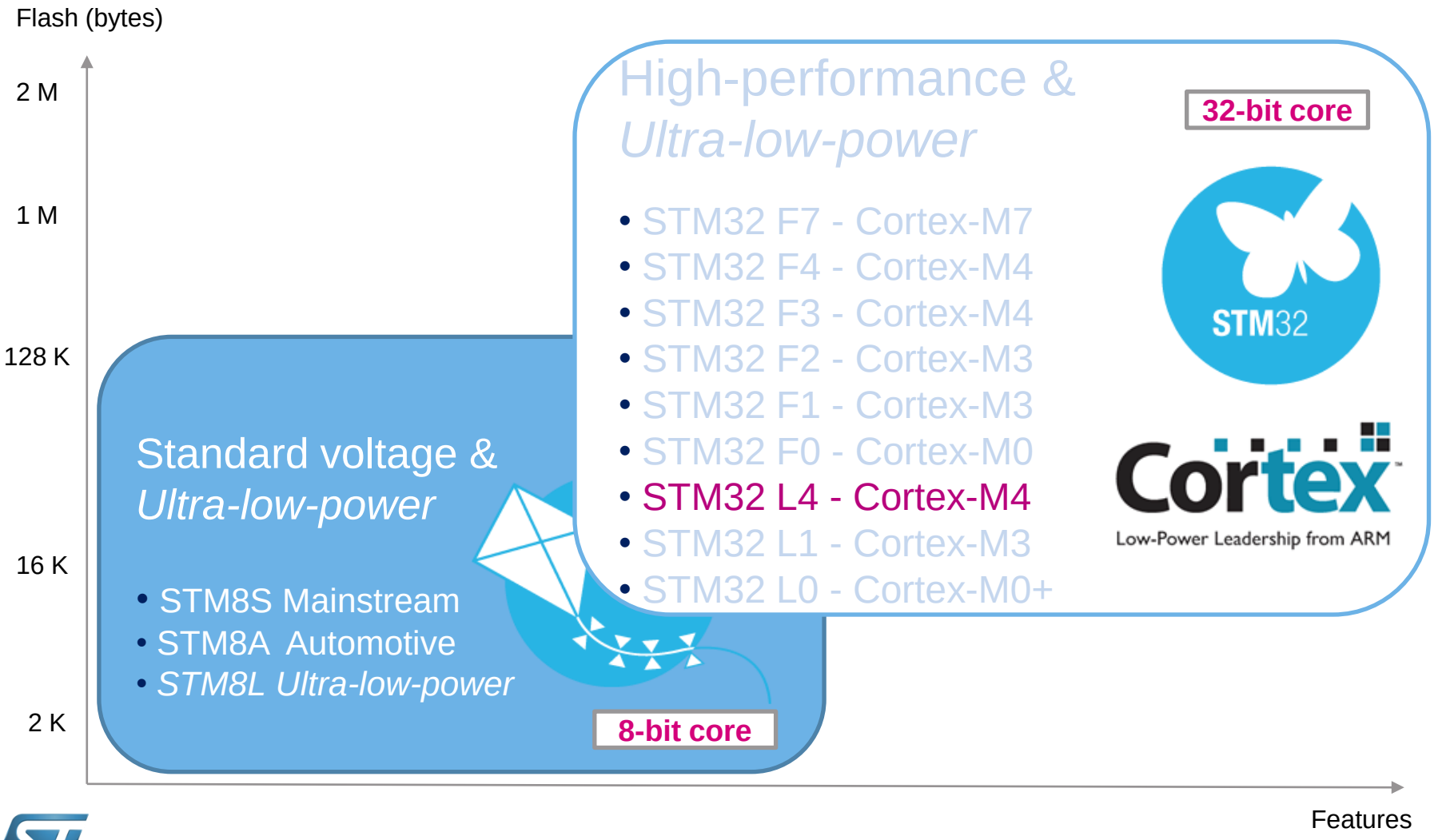
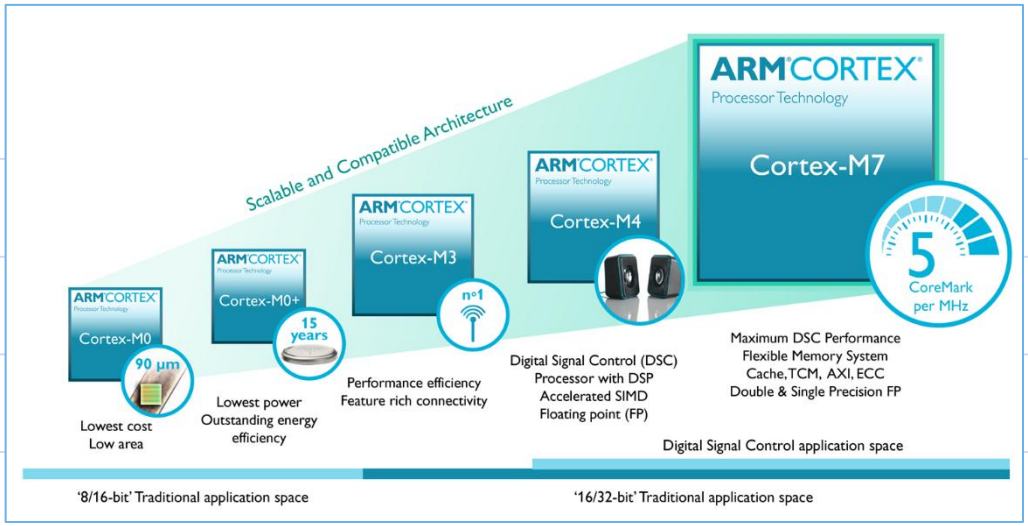
# MCUs – new families development focus





# STM32 DMIPS performance









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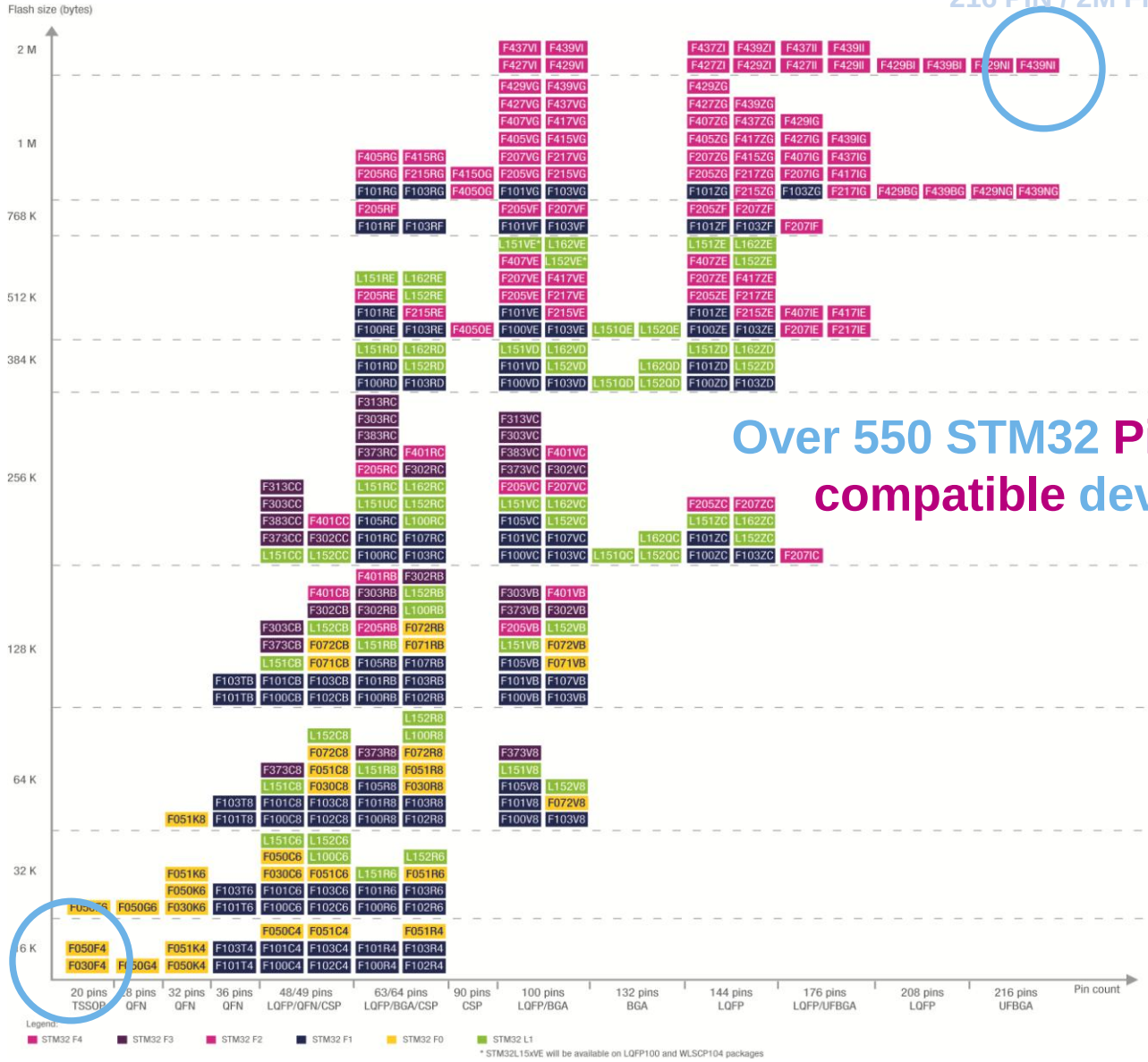
# A rich & reliable product base and…



216 PIN / 2M Flash /320KSRAM




**Over 550 STM32 Pin-to-pin compatible devices**

20 PIN / 16KFlash

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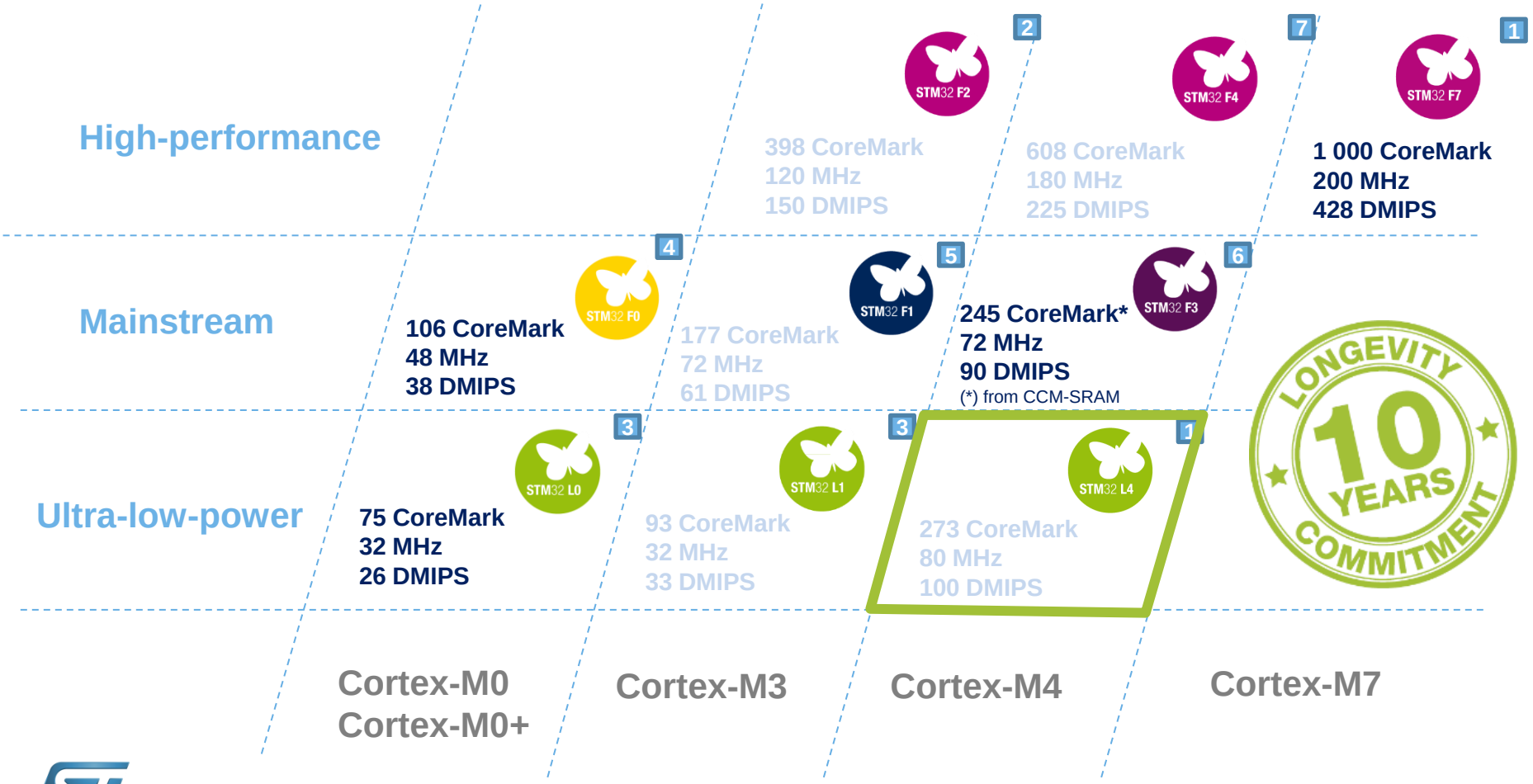
# STM32 L4 : continuity in STM32 portfolio



## 9 product series / 32 product lines



# STM32L ULP offer



**STM32L4 completes the ultra-low-power family**

## Cost-smart ULP Champion


Cortex-M0+ @ 32 MHz
Operating range:
1.65 to 3.6V
8/16-bit applications
Numerous pin counts

3 product lines,
Cost-effective,
Smaller packages
USB, LCD, Analog
16 to 192 Kbytes of Flash
Up to 20 Kbytes of SRAM

## Broad Range Foundation


Cortex-M3 @ 32 MHz
Operating range:
1.65 to 3.6V
Wide choice of memory sizes

3 product lines,
USB, LCD, AES,
Rich Analog
True EEPROM,
Dual bank Flash (RWW)
32 to 512 Kbytes of Flash
Up to 80 Kbytes of SRAM

## ULP with performance


Cortex-M4 w/ FPU @ 80 MHz
Operating range:
1.71 to 3.6V
Advanced Peripheral Performance

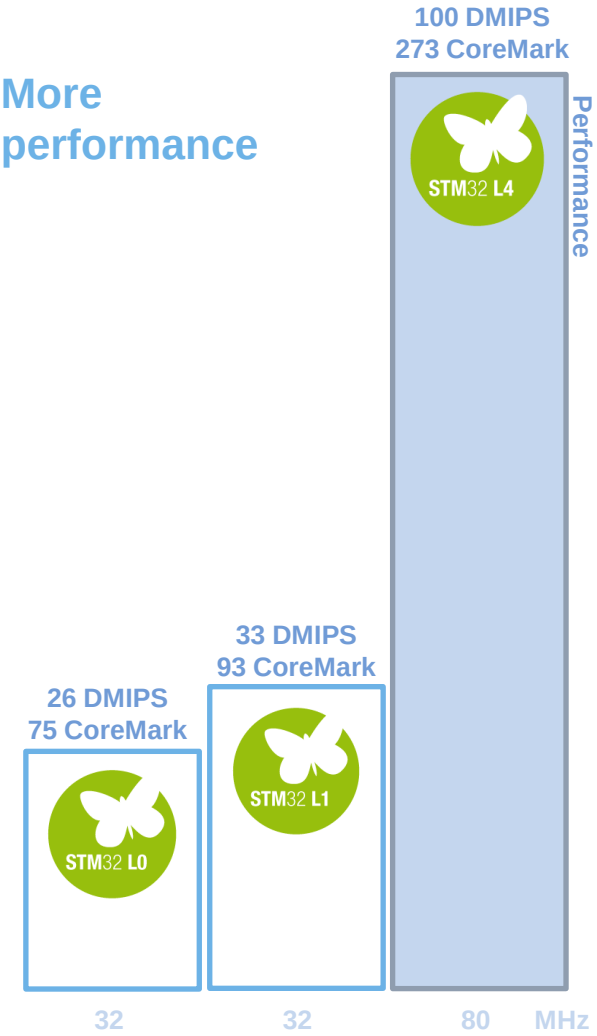
3 product lines,
ADC 5 Msps, PGA, Compar.,
DAC, op amp, USB OTG,
LCD, AES
256 Kbytes to 1 Mbyte of Flash
Up to 128 Kbytes of SRAM

# STM32L, a complete offer

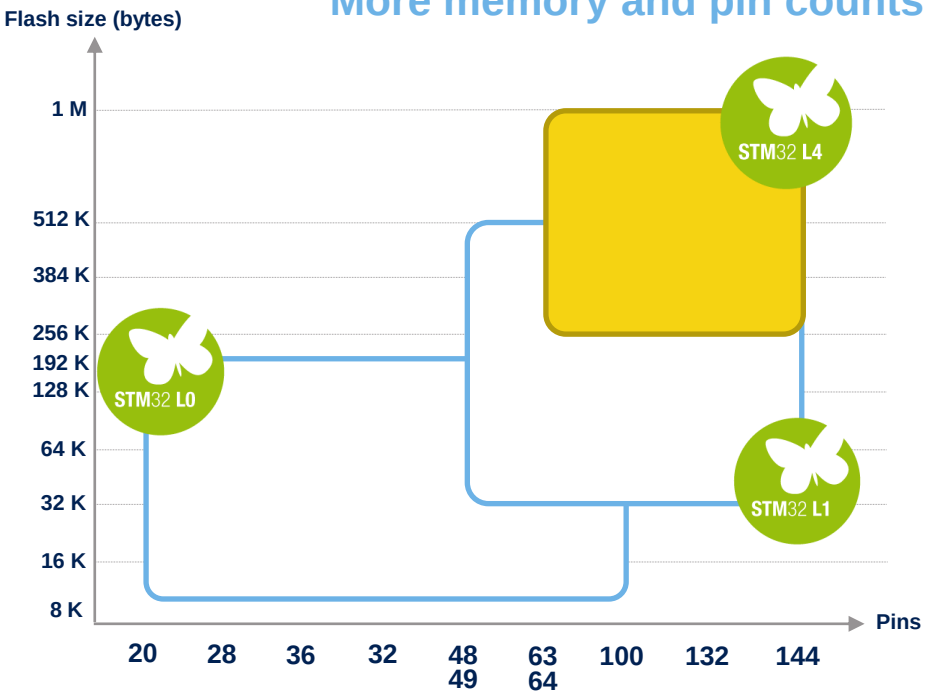


## STM32L4 completes the ultra-low-power family

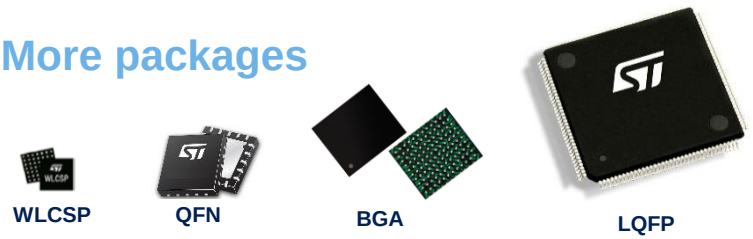
### More performance




### More memory and pin counts




### More packages

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# Ultra-Low-Power and Flexibility
## FlexPowerControl

**STM32L4 is based on a new platform optimized to reduce power consumption and increase flexibility**

**Down to 30 nA for I/O wake-up**
with additional Shutdown mode

**External level shifter no longer needed**
Separate $V_{DD}$ supplies (down to 1.08 V)

**RTC available for all power modes**
(from Active down to $V_{BAT}$)


**4 nA $V_{BAT}$ mode with charging capability**
Automatic switch to maintain power for RTC and backup registers

**Down to 360 nA keeping 32 Kbytes of SRAM active**
in Standby mode

**Wake up MCU with any peripheral**
(Communication I/Fs, analog circuits, timers …)

**USB capable with 32 kHz crystal oscillator**
(Dedicated crystal oscillator is no longer needed for USB function)

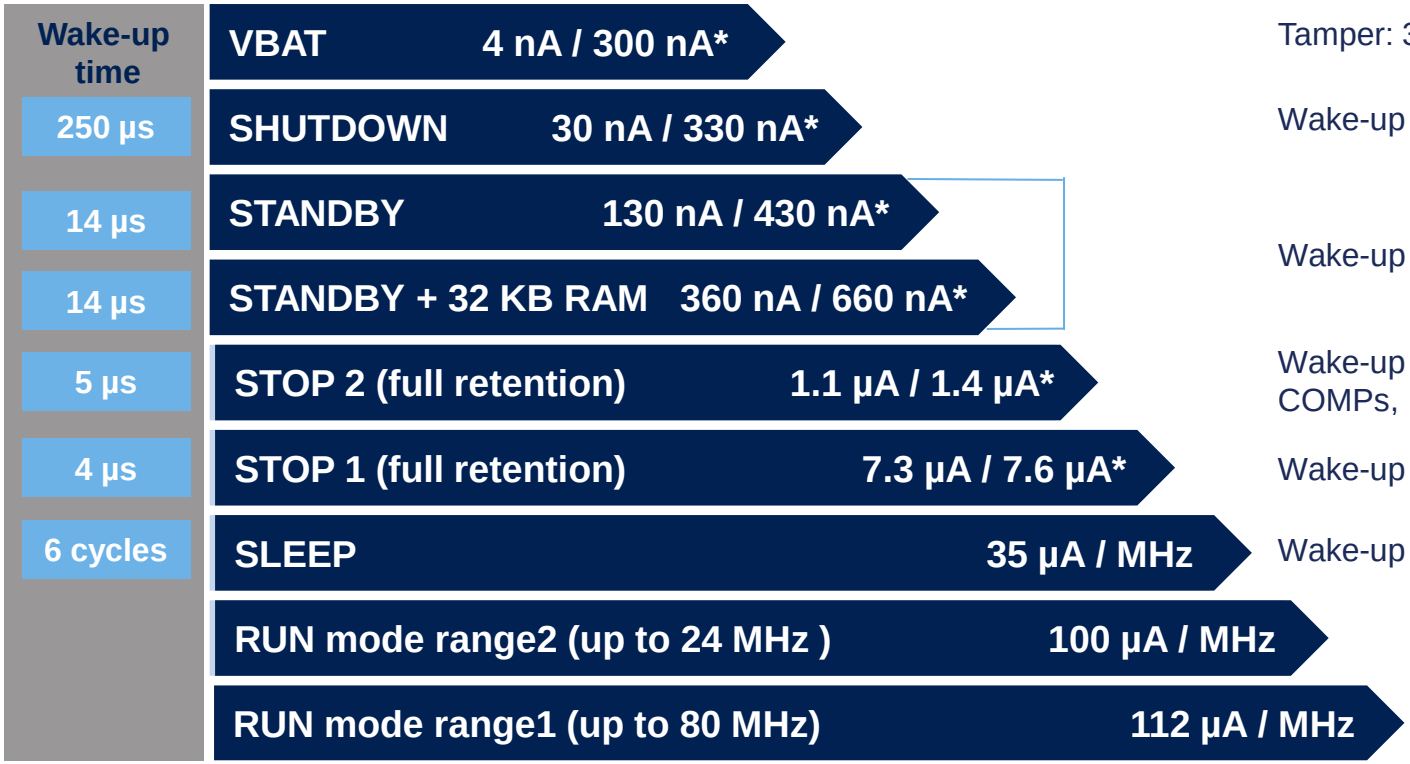
**I/O level kept in low power modes**
Optimization of system consumption

**Internal oscillator from 100 kHz to 48 MHz**
(+/-0.25% int. clock accuracy over voltage/temperature with 32 kHz crystal)

# Ultra-low-power modes



## Best power consumption numbers with full flexibility




Tamper: 3 I/Os, RTC

Wake-up sources: reset pin, 5 I/Os, RTC

Wake-up sources: + BOR, IWDG

Wake-up sources: + all I/Os, PVD, LCD, COMPs, I²C, LPUART, LPTIM

Wake-up sources: + all I²C, UART

Wake-up sources: any interrupt or event

Note : * without RTC / with RTC

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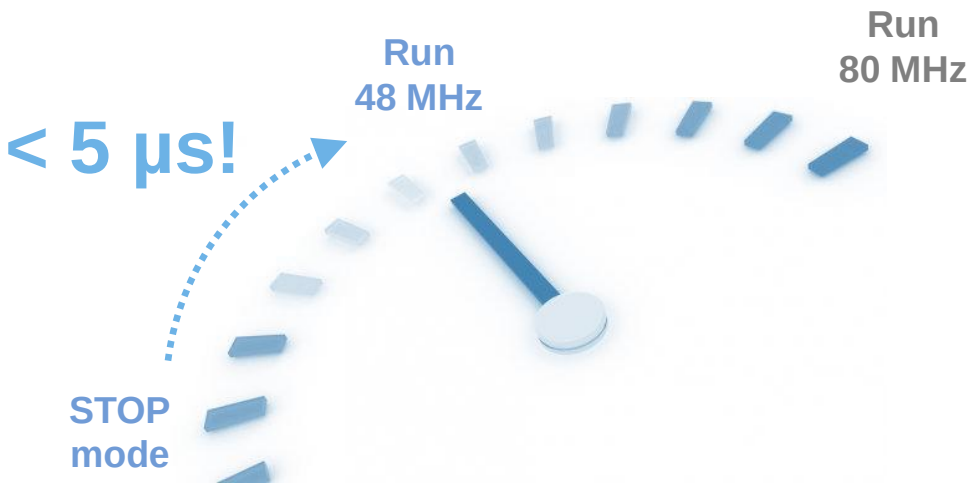
# Efficient run and fast wake-up



**Ready for Launch Control ? From 0 to 48 MHz in less than 5 µs**

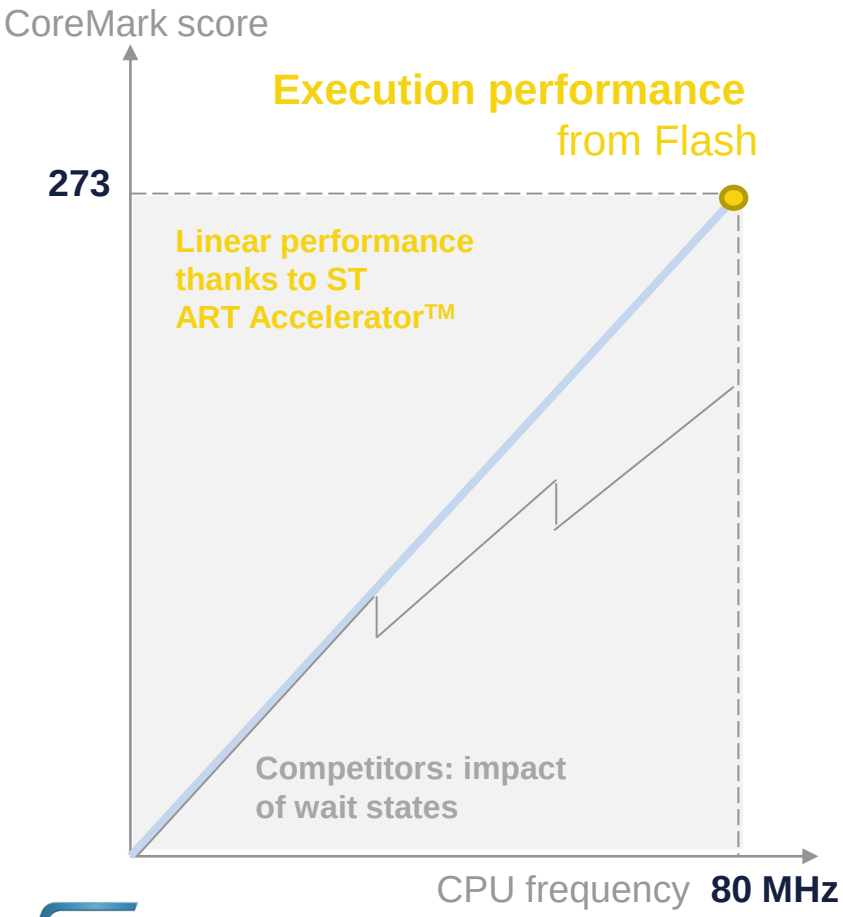
- Thanks to our internal oscillator (MSI) used at start-up (programmable from 100 kHz to 48 MHz)
- PLL wake-up time
  < 15 µs
  (needed to reach $f_{MAX}$)



# Providing **more performance**



## Do not compromise on performance with STM32L4




- **Up to 80** MHz/ **100 DMIPS** with ART Accelerator™
- **Up to 273** CoreMark Result
- ARM Cortex-M4 with DSP instructions and floating-point unit (FPU)
- Optimized DMA (14 channels)

# Smart peripherals
## Metering

**D**igital **F**ilter for **S**igma **D**elta **M**odulators
8 x parallel inputs
with up to 24-bit data
output resolution


**$V_{BAT}$ with RTC**
for battery backup
240 nA in $V_{BAT}$ mode
for RTC and
32x 32-bit backup registers

**TRNG & AES**
for Security
128-/256-bit AES
key encryption hardware
accelerator

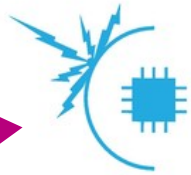

**FSMC**
External memory interface
for static memories supporting SRAM,
PSRAM, NOR and NAND

**STM32L4**



**Electricity/Gas /Water Smart Meter**

**LCD Display**
8×40 or 4×44
with step-up converter



**Anti Tamper pin**
3 x tamper pins
for battery domain

**SPI / UART/ SDIO for Wireless**
3x SPIs (4x SPIs with the Quad SPI)
6x USARTs (ISO 7816, LIN, IrDA, modem)
1 x SDIO

**I/Os** Up to 114 fast I/Os for buttons & relays

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# Smart peripherals

## Fitness tracker - Wristband

**D**igital **F**ilter for **S**igma **D**elta **M**odulators
with PDM (Pulse Density Modulation) microphone input support

### TFT Display

**FSMC**
Parallel interface to TFT
**SPI**
Up to 40 MHz speed

### STM32L4

### Sensors



**I²C**
3x I²C FM+(1 Mbit/s), SMBus/PMBus

**B**atch **A**cquisition **M**ode (BAM)

### SPI / UART

3x SPIs (4x SPIs with the Quad SPI)
6x USARTs (ISO 7816, LIN, IrDA, modem)

### SWP

Single wire protocol master interface (SWPMI)

### USB

USB OTG 2.0 full-speed, LPM and BCD

### OPAMP

2x op amp with built-in PGA

### DAC

2x 12-bit DAC, low-power sample and hold

### ADC

3× 12-bit ADC 5 MSPS, up to 16-bit with hardware oversampling, 200 µA/MSPS

### SAI

2x serial audio interfaces

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# Smart Peripherals
## Industrial



**Motor Control :**
2x 16-bit advanced
motor-control timers
3x 12-bit ADCs: 5 MSPS,
with up to 16-bit with hardware oversampling,
200 µA/MSPS

**LCD Display**
8×40 or
4×44
with step-up converter

**CAN** Bus
(2.0B Active)

**STM32L4**

**High temperature**
from -40°C
up to **125°C**

**TRNG & AES**
for Security
128/256-bit AES
key encryption hardware accelerator

**SPI / UART**
3x SPIs (4x SPIs with the
Quad SPI)
6x USARTs (ISO 7816, LIN,
IrDA, modem)


**FSMC**
External memory interface
for static memories supporting
SRAM, PSRAM, NOR and NAND

**I/Os**
Up to 114 GPIOs

**I²C**
3x I²C FM+(1 Mbit/s), SMBus/PMBus

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# High integration

## High integration with high memory size in small packages

Package size down to 4.4 x 3.8 mm

### Parallel Interface

FSMC 8-/16-bit
(TFT-LCD, SRAM, NOR, NAND)

### Display

LCD driver 8 x 40

### Timers

17 timers including:
2 x 16-bit advanced motor control timers
2 x ULP timers
7 x 16-bit-timers
2 x 32-bit timers

### I/Os

Up to 114 I/Os
Touch-sensing controller

**Cortex-M4**
**80 MHz**
**FPU**
**MPU**
**ETM**

DMA

ART Accelerator™

Up to
1-Mbyte Flash with ECC
Dual Bank

128-Kbyte RAM

### Connectivity

USB OTG,
1x SD/SDIO/MMC, 3 x SPI,
3 x I²C, 1x CAN, 1 x Quad SPI,
5 x USART + 1 x ULP UART,
1 x SWP

### Digital

AES (256-bit), TRNG, 2 x SAI,
DFSDM (8 channels)

### Analog

3 x 16-bit ADC, 2 x DAC,
2 x comparators, 2 x op amps
1 x temperature sensor

# Power management

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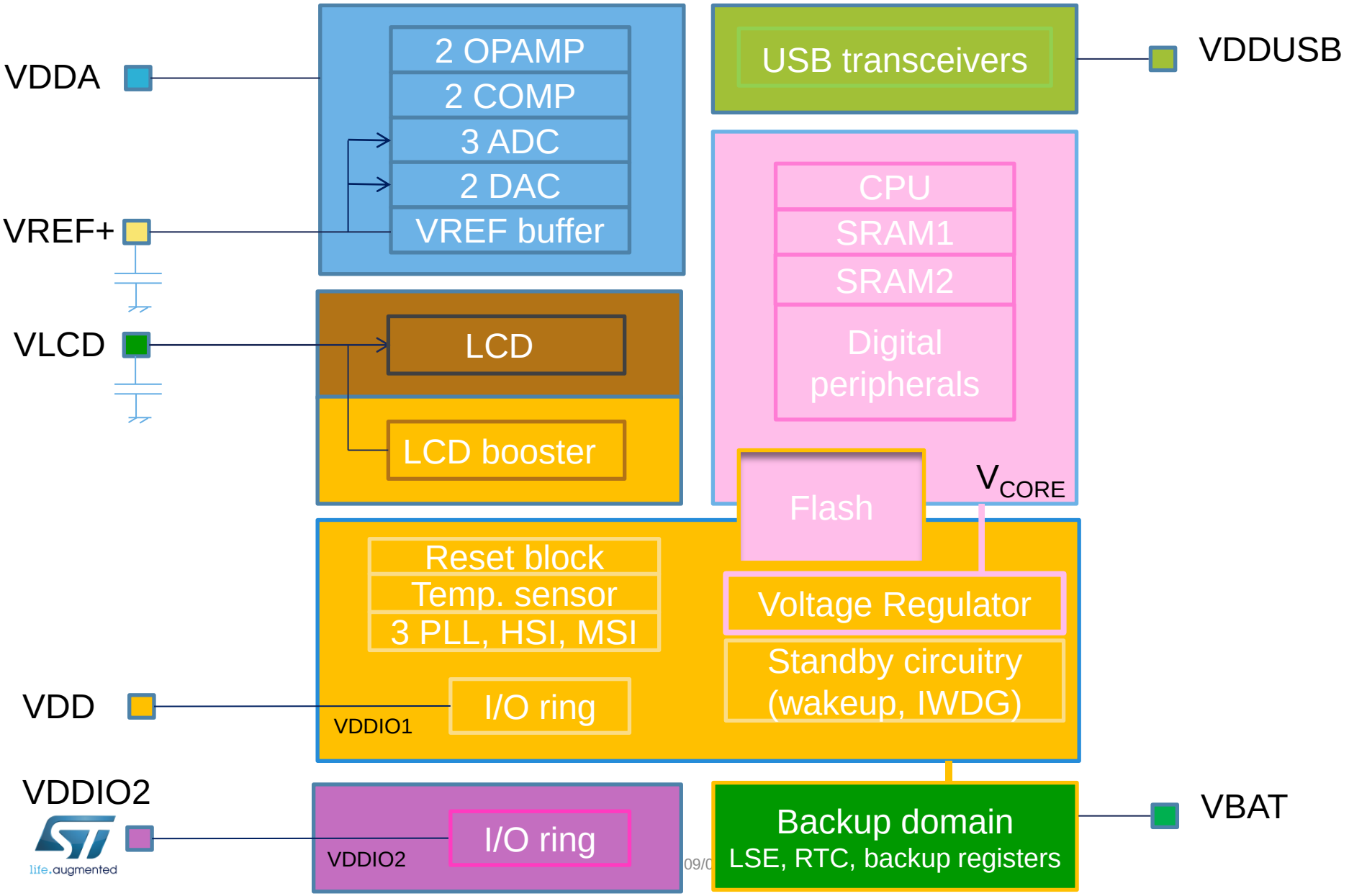
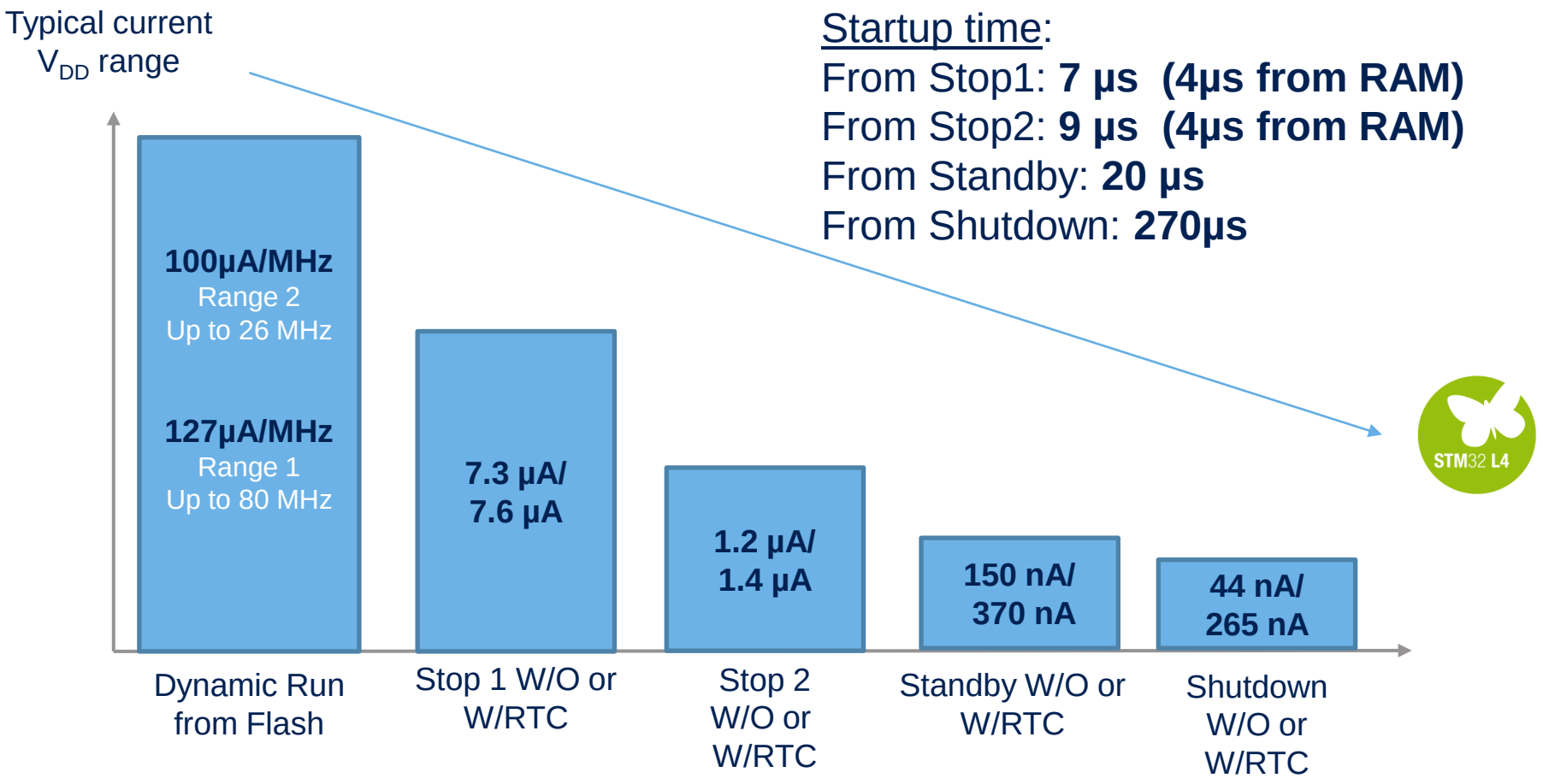
# Power schemes





# STM32 L4 power consumptions





# STM32L4 Power Mode

## Run mode

**Run Mode Range 1 :Execution from Flash**

Available Peripheral

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

Cortex M4

Flash (1MB)

SRAM 1 (96KB)

SRAM 2 (32KB)

Main regulator (MR)

Range 1 (up to 80MHZ)

Range 2 (up to 26MHZ)

Low Power regulator (LPR) up to 2MHz

Range 1
127uA/MHz at 80 MHz (10.2mA)

Range 2
111uA/MHz at 26 MHz (2.9 mA)

Available Clock

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell

Frozen cell

Cell in power-down

Available Periph and clock

# STM32L4 Power Mode

## Run mode

**Available Peripheral**

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

**Run Mode Range 2 : Execution from SRAM**

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)
- Main regulator (MR)
  - Range 1 (up to 80MHZ)
  - Range 2 (up to 26MHZ)
- Low Power regulator (LPR) up to 2MHz

Range 1 from SRAM1 127uA/MHz at 80 MHz (10,2 mA)

Range 2 from SRAM1 111uA/MHz at 26 MHz (2,9 mA)

**Available Clock**

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

# STM32L4 Power Mode

## Low-power run mode

**Available Peripheral**

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

**Execution from Flash**

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

- Main regulator (MR)
- Range 1 (up to 80MHZ)
- Range 2 (up to 26MHZ)
- Low Power regulator (LPR) up to 2MHz

from Flash
136 µA/MHz at 2 MHz (272 µA)

From SRAM1
121 µA/MHz at 2 MHz (242 µA)

**Available Clock**

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

# STM32L4 Power Mode

## Sleep mode

**Available Peripheral**

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

**Sleep Mode Range 1**
**Ex: Flash ON, SRAMs ON (default)**


Cortex M4

Flash (1MB)

SRAM 1 (96KB)

SRAM 2 (32KB)

Main regulator (MR)

Range 1 (up to 80MHZ)

Range 2 (up to 26MHZ)

Low Power regulator (LPR) up to 2MHz

Range 1
37 µA/MHz at 80 MHz
(2,96 mA)

Range 2
35 µA/MHz at 26 MHz
(0,92 mA)

**Available Clock**

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell

Frozen cell

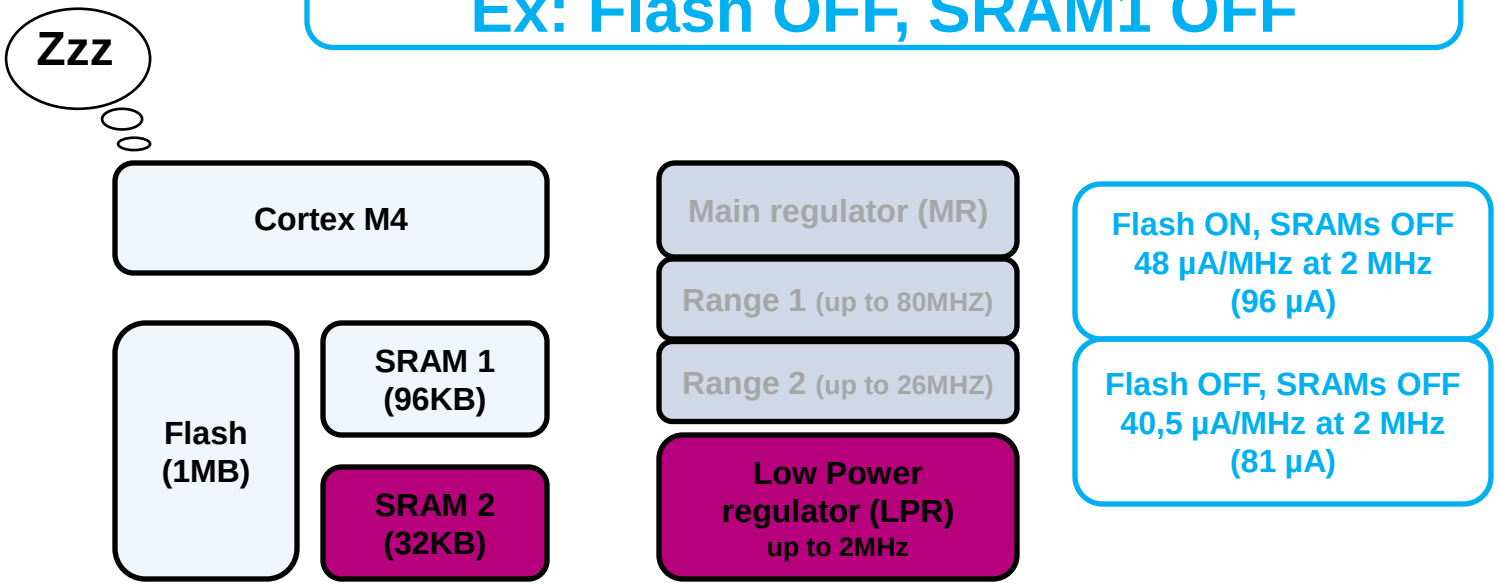
Cell in power-down

Available Periph and clock

# STM32L4 Power Mode

## Low-power sleep mode

**Low-power sleep mode**
**Ex: Flash OFF, SRAM1 OFF**




**Available Peripheral**

- GPIO
- DMA
- FSMC
- QUADSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

**Available Clock**

- HSI
- HSE
- LSI
- LSE
- MSI

Active cell | Frozen cell | Cell in power-down | Available Periph and clock

# STM32L4 Power Mode

## Stop 1 Mode

**Available Peripheral**

I/Os kept, and configurable

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

**Stop 1 w/ RTC on LSE quartz** ⇨ **7.9 µA @3.0V**
**7.6 µA @1.8V**

Zzz

- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

- Main regulator (MR)
- Low Power regulator (LPR)
- Backup domain
  - Backup Register (32x32-bits)
  - RTC

**Available Clock**

- HSI
- HSE
- LSI
- LSE
- MSI

**Wake-up event**

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SWPMI
- COMP
- LPTIM 1
- LPTIM 2
- IWDG
- GPIOs

6us wake-up from Flash
4us wake-up from RAM

# STM32L4 Power Mode

## Stop 2 Mode

**Available Peripheral**

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

I/Os kept, and configurable

**Stop 2 w/ RTC on LSE quartz** ⇨ **1.66 µA @3.0V**
**1.43 µA @1.8V**


- Cortex M4
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)

Main regulator (MR)

- Low Power regulator (LPR)
- Backup domain
  - Backup Register (32x32-bits)
  - RTC

**Available Clock**

- HSI
- HSE
- LSI
- LSE
- MSI

**Wake-up event**

- NRST
- BOR
- PVD
- PVM
- RTC + Tamper
- LCD
- LP UART
- I2C 3
- COMP
- LPTIM 1
- IWDG
- GPIOs

7us wake-up from Flash
5us wake-up from RAM

# STM32L4 Power Mode

## Standby Mode

**Available Peripheral**

- GPIO
- DMA
- FSMC
- QSPI
- **BOR**
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- **IWDG**
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

**I/Os can be configured**
**w/ or w/o pull-up**
**w/ or w/o pull-down**

**Standby w/ RTC on LSE quartz**

**674 nA @ 3.0V**
**433 nA@ 1.8V**

Zzz

Cortex M4

Main regulator (MR)

Flash (1MB)

SRAM 1 (96KB)

SRAM 2 (32KB)

Low Power regulator (LPR)

**Backup domain**

**Backup Register (32x32-bits)**

**RTC**

**Available Clock**

- HSI
- HSE
- **LSI**
- **LSE**
- MSI

**Wake-up event**

- **NRST**
- **BOR**
- **RTC + Tamper**
- **IWDG**
- **5 WKUP pins**

**14 us wake-up**

# Shutdown mode : NEW!



- Similar to standby mode but
  - NO power monitoring: no BOR, no switch to VBAT
  - NO LSI , no IWDG
  - BOR reset is generated when exiting Shutdown mode

    => all registers except those in Backup domain are reset.

    => reset generated on the pad
- 128 bytes backup registers
- Wakeup sources : 5 wakeup pins, RTC
- Wakeup clock is MSI 4 MHz.

# STM32L4 Power Mode

## Shutdown Mode

**Available Peripheral**

- GPIO
- DMA
- FSMC
- QSPI
- BOR
- PVD, PVM
- LCD
- USB OTG
- USART
- LP UART
- I2C 1 / I2C 2
- I2C 3
- SPI
- CAN
- SDMMC
- SWPMI
- SAI
- DFSDM
- ADC
- DAC
- OPAMP
- COMP
- Temp Sensor
- Timers
- LPTIM 1
- LPTIM 2
- IWDG
- WWDG
- Systick Timer
- Touch Sens
- RNG
- AES
- CRC

**I/Os can be configured**
**w/ or w/o pull-up**
**w/ or w/o pull-down**
**But floating when exit from Shutdown**

**Shutdown w/ RTC on LSE quartz** → **476 nA @ 3.0V**
**265 nA @ 1.8V**


- Cortex M4
- Main regulator (MR)
- Flash (1MB)
- SRAM 1 (96KB)
- SRAM 2 (32KB)
- Low Power regulator (LPR)
- Backup domain
  - Backup Register (32x32-bits)
  - RTC

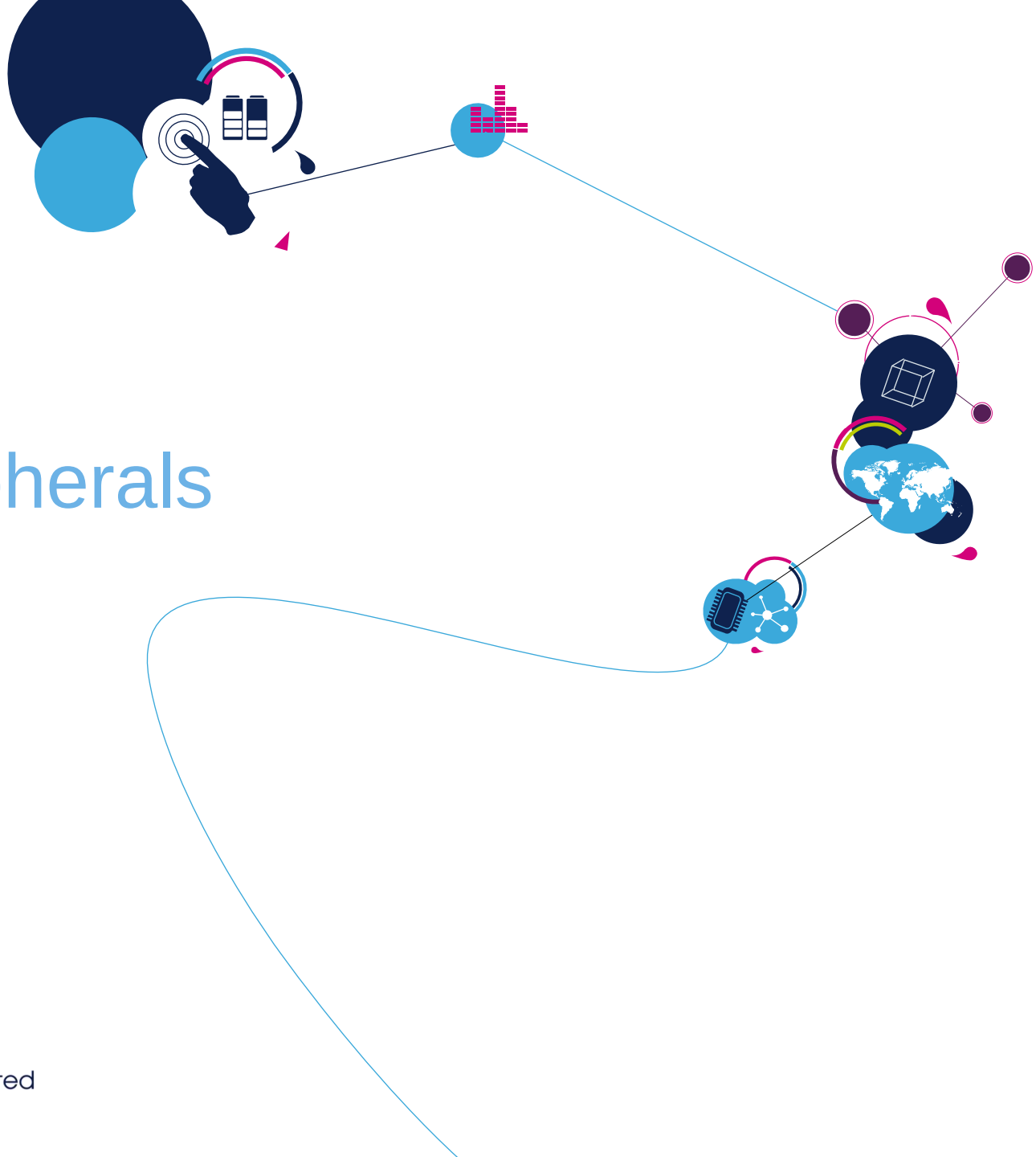
**Available Clock**

- HSI
- HSE
- LSI
- **LSE**
- MSI

**Wake-up event**

- NRST
- RTC + Tamper
- 5 WKUP pins

**250 us wake-up**



# New peripherals

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# Analog-to-digital converter (ADC)

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# ADC Features

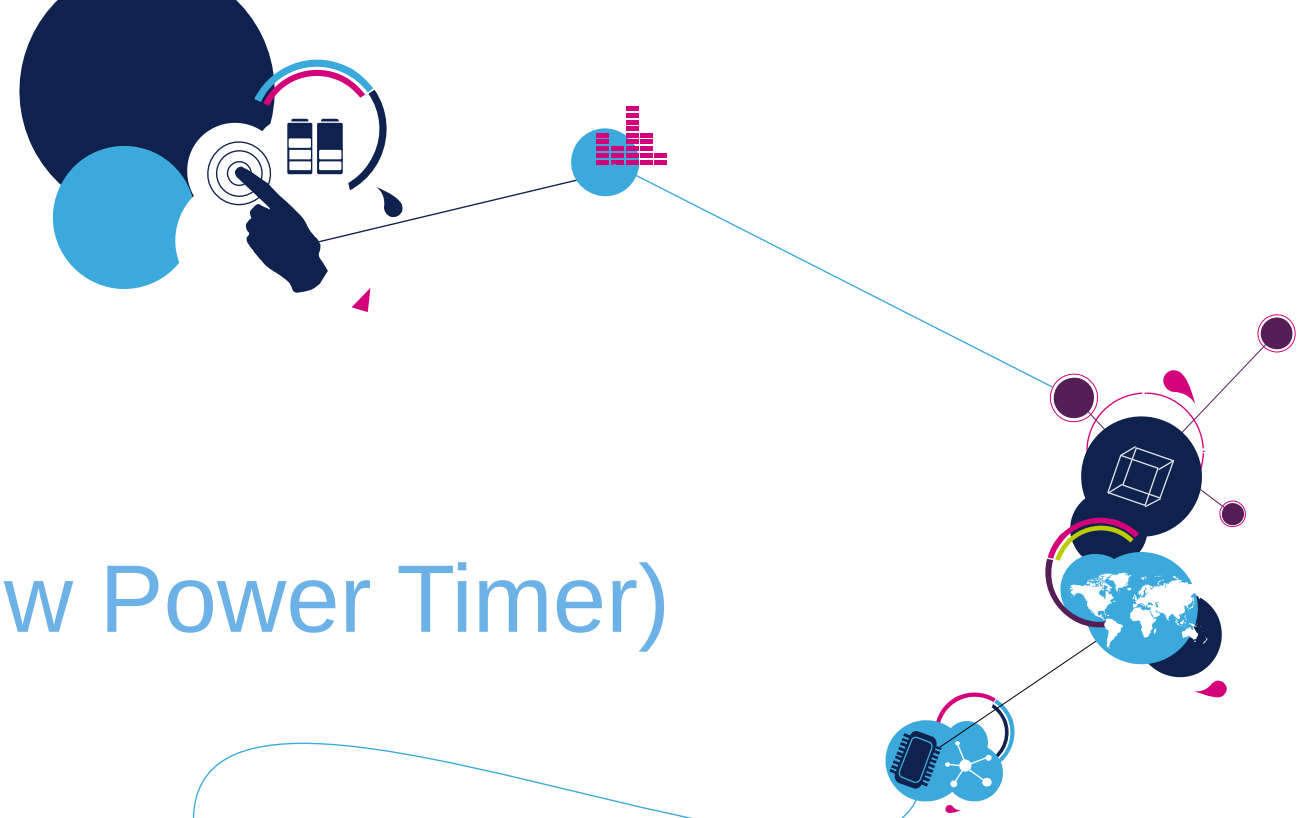


- Up to 3 ADCs:
  - ADC1 & ADC2 are  tightly coupled and can operate in dual mode (ADC1 is master)
  - ADC3 is standalone, but it share the interface with ADC1 & 2
- Programmable Conversion resolution : 12, 10, 8 or 6 bit
- Low power design
  - Consumption linear vs. conversion rate : 200 µA / MSps
  - ADC speed independent from CPU frequency (dual clock architecture)
- ADC conversion time:
  - Fast channels : up to 5.3Ms/s with 12 bit resolution in single mode
  - Slow channels: up to 4.8Ms/s with 12 bit resolution in single mode
- Channel-wise programmable sampling time
- External Analog Input Channels for each of the 3 ADCs:
  - 5 fast channels from dedicated GPIOs pads
  - Up to 11 slow channels from dedicated GPIOs pads
- Can manage Single-ended or differential inputs

# ADC STM32L1xx VS STM32L4xx



| | STM32L1xx | STM32L4xx |
|---|---|---|
| ADC clock frequency | Max. 16MHz | Max. 80MHz |
| 12-bit sampling rate | Max. 1Msps | Max. 5.33Msps |
| Sampling time | Min. 0.25µs | Min. 0.03124µs |
| Total conversion time | 1us ~ 24.75µs | 0.18us ~ 8.16µs |
| $I_{VDDA}$ (typical) | 1000µA | 950µA |



# LPTIM(Low Power Timer)

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# LPTIM(Low Power Timer) (1/3)

- Asynchronous running capability

- Ultra low power-consumption


- Timeout function for wakeup from low power modes

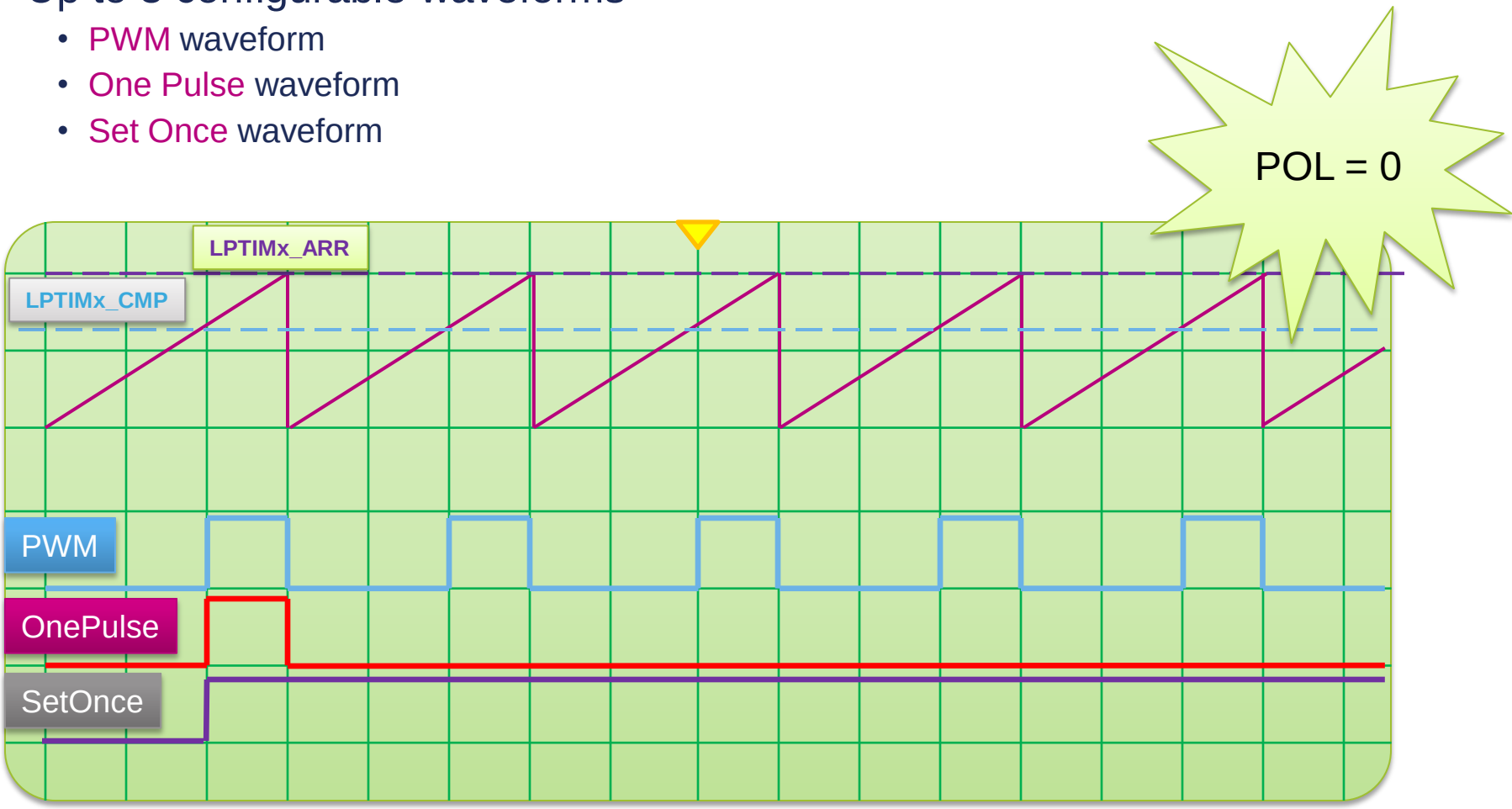
# LPTIM(Low Power Timer) (2/3)



- Up to 5 clock sources to achieve lowest power consumption
  - APB clock
  - LP oscillators: LSE, LSI, HSI
  - External clock
    - With configurable active edge: Rising edge, Falling edge and Both edges
    - When both edges configuration is chosen, an auxiliary clock source is needed with a frequency 4 times bigger, at least, than the external signal
- Up to 8 external triggers
  - With configurable active edges: Rising edge, Falling edge and Both edges
  - With digital glitch filter to avoid spurious triggers
- Up to 2 operation modes
  - Continuous mode: free running mode; many counter overruns are possible
  - One Shot mode: Counter stops counting when the overrun value is reached

# LPTIM(Low Power Timer) (3/3)

- Up to 3 configurable waveforms
  - PWM waveform
  - One Pulse waveform
  - Set Once waveform



# Low Power UART
# LPUART

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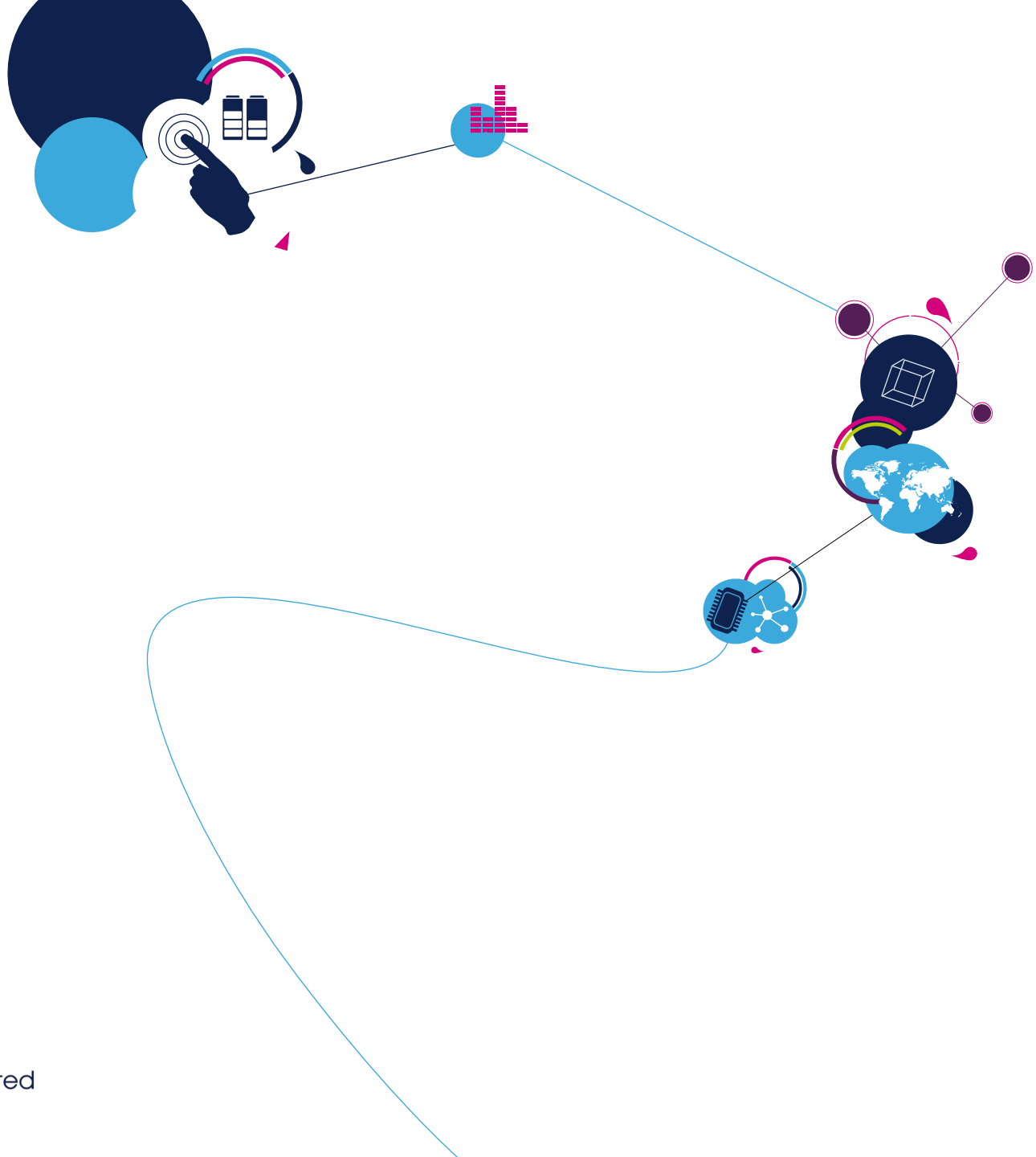
# LPUART (Low Power Universal Asynchronous Receiver Transmitter )

- LPUART includes all necessary hardware support to make asynchronous serial communications possible with minimum power consumption.
- Only LSE 32.768 is required to allow UART communication at up to 9600 baud → For this purpose, the baudrate generation has been changed comparing to the USART peripheral.
- Higher baudrates can be reached when the LPUART is clocked by clock sources different from the LSE clock.



# QuadSPI

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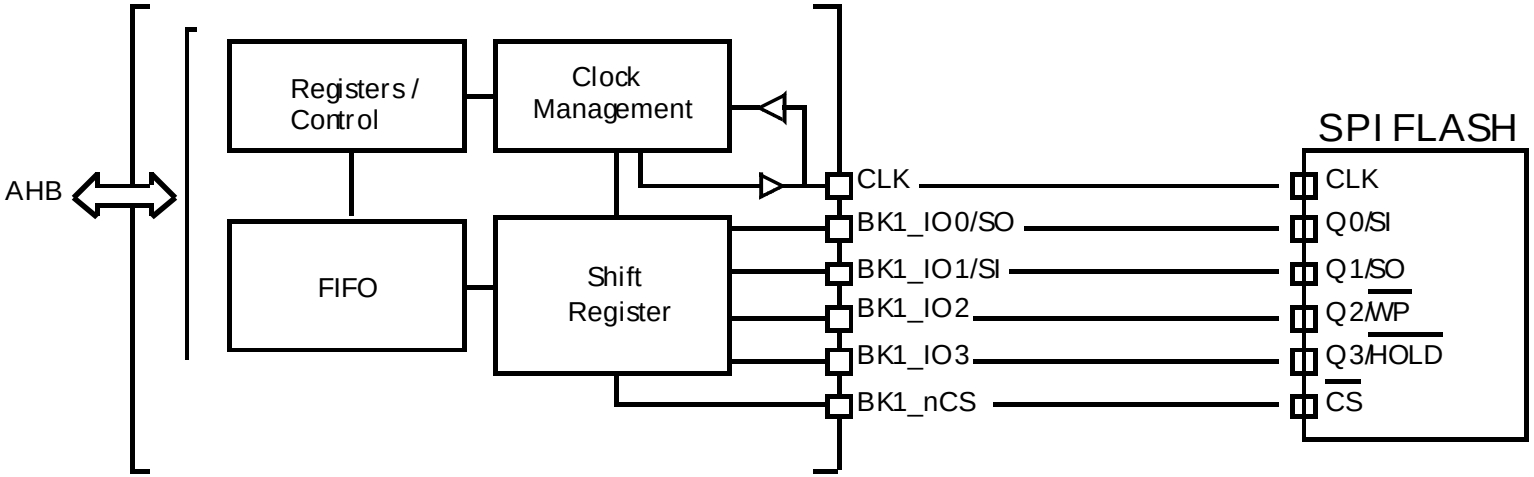
# Overview



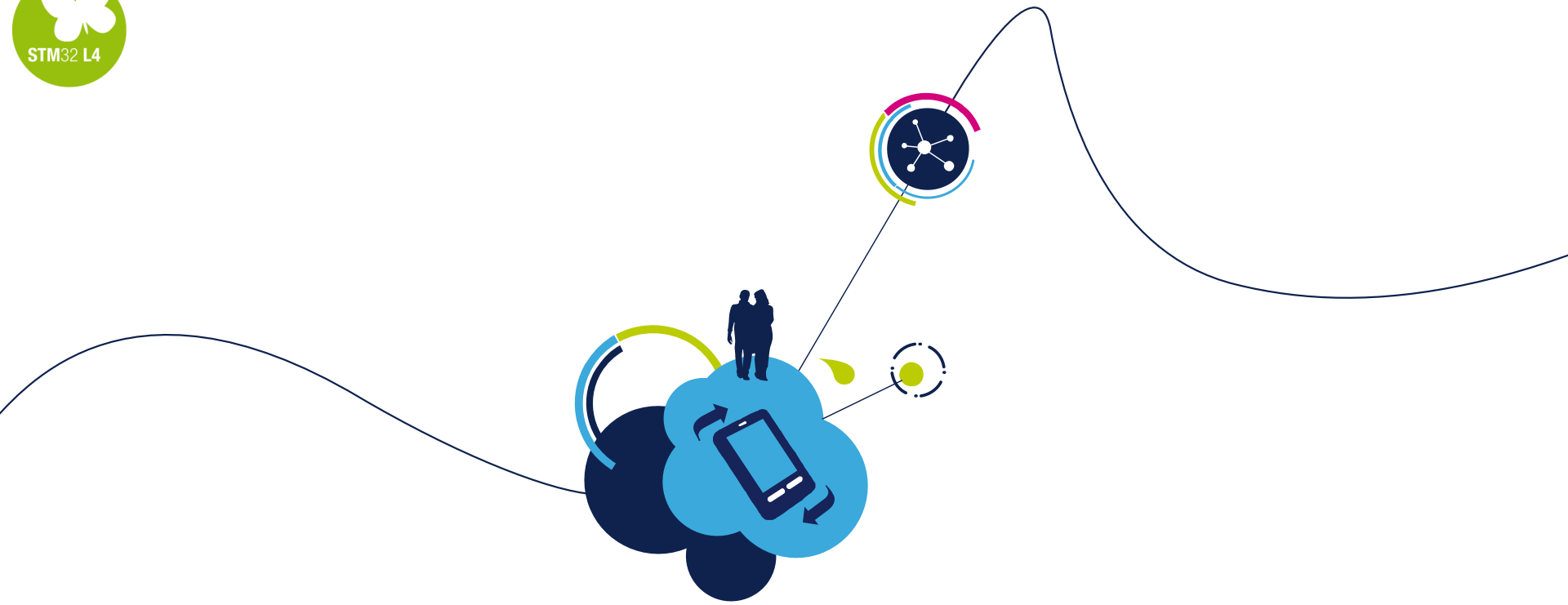
- Communication interface for single/dual/quad SPI flash memories
- Three operating modes
  - **Indirect** : all the operations are performed through registers (classical SPI)
  - **Status polling** : periodical read of the flash status registers (interrrupt generation)
  - **Memory mapped** : External flash seen as internal for read operations



# Main features



- Three functional modes:
  - Indirect
  - Status-polling
  - Memory-mapped with Execute in Place support
- Optimized operations
  - *Dual-flash mode (8 bits accessing two flash memories in parallel)*
  - SDR and DDR support
- Fully programmable
  - Opcode for both indirect and memory mapped mode
  - Frame format for both indirect and memory mapped mode
- Integrated FIFO for reception and transmission
  - 8, 16, and 32-bit data accesses are allowed
  - DMA channel for indirect mode operations

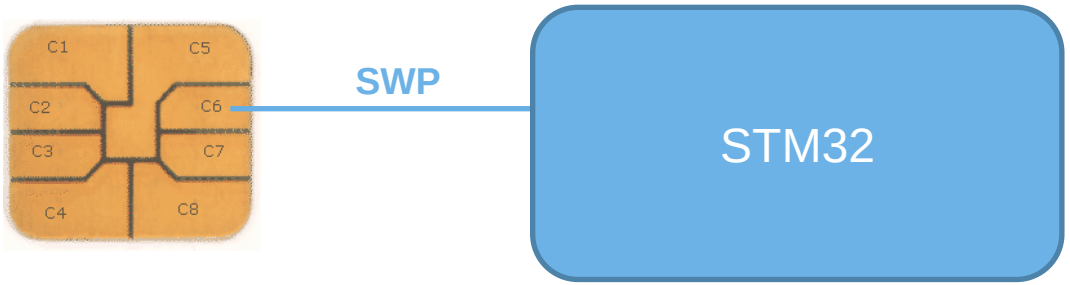


# SWPMI
## Single Wire Protocol Master Interface

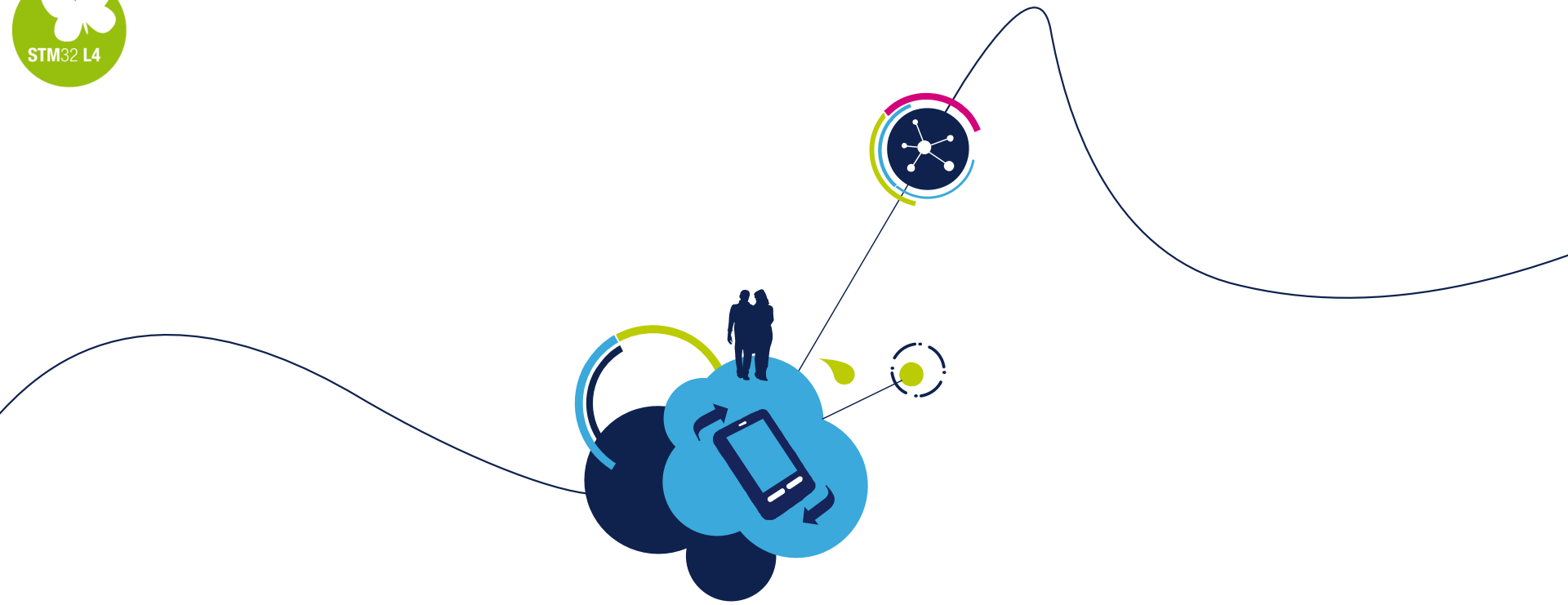
# Introduction



- SWPMI aims to implement a full-duplex single wire communication according to the single wire protocol defined in ETSI TS 102 613 standard
- The STM32 also embeds the SWP transceiver
  - SWPMI correponds to the Layer 2 (data link layer)
  - The SWP transceiver corresponds to the Layer 1(physical layer)
- STM32 SWPMI supports the master mode only (to be connected to a smart card)




- Bitrate configurable from 100kbit/s to 2Mbit/s



# USB OTG v2.x

# USB OTG v2.x new features summary



- Supports USB 2.0 Link Power Management (LPM)
- Supports the On-The-Go (OTG) Specification 2.0
- Optionally supports:
  - Attach Detection Protocol (ADP)
  - Battery Charging Detection (BCD) – same as on STM32F0x2

| | STM32F2 / STM32F4 | | STM32L4 |
|---|---|---|---|
| USB OTG IP revision | FS v1.2 | HS v1.1 | FS v2.0 |
| LPM supported | No | | Yes |
| OTG revision supported | 1.3 | | 1.3 & 2.0 |
| Device BIDIR Endpoints (including EP0) | 4 | 6 | 6 |
| Host mode channels | 8 | 12 | 12 |
| Total RAM | ~1,2 KB | ~4 KB | ~1,2 KB |
| Other features | - | - | ADP, BCD |

# USB OTG v2.x new features in brief



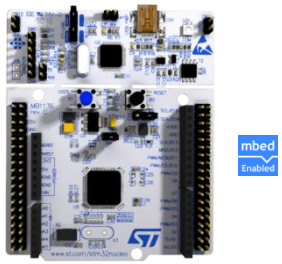
- LPM - Link Power Management
  - This adds L1 (Sleep), a new power state between enabled and suspended states. Device in this state is not required to reduce its power consumption, however, switching between enabled and sleep states is much faster than switching between enabled and suspended states, which allows devices to conserve power while idle.
- OTG revision 2.0 support (when enabled)
  - Adds support for Attach Detection Protocol (ADP)
  - The VBUS pulsing method of SRP is no longer supported. Only data line pulsing is supported.
- ADP - Attach detection protocol
  - Allows an OTG device, embedded host or USB device to determine attachment status in the absence of power on the USB bus.
- BCD - Battery charging detection
  - ability to detect and identify the type of port it is connected to (standard or charging)

# STM32L4 ecosystem



## HARDWARE TOOLS

### STM32 Nucleo



Flexible prototyping

### Discovery kit

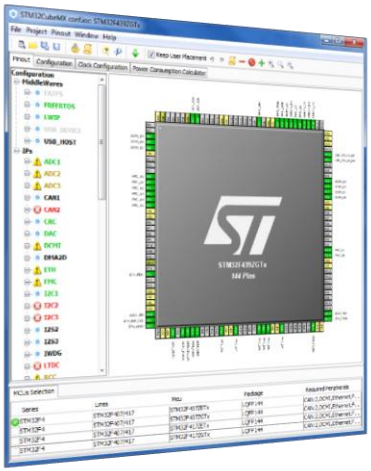
Key feature prototyping

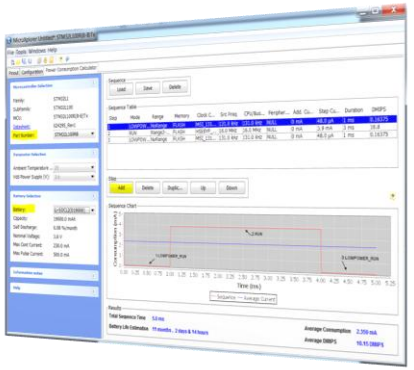
### Evaluation board

Full feature evaluation

## SOFTWARE TOOLS

STM32CubeMX featuring code generation and power consumption calculation

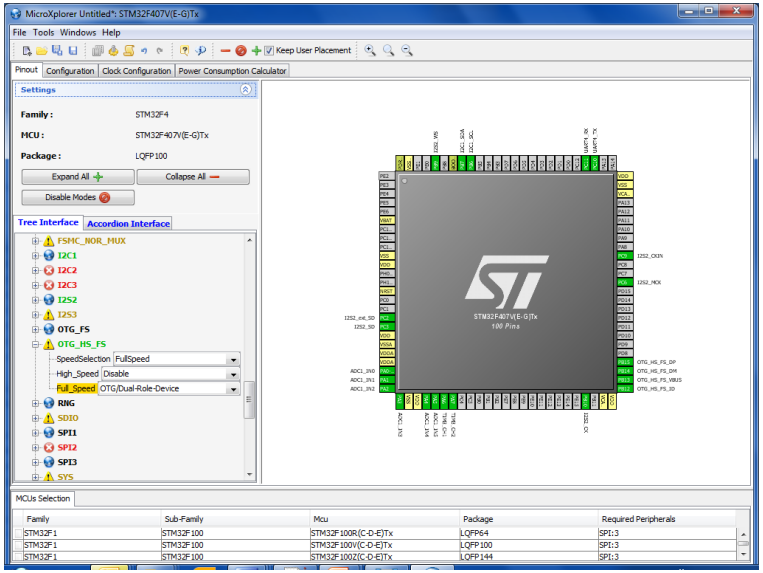


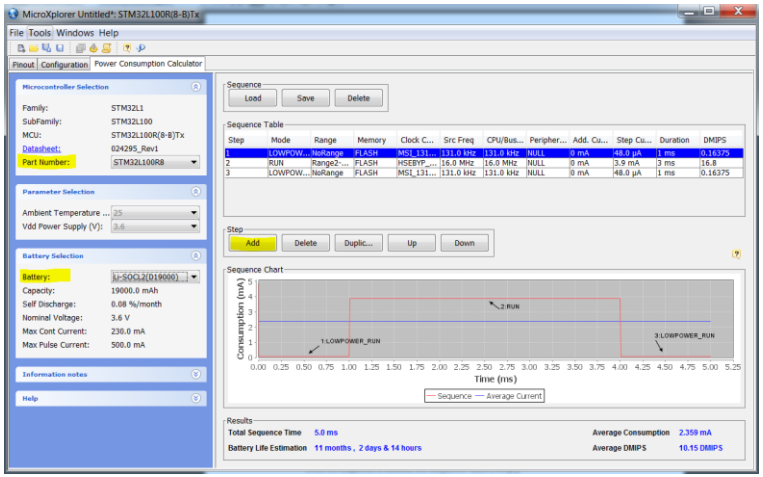


# STM32Cube™ V1 – Software Tool in brief



- STM32CubeMX is an extension of today existing MicroXplorer tool:
  - Step 1: Select the microcontroller
    - Smart Selector with advanced portfolio filtering choices
  - Step 2: Configure the microcontroller via wizards:
    - Pin out wizard, solving conflicts !
    - Clock Tree wizard
    - Peripherals and Middleware wizards, from SPI to TCP/IP !
    - Power consumption wizard
  - Step 3: Initialization code generation
    - Generates code for your favorite IDE !
- Automatic check for updates on st.com



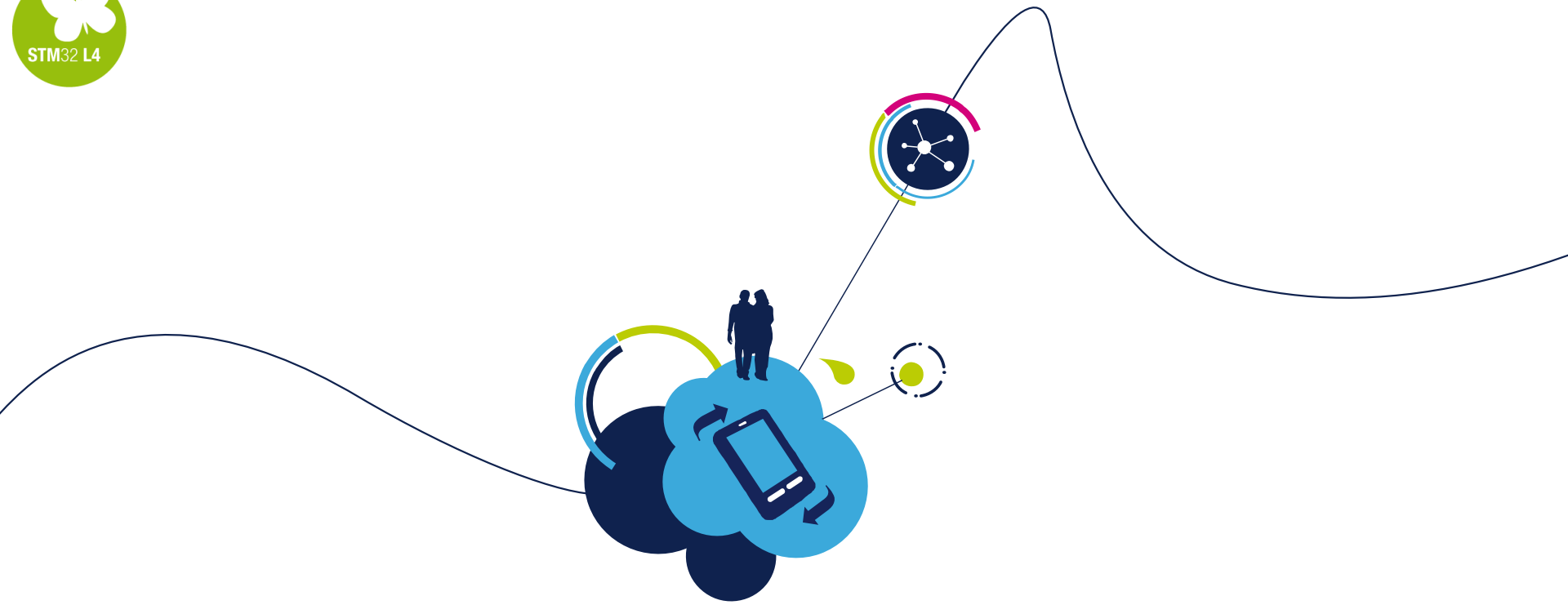
# STM32Cube™ V1 – Key Benefits



- **Consistent and Complete embedded software offer !**
  - Maximized portability between STM32 Series: seamless switch between series!
  - No more dependency headache: HAL and Middleware delivered altogether!
  - Easy to understand: Examples and demonstrations at all levels
  - Advanced demos putting altogether all the embedded software components
  - Fully documented

| Layer | Category | Provided Embedded software | Provided Examples |
|---|---|---|---|
| **HAL** | Analog | Analog/Digital conversions, Comparators, OpAmps, … | 150 examples<br>on ST evaluation boards* ! |
| | Timers | Timers, RTC, Watchdogs, … | |
| | Cryptography | CRC, AES, 3DES, Hash and Random Number generator, … | |
| | Connectivity | I2C, USART, SPI, I2S, SDIO, CAN, CEC, USB, Ethernet, … | |
| | Interface | External Memory, Display, Camera, Audio,… | |
| **Middleware** | RTOS | FreeRTOS open source RTOS, with CMSIS-RTOS wrapper | 40 examples<br>on ST evaluation boards* ! |
| | USB | USB Host and Device cores<br>Host Classes: HID, MSC, CDC, Audio, MTP<br>Device Classes: HID, MSC, CDC, Audio, MTP, DFU, CCID | |
| | TCP/IP | LwIP open source stack<br>with DHCP, DNS, ICMP, TCP, UDP, TFTP, HTTP, SSL/TLS (PolarSSL)… | |
| | File System | FatFS open source file system<br>with enhanced mechanisms like NAND handling | |
| | Graphic | STemWin professional stack<br>coming from SEGGER and available in binary form | |
| **Application** | Demonstration | Full demonstrations for ST boards | ~23 boards will be supported ! |

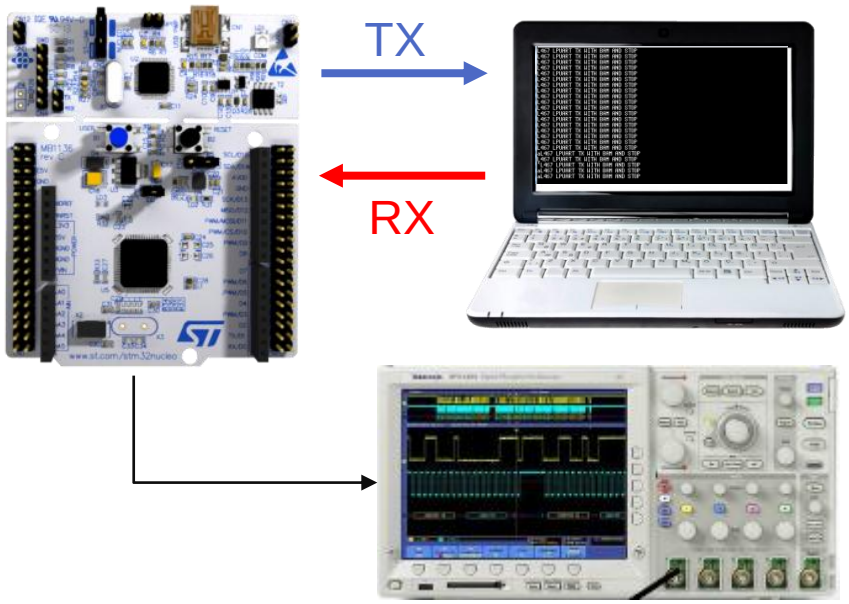
*: STM32 F4 Serie



# STM32L4 Demonstration

# Low Power Communication with LPUART + BAM

- LPUART
  - Clock from LSE 32.768KHz
  - Baudrate 9600 bps
  - Using DMA



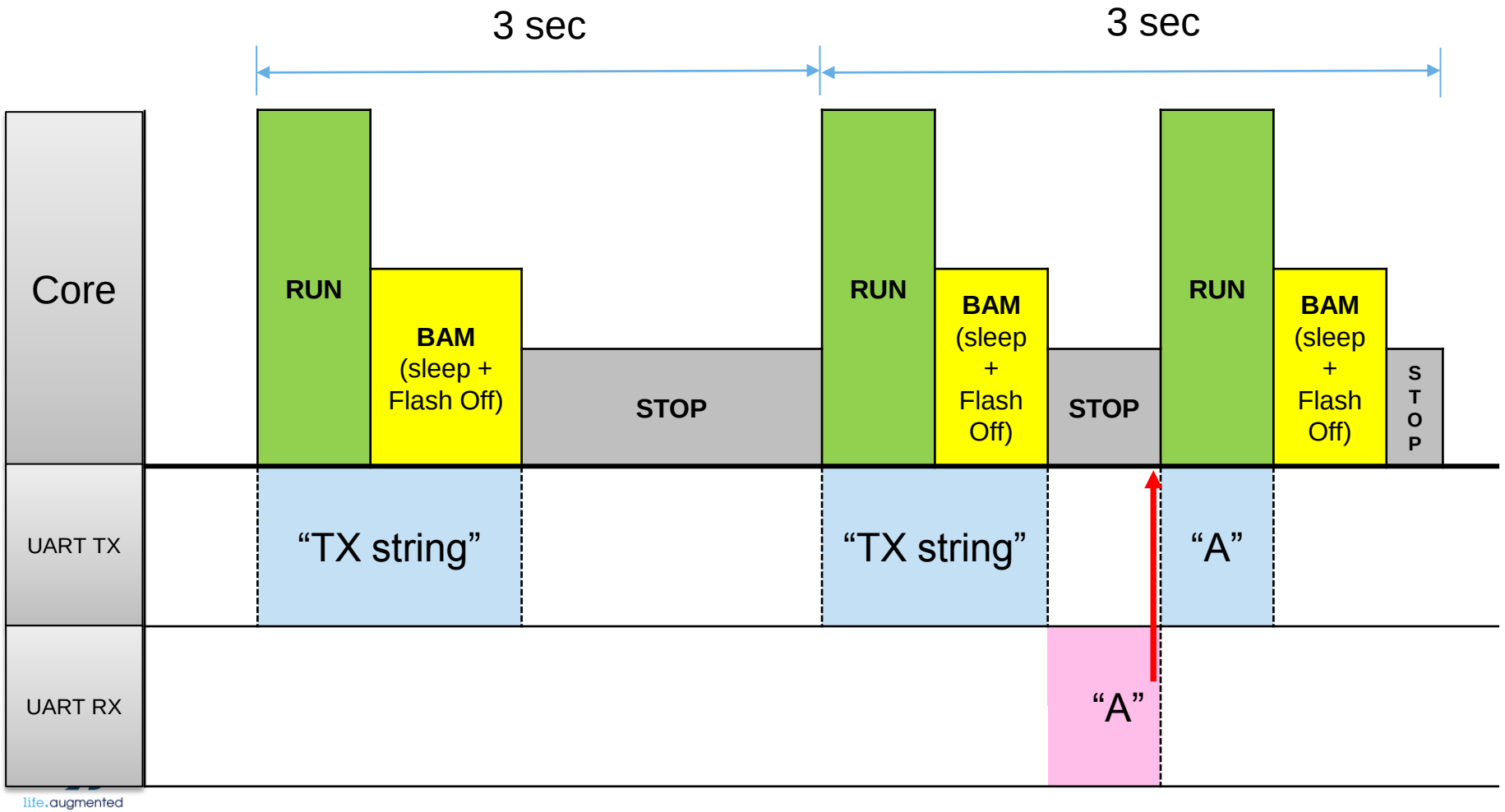

- Run mode
  - System clock 80MHz by PLL
  - PLL clock source : HSI 16MHz

- BAM (Batch Acquisition Mode)
  - Optimized mode for transferring data with communication peripherals, while the rest of the device is in low power mode.
    - Flash is put in power-down mode and Flash clock is gated off during Sleep mode

- RTC
  - wake-up time : 1 sec

# Low Power Communication with LPUART + BAM

- LPUART + BAM(Batch Acquisition Mode) + STOP mode



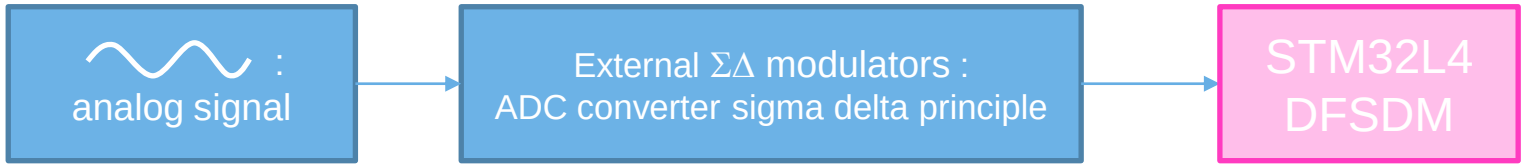
# Low Power Communication with LPUART + BAM



- 데모 중….

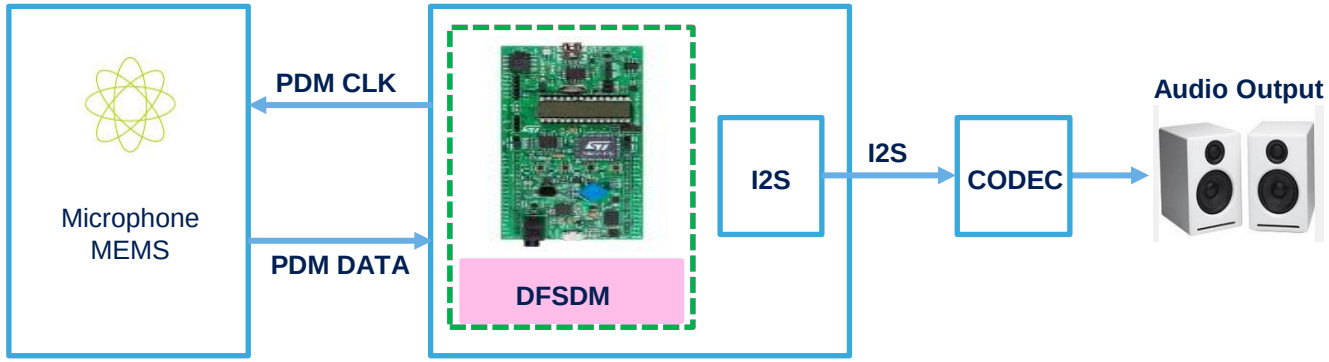
# Mono audio recorder with DFSDM + MEMES microphone

- DFSDM (Digital Filter for Sigma Delta Modulators)
  - Implements complete post-processing from external ΣΔ modulators outputs.

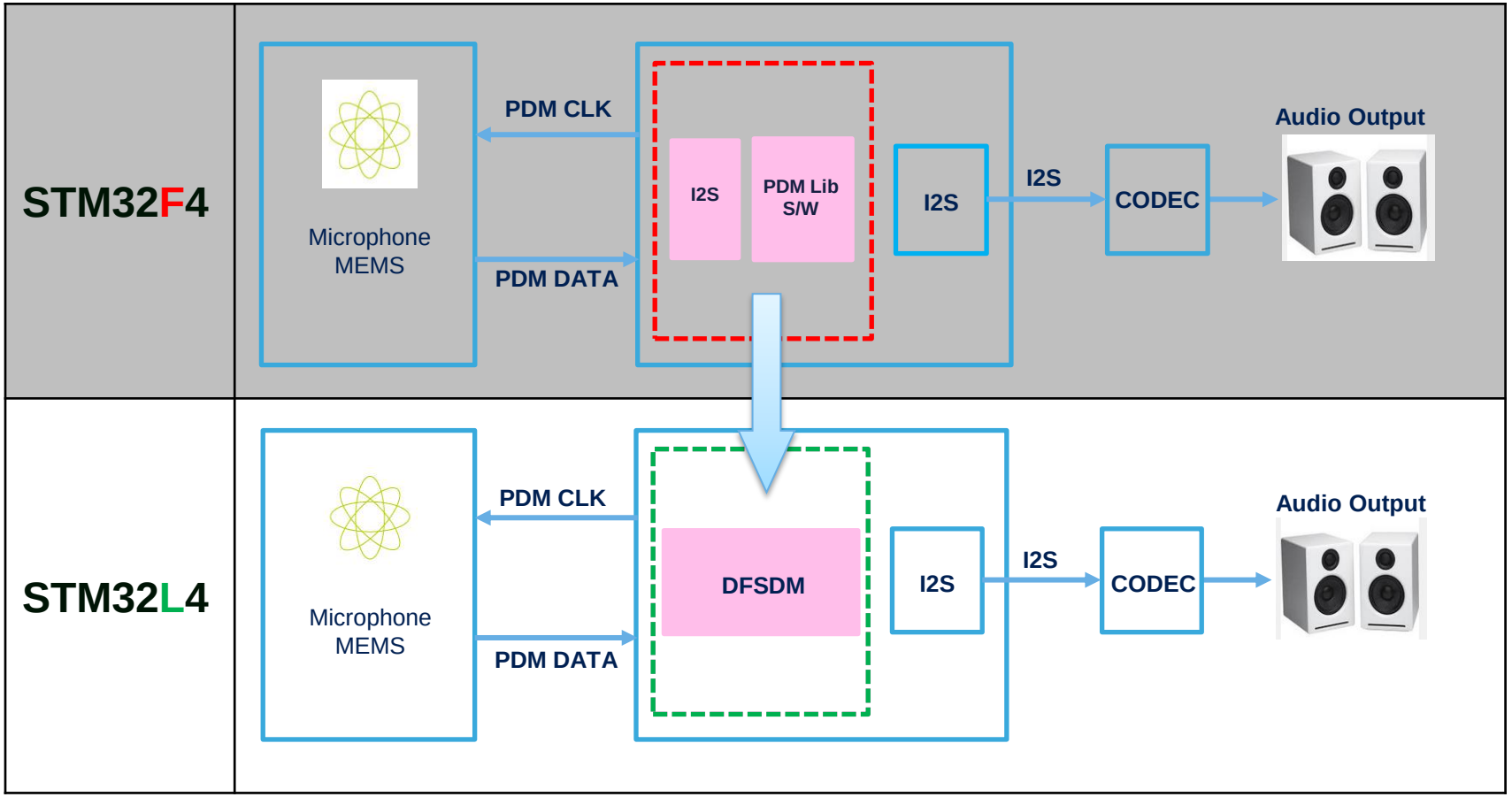



- The purpose is to demonstrate the DFSDM function with external digital MEMS microphone
  - Use external MEMS microphone
  - Continuous mode with one DFSDM filter and DMA transfer

- Send collected mono audio data on the fly to audio output → speaker



# Mono audio recorder with DFSDM + MEMES microphone



# Thank you




www.st.com/stm32l4